TDA1541A Balanced Driver

What it does

This circuit takes I2S data (with any number of bits per frame) and splits up the stream so that it can feed 2 x TDA1541As running in simultaneous data mode. The output of the circuit drives a channel of one TDA1541A with L+ and the other channel with L-, so that the DAC is producing L +/- balanced output. The other TDA1541A is operated in a same manner, but with R +/- balanced output.

Some things to consider:

- The output current swing of the DAC, the circuit here is splitting the phase in the digital domain.
- The digital representation of audio, remember that both offset binary and 2' complement are asymmetrical in terms of the largest positive and largest negative integer they can represent. Unlike sign-magnitude, there is no –0. To invert the phase of the digital audio, you DO NOT add 1 after the bit inversion.
- All output from this circuit is delayed by exactly one cycle of the input bit clock BCK. This is why you see `datal_n` and `datar_n` in phase with `data`.

How it does it

This is just taken from my previous posts on diyAudio, and may give some hints, it does not necessarily apply to this circuit, although the principal of operation hasn't change:

"When input OB/TWC input is connected to VDD1 the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. "

If you look at the timing data below, you'll see that LE goes high after the LSB has been clocked in, and loads the data from the shift register used to receive it internally. Now from I2S, we are able to select left/right data based on WS. So for example if WS is low, we select left, and feed I2S - BCK to LCK (the burst wave). With it goes the data. If the LCK clock isn't ticking, it won't load any data in, that's why it remains low (after the falling clock-in edge), at this time the right one takes over. Now with I2S, WS changes before the LSB is clocked in (rising edge) , with the simultaneous mode we want the latch to open after the LSB has been clocked in (on the falling edge), so the WS signal is delayed appropriately.

The timing chart below shows that LE must close before the data for the next word is clocked in (starting with the MSB), and this is fine, cause the clock LCK/RCK don't tick in the period where RLE /LLE is high (latch open) and no data is clocked in. Before the clock starts up again, LLE or RLE close, so that the data may be loaded.

As for the two's complement to offset binary conversion, this can simply be done by inverting the MSB of each word. When WS on the I2S bus changes, the next rising edge of BCK is the LSB of the pervious word, and on the rising edge after that, is the MSB of the new word. We use WS and a few D-F/F to find the MSB, ie. a signal that goes high when the MSB of a word is present in the stream. And, pass the DATA and the find-MSB signal through a XOR gate. The XOR gate will invert the DATA when the find signal is high, therefore inverting the MSB, doing tow's complement to offset binary conversion.

The final stage uses a counter to count in the first 16 bits from each channel, and this must be done to stop the remaining bits from flushing out the data. Different sources can have different frame widths.

Disclaimer

Use may use this information for all non-commercial purposes, at your own risk. I do not take responsibility for any inaccuracies, or consequent damage that may arise from the use of this information. So if you blow up your pair of TDA1541A/S2s, then don't come complaining to me! ☺

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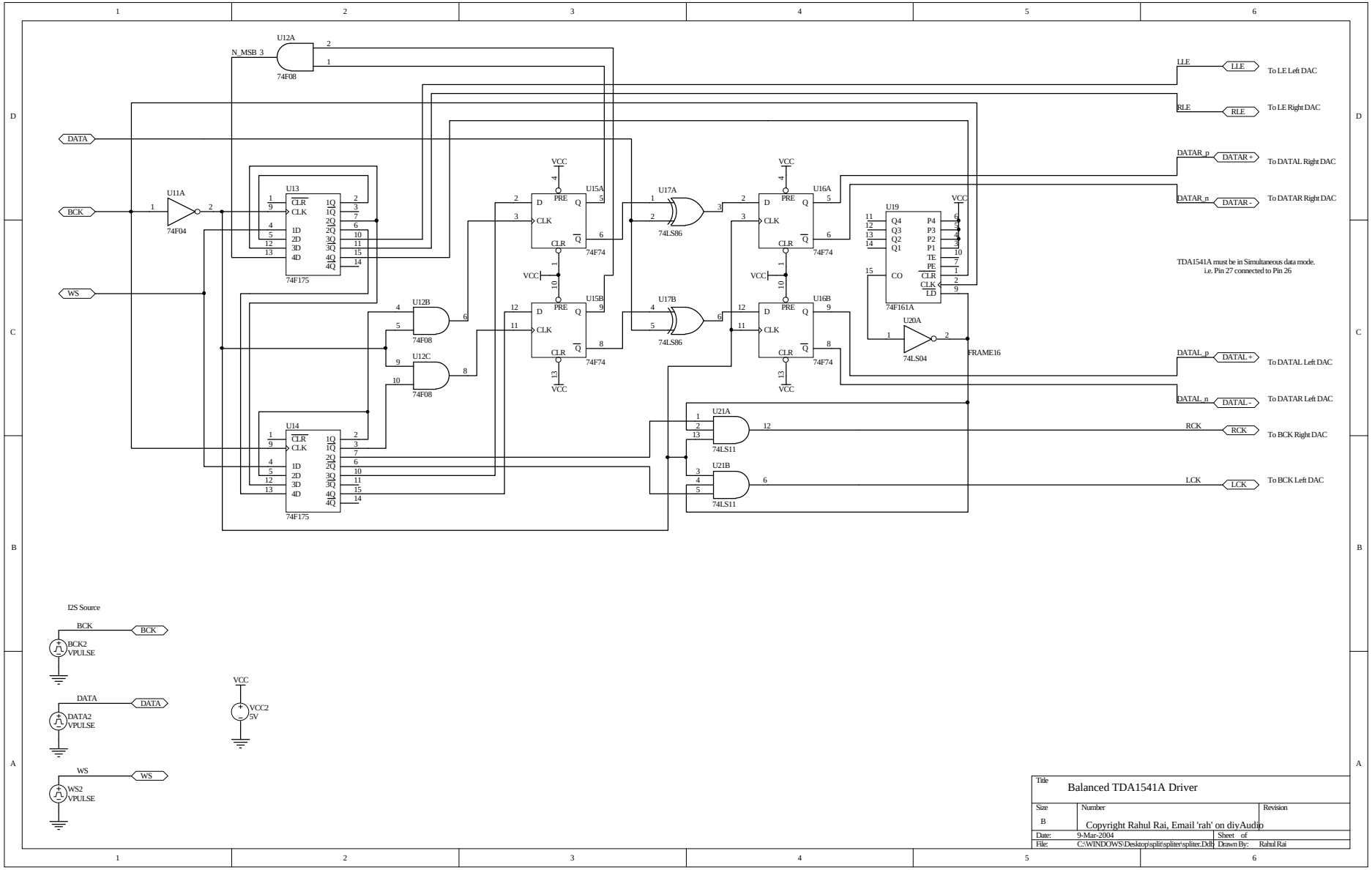
(Email 'rah' on diyAudio)


U12A
N_MSB 3
74F08
LLE
To LE Left DAC
RLE
To LE Right DAC
DATA
DATAR_p
DATAR +
To DATAL Right DAC
BCK
U11A
74F04
U13
74F175
DATAR_n
DATAR -
To DATAR Right DAC
VCC
U15A
U17A
U16A
U19
74F74
74LS86
74F161A
TDA1541A must be in Simultaneous data mode.
i.e. Pin 27 connected to Pin 26
WS
U12B
74F08
U15B
U17B
U16B
U20A
74LS04
FRAME16
DATAL_p
DATAL +
To DATAL Left DAC
DATAL_n
DATAL -
To DATAR Left DAC
U12C
74F08
U14
74F175
U21A
74LS11
RCK
RCK
To BCK Right DAC
U21B
74LS11
LCK
LCK
To BCK Left DAC
I2S Source
BCK
BCK2
VPULSE
DATA
DATA2
VPULSE
WS
WS2
VPULSE
VCC
VCC2
5V
Title
Balanced TDA1541A Driver
Size
B
Number
Revision
Copyright Rahul Rai, Email 'rah' on diyAudio
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9-Mar-2004
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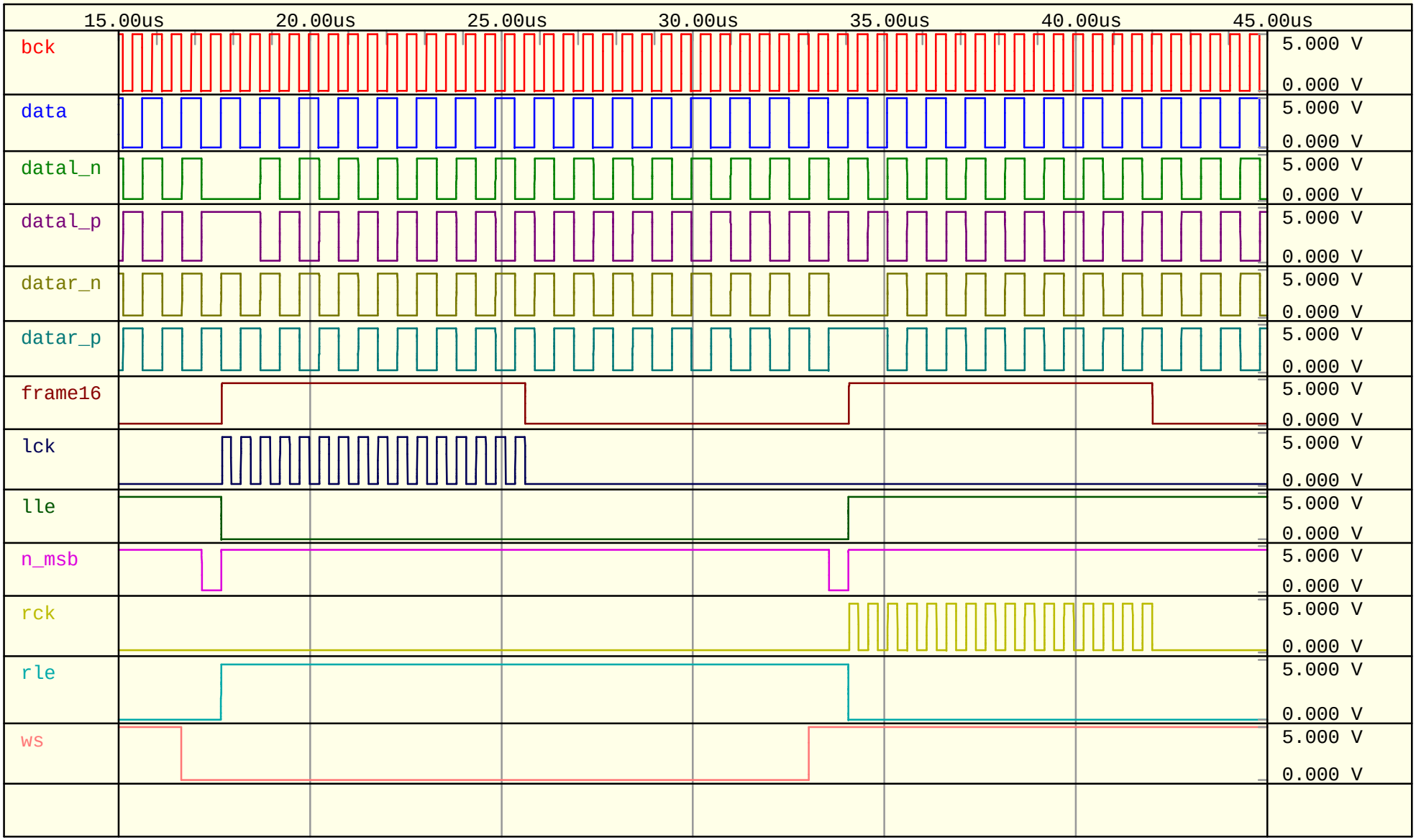
Drawn By:
Rahul Rai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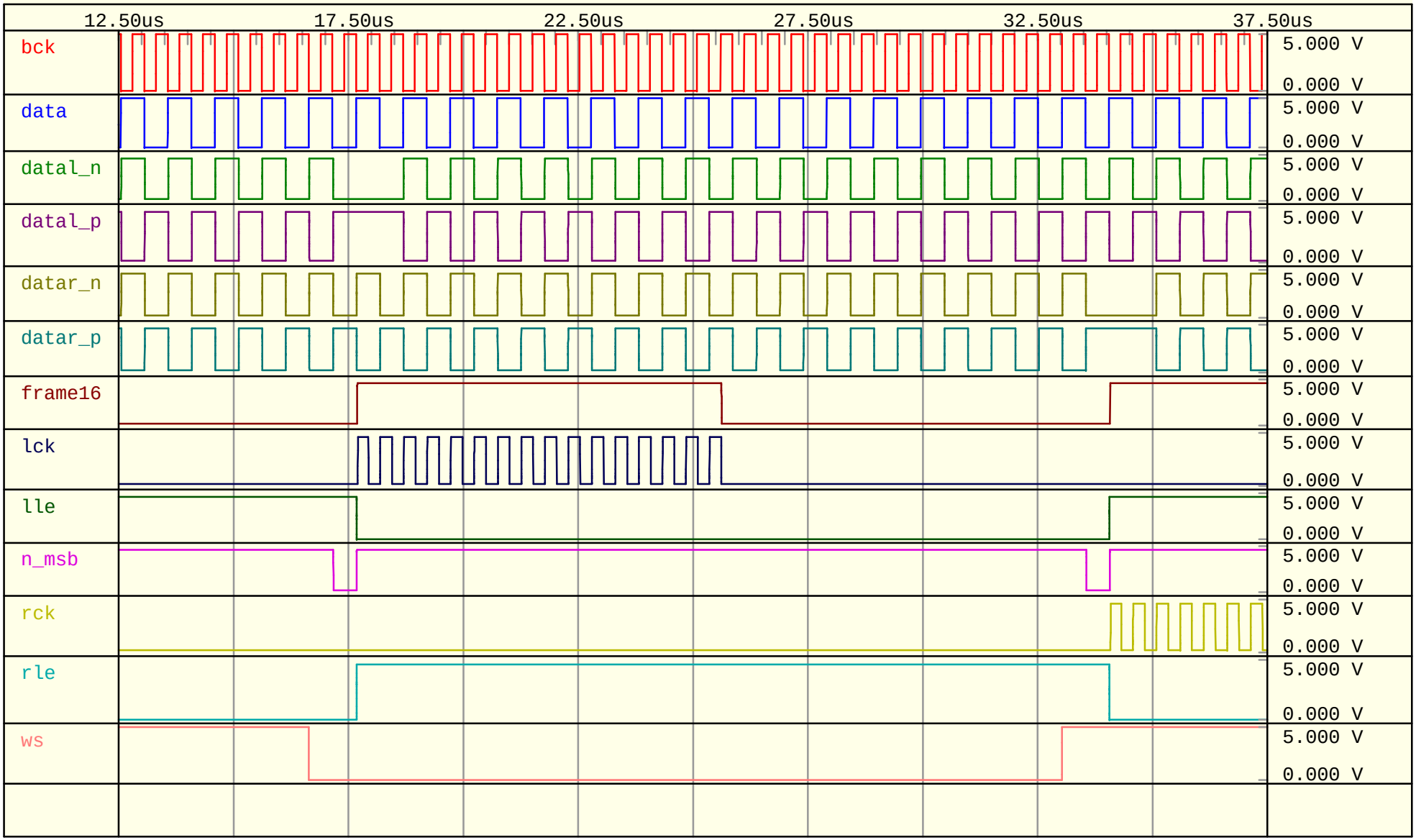
20.00us
25.00us
30.00us
35.00us
40.00us
45.00us
bck
data
datal_n
datal_p
datar_n
datar_p
frame16
lck
lle
n_msb
rck
rle
ws
5.000 V
0.000 V


12.50us
17.50us
22.50us
27.50us
32.50us
37.50us
bck
data
datal_n
datal_p
datar_n
datar_p
frame16
lck
lle
n_msb
rck
rle
ws
5.000 V
0.000 V