ARCAM

AVR400 Service Manual Issue 1

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ECO NR.	DATE	CHG.	ZONE	DESCRIPTION OF CHANGE	REL.	DR.	CHK.
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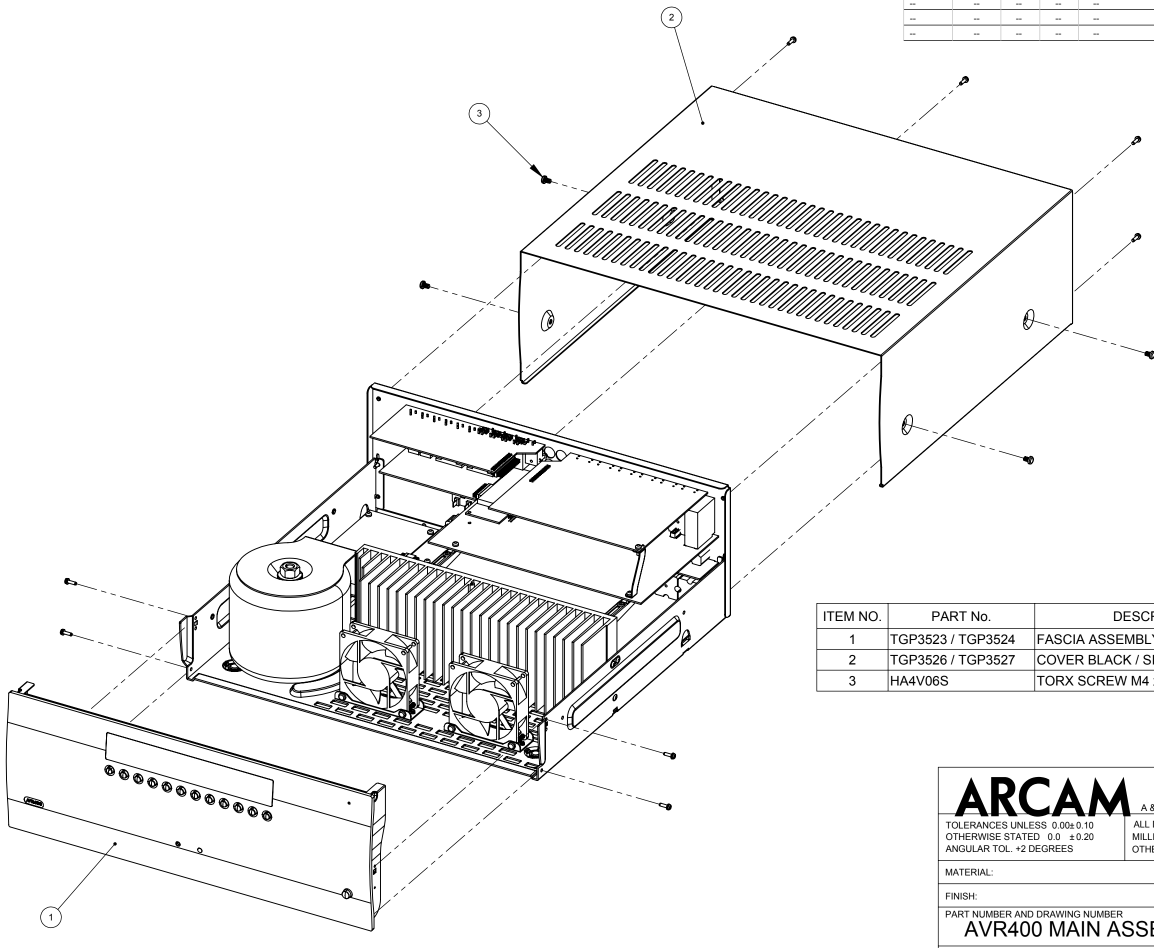

ITEM NO.	PART No.	DESCRIPTION	QTY
1	TGP3523 / TGP3524	FASCIA ASSEMBLY BLACK / SILVER	1
2	TGP3526 / TGP3527	COVER BLACK / SILVER	1
3	HA4V06S	TORX SCREW M4 x 6	4

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		DATE:	7-9-2010
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		ORIGINAL SCALE 1:4	
MATERIAL:			
FINISH:		SHT 1 OF 4	
PART NUMBER AND DRAWING NUMBER AVR400 MAIN ASSEMBLY			
DRAWING TITLE COVER + FASCIA			A3

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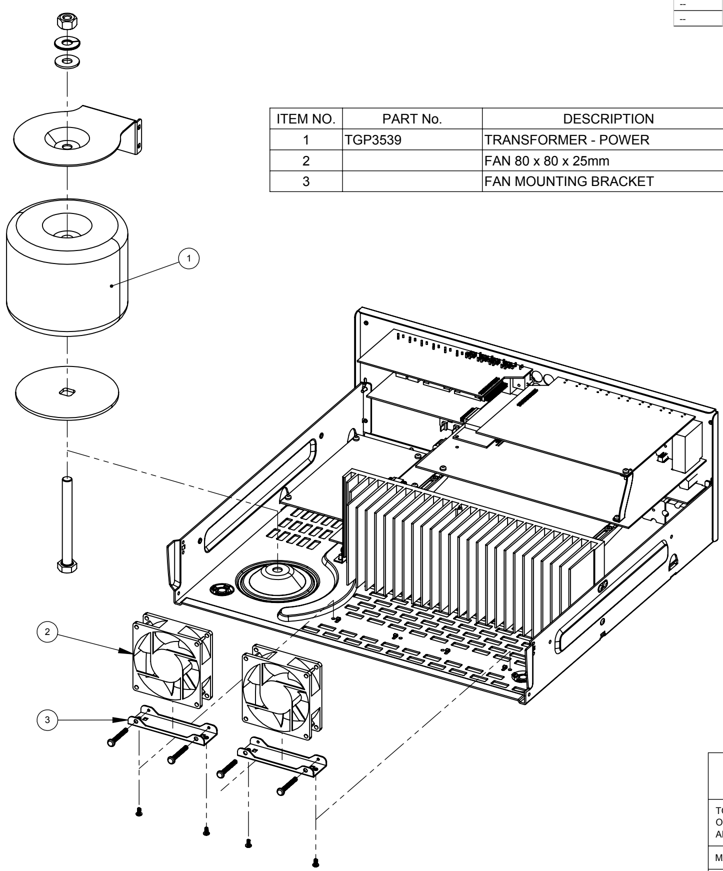

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ITEM NO.	PART No.	DESCRIPTION	QTY
1	TGP3539	TRANSFORMER - POWER	1
2		FAN 80 x 80 x 25mm	2
3		FAN MOUNTING BRACKET	2

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SHT 2 OF 4

PART NUMBER AND DRAWING NUMBER
AVR400 MAIN ASSEMBLY

DRAWING TITLE
FANS + TRANSFORMERS

A3

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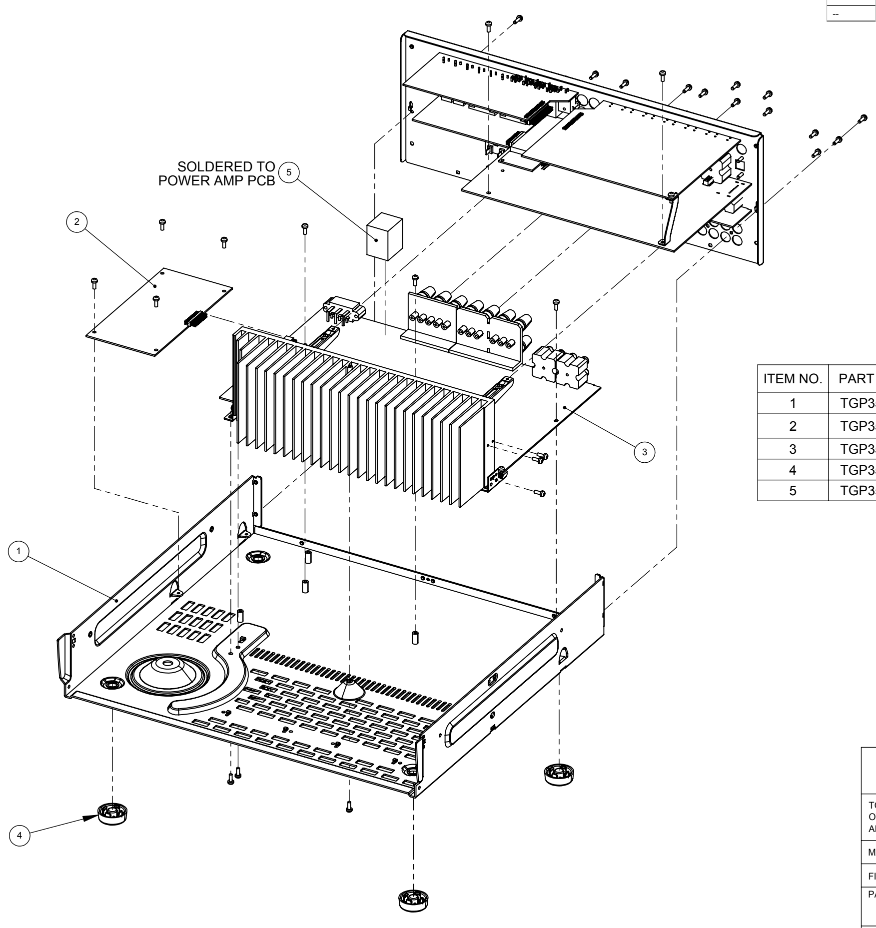

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ITEM NO.	PART No.	DESCRIPTION	QTY
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2	TGP3535	FRONT PCB ASSY	1
3	TGP3538	POWER AMP PCB ASSY	1
4	TGP3525	FOOT ASSY	4
5	TGP3540	TRANSFORMER - STANDBY	1

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PART NUMBER AND DRAWING NUMBER

AVR400 MAIN ASSEMBLY

DRAWING TITLE

POWER PCBs + FEET

A3

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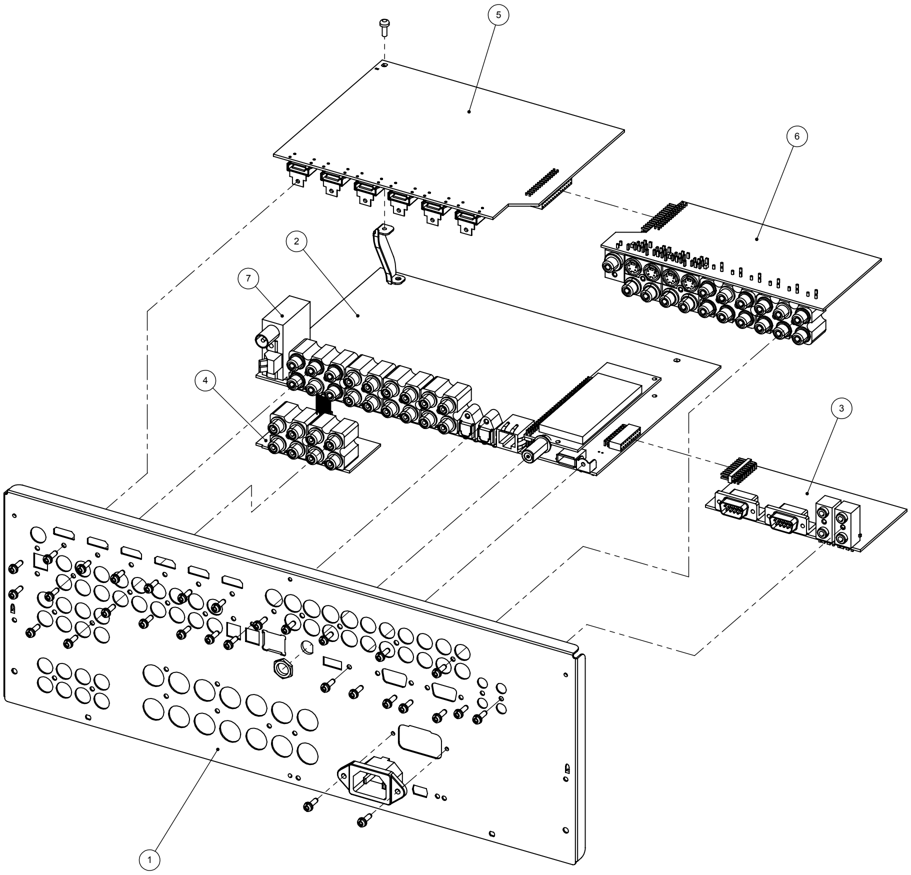

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3	TGP3536 (part)	INPUT PCB ASSY - ETHERNET	1
4	TGP3536 (part)	INPUT PCB ASSY - CONNECTORS	1
5	TGP3537	HDMI PCB ASSY - MAIN	1
6	TGP3537 (part)	HDMI PCB ASSY - VIDEO	1
7	TGP3529 / TGP3530	AM/FM TUNER EU / US	1

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MATERIAL:

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SHT 4 OF 4

PART NUMBER AND DRAWING NUMBER
AVR400 MAIN ASSEMBLY

DRAWING TITLE
REAR PANEL + PCBs

A3

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AVR400 Power Amplifier Circuit Description

Apart from the power transformer, the power amplifier electronics is fully contained on the large double sided PTH PCB and heatsink located at the bottom of the AVR400. This is called the Main Board on the schematic diagrams (pages 11 and 12). *The Main Board also contains the mains input circuitry, including the safety fuses and standby power transformer, so great care should be exercised when probing this area of the board.*

Note that some small surface mount components are soldered to the underside of this PCB.

The 7 power amplifiers are identical in terms of circuitry, although necessary compromises in the physical layout may give rise to slight differences in measured noise, crosstalk and distortion performance. The two channels at the extreme ends of the heatsink have less radiating area available to them and will run hotter under load – this is not normally an issue as these are assigned to the SBL and SBR channels.

Looking from the rear of the AVR, facing the flat face of the heatsink, the channel order is SBR, SR, FR, C, FL, SL and SBL, the same order as the loudspeaker terminals. The SBL and SBR channels can also be assigned to zone 2 or as duplicates of the FL and FR channels for when passively biamping the main stereo loudspeakers. In this latter condition we recommend assigning the SBL and SBR outputs to the tweeters of the FL and FR speakers, in order to minimize the power amplifiers' heat dissipation.

Note that the 8 pre-amplifier outputs are also on this PCB – apart from SUB their phono sockets are effectively in parallel with the power amplifier inputs, which are fed from the Input Board via a ribbon cable and CON103. This connector also carries 5 power supply and power amplifier control signals to and from the system microprocessor (µP) IC151 situated on the Input Board above the Main Board.

The amplifiers' power supply is provided from a centre-tapped secondary winding on the toroidal power transformer, via the connector BN508, to the bridge rectifier D5830. This is mounted on a small PCB near the top of the heatsink. The rectified AC is then sent to the main PCB via connectors BN581/582. To avoid induced hum and distortion it is important to keep these cables twisted tightly together and well away from the actual power amplifier circuitry. The main 15,000µF 80V reservoir capacitors, C835 and C836, are positioned on the main PCB well away from the power amplifier input traces and close to the system star ground. The smoothed DC is fed to the power amplifiers' Vcc and Vee lines near the centre of the heatsink via a twisted-pair cable, again to minimize induction into the power amplifiers. Vcc and Vee are typically +/- 52V at 234VAC with no signal. Q5845 sends a fraction of Vcc to the muting control on the Input Board.

The FL (front left) channel will now be described in detail.

The *input stage* is a long tailed pair Q5101 and Q5102, with local degeneration provided by R5105 and R5107. The tail is fed from the negative rail via an approx 3mA ring-of-two constant current source, Q5109 and Q5110. R5101 and C5101 at the input provide high frequency rolloff and help keep residual DAC ultrasonic noise above 100kHz out of the power amplifier. DC blocking is provided by C5102 at the input and C5107 in the feedback loop so that the whole power amplifier has unity gain at DC. The midband AC gain is 22000/680 = 32.35 after allowing for the attenuation provided by R5101 and R5102. Thus 875mV at the input produces 100W into 8 ohms at the output.

The long tailed pair's collectors are loaded by a current mirror, Q5103 and Q5104. The resistors R5103/4 and R5105/6 are 1% tolerance to minimize even order distortion. The collector of Q5101 also feeds the Darlington *class A voltage amplifier stage (VAS)* made up of Q5115 and Q5116. Q5113 is loaded by the output stage and the 8mA constant current source made up by Q5125 and Q5126. The amplifier's main frequency compensation network (for stability) comprises C5115 plus the combination of C5116 and R 5115. This adds gain inside the loop (two pole compensation) at high audio frequencies so that the

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additional feedback further reduces high frequency distortion and crossover distortion within the audio band.

These stages are partially decoupled from the Vcc and Vee power supplies by D5130/R5130/C5130 and D5129/R5129/C5129 respectively. They are also bootstrapped to the amplifier output via the networks R5118/C5128/R5128 and R5117/C5127/R5127. This raises the supply lines by approximately 3V at full output to avoid clipping the driver stage prematurely.

The *output stage* comprises classic complementary emitter followers Q5150/Q5170 (NPN) and Q5160/Q5180 (PNP). The On Semiconductor output transistors have a current gain that is sustained to about 10 amps and a very large safe operating area, which allows the amplifiers to drive low impedances well. They also have built-in thermal compensation diodes which helps stabilize the quiescent current both statically (when hot) and dynamically (when playing music at high level) – this minimizes crossover distortion and improves sound quality.

The output stage biasing is performed in the network around the amplified diode Q5120, which is mounted in intimate thermal contact with the driver transistor Q5130, plus the two built-in diodes associated with the output transistors. The thermistor R5122 is positioned on the PCB close to the heatsink and provides extra downward compensation at very high temperatures. Bias is set by VR51 and is largely independent of temperature – it should be set to16-20mV when measured across the outer terminals of the compound emitter resistor R5175, using the 2 pin connector CN51, 5 minutes or more after the AVR400 is powered up.

The power amplifier output is routed across the PCB to the back panel. It includes a Zobel network (sometimes called a Boucherot cell) R5183/C5183 and a series inductor L5185 damped by a 4.7R 2W resistor R5184. These components help isolate the amplifier from reactive loads to ensure high frequency stability. One half of the normally-off relay RL52 is used to switch the load in and out.

Each power amplifier is protected against overload in a number of ways. The complementary transistors Q5130 and Q5131 protect the NPN half of the output stage and Q5140 and Q5141 the PNP half. They operate as Sziklai pairs, passing negligible current until a threshold voltage of approx 600mV is reached across R5132 and R5142. Between 600 and 700mV the pairs then ramp up current smoothly, diverting it away from the bases of Q5150 and Q5160 to limit the output stage drive to a safe level, within the power transistors' SOA (safe operating area). The 600mV threshold voltage depends upon both the instantaneous current and voltage across the output transistors, set by the networks R5132/R5136/R5137/R5138/R5175 for the top half and R5142/R5146/R5147/R5148/R5175 for the bottom half. R5135/R5145 and the zener diodes D5135/D5145 change the slope of the protection locus at high Vce voltages. R5134/R5135 plus C5134/C5145 prevent fast transients and brief overloads from prematurely triggering the protection.

The above dual slope SOA protection is self resetting but if a gross overload persists for more than a second or two (such as when a channel's output is short circuited with music playing at a moderate to loud level) then the open collector transistor Q5181 sinks current for long enough to initiate the amplifier's full shutdown procedure via the line SOA_PROTECT. This can also be triggered by a total output stage failure (which passes enough current through R5175 to turn on Q5188) via OVERLOAD or by an excessive DC offset at the output terminals (via R5185) via V_DET. All these signals, and others, feed into the protection module, described below.

The *protection module* comprises 8 transistors and associated parts positioned at the back of the PCB near the preamplifier output sockets. It has a single output line named PROTECT which, when pulled down from Vcc to ground, instructs the system µP IC151 to shut down the whole amplifier. This occurs when any of the following events happen:

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1) Any amplifier channel pulls current through the SOA_PROTECT line for long enough to charge up capacitors C5871 and then C5872 so that Q5874 turns on.

2) Any amplifier channel pulls current through the OVERLOAD line for long enough to charge up C5882 and turn on Q5882 and thus Q5884.

3) Any amplifier channel has a large long term (DC) offset (typically greater than +/-3V) sμFficient to charge up C5861 enough to turn on either Q5862 (positive offset) or Q 5864 (negative offset). These then turn on Q5863. N.B. This circuit is also used to detect imbalances in both the Vcc/Vee and +/-15V power supplies (the latter is generated on the Power Supply board).

4) When the PTC thermistor TH585 mounted at the top centre of the heatsink gets sμFficiently hot (around 100C) and thus high resistance enough to cause Q5855 to turn on via the +12V supply. Intermediate temperatures will not activate PROTECT but will provide signals to the level detectors associated with the FAN_1 and FAN_2 lines, to run the cooling fans at high or low speeds respectively.

Note that the fans' 12V supply is gated via Q5909 and Q5911. This means the fans will not run when no signal is present on the FL, C or SR channels, so that during quiet passages no fan noise should be audible.

AVR400 Main Power Supplies Circuit Description

The main DC power supplies are located on the Power Supply Board - a double sided PTH PCB adjacent to the Main Board. Note that the mains input switching, mains fuses, standby power transformer with its associated unregulated DC supply and the relay for enabling the power amplifier supply rails are located on the Main Board. The two boards communicate via CON501.

Considering the **Main Board** first, the mains voltage switching uses a double pole double throw slide switch accessible from the back panel. One pole addresses the standby transformer and the other the toroidal power transformer. *Ensure the switch setting matches the supply voltage before switching on the AVR400*. Nominal settings are 115 and 230V +/- 15%. The 20mm 115V fuse in line with the toroidal transformer is rated at 15A T (Time delay) and the 20mm 230V fuse is rated at 8A T. *Always replace these fuses with the same type and value*. The standby transformer T5941 is not fused but is designed to go open circuit in case of overheating (e.g. if left connected to a 230V supply for longer than a few minutes when the mains voltage selector is set to 115V).

The standby transformer generates approximately +9V DC via the bridge rectifier diodes D5495/6/7/8 and the 1,000μF reservoir capacitor C5947.This is sent via pin 7 of CN501 to the Power Supply PCB (confusingly marked as 5V). The rail voltage is also routed to the system microprocessor (μP) via D5965/R5965 and pin 6 of CN103 as POWER_MUTE.

The 5V relay RY594 is normally open. When the mains switch is closed then the SUB_POWER rail (approx +4.3V) is activated from the Power Supply PCB via the standby transformer. When the system has booted correctly, without any shutdown signals, then the POWER_RELAY signal from the system μP also goes high, pulling down Q5947 hard. Only then does the relay close and switch on the main toroidal power transformer, enabling the rest of the system to boot up.

Now consider the **Power Supply Board**, found on page 14 of the schematic. This generates all the main DC supplies for the AVR400 except +Vcc and -Vee for the power amplifiers and the non-logic part of the VFD display requirements of the Front Panel Board. Note that additional local regulation also takes place on the other PCBs, e.g. for large digital ICs.

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Two secondary windings from the toroidal power transformer are fed in via CN63. Pins 1, 2 and 3 connect to a centre-tapped secondary winding used to generate approx +/- 20VDC via the bridge rectifier diodes D603/3/4/5 and the 2,200µF 35V reservoir capacitors C609 and C610. *R603 and R604 are 0.47R 1W fusible resistors for circuit protection – if they fail replace only with the same type and value.*

The 3 terminal regulators IC63 and IC62 are mounted on two of the larger heatsinks near the back of the amplifier. These provide +/-15V to the op amps on the amplifier's Input Board via the 11-way connector BN62. The Input Board also then routes the +/-15V onwards to the Front Panel Board.

Pins 4 and 5 of CN63 receive AC from another transformer secondary to generate approx +15VDC via the heatsink mounted bridge rectifier D601 and the 18,000µF 25V reservoir capacitor C631. *F601 and F602 are hard wired 6.3Amp T (time delay) fuses for circuit protection – if they fail replace only with the same type and value.*

This +15V unregulated supply has 4 main outputs:-

1) It is regulated down to +12V with the low dropout (LDO) 3 terminal regulator IC64. This is situated on the heatsink closest to the Main Board, near the back panel. Its output goes to BN62 for the +12V triggers and also to CN501, to drive the power amplifiers' cooling fans.

2) It supplies the HDMI Board via CN61. To minimize ripple currents in the ground return, Q643 is wired as a low dropout voltage follower with low pass filtering via R650 and C569.

3) It feeds the switched mode buck regulator IC61 via L631 and C615. The tank circuit comprises L632, C640 and C641, discharged via D631. R636 and C643 make up a snubber to reduce overshoot. This provides a high current +5V supply to the Input Board via pins 4 and 5 of BN62. This 5V supply also feeds two 3V3 linear regulators, IC67 and IC68. These in turn supply the audio DSP ICs on the Input Board via pins 10 and 11 of BN62.

4) It feeds the +5V 3 terminal LDO regulator IC66 via the diode D616, which itself is preceded by the smoothing network comprising R615 (2W 15R) and C615. Note IC66's output is actually approx +5.7V because of D644 in its ground line; this is brought back to +5V after D643, to feed the relay

IC66 is noteworthy because it continues working when the amplifier is in standby.

It takes a second input from the +9V standby power supply on the Power Amplifier PCB – D616 acts as a gate to prevent this from feeding back to the +15V supply when the system is in standby. It also allows the +15V supply to override and remove the load from the +9V supply when the amplifier is fully booted up.

D606 and D607 form half of a second bridge rectifier (with the other two diodes coming from the full bridge rectifier D601). These diodes charge up the 1µF/50V capacitor C604 to +15V, generating a "mains power present" signal. The 10K resistor R614 in parallel with C604 continually discharges it so that this signal effectively disappears within about 50 milliseconds of the mains being switched off. This +15V goes to the Main Board via pin 8 of BN62, where it is used as a "pull up" signal to help control the various audio muting circuits.

AVR400 Front Panel Board Circuit Description

The Front Panel Board is a double-sided PTH PCB. It contains the VFD (Vacuum Fluorescent Display) and its associated electronics, plus the keyboard, power status LED, IR remote receiver and headphones amplifier. A daughter board carries the front panel I/O socketry. See page 1 of the schematic diagram.

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It communicates with the Input Board via CN101 and a 31 way ribbon cable. Other connectors comprise CN94 which connects to two secondaries of the main power transformer and the hard wired BN93 which connects up the daughter board.

There are two associated break off boards. One houses the front panel mounted single pole mains switch plus its suppression capacitor C901 and a connector BN502. The second is mounted on the power amplifiers' heatsink and is used to route power to the cooling fans and also to guide the 31 way ribbon cable.

The VFD draws AC filament power from a centre tapped winding of the power transformer connected to pins 1, 2, and 3 of CN94. The centre tap connects to ground via the zener diodes D901/2 and C903 to provide the filament with its required DC offset. Pins 4 and 5 connect to a relatively high voltage transformer secondary which is half wave rectified by D916 and smoothed by C907 and C960. The zener diodes D903 and D904 in series with R906 generate +40V which is then coupled to the emitter follower Q901 to provide a nominal regulated 40V HT power rail for the VFD.

The VFD's internal driver IC and external data bµFfer IC901 run from the main +5V supply generated in the Power Supply board and routed onwards through the Input Board. The drive signals (data, clock, chip select and reset) come directly from the system microprocessor via CN101.

The 12 front panel switches are arranged in 2 blocks of 6 with resistive divider chains connected to two ADC inputs on the system micro. These have 10K pull-up resistors at the system µP end to complete the potential divider chains. The pnp switching transistors Q906 and Q907 turn on the 3V3 supply from the system µP via another 10K pull-up resistor at the µP end to provide interrupt control.

The power status LED D905 is a tri-colour type. The green side indicates power on and the red side standby. A high signal on the LED net turns on Q902 and Q903. This turns off the npn Q913 to disable the red LED and turns on the pnp Q912 to enable power to the green LED. The reverse is true when the LED line is low. Pulling the STB(LED) line low when the LED line is also low powers both LEDs and gives a yellow light to show when the unit is booting up. Note that the power supply is STBY+5V to allow the red LED to operate in standby mode.

RC901 is a Kodenshi KSM603TH5B encapsulated infra red receiver for processing commands from an external IR remote control. It is designed to work with the 36-38kHz carrier frequencies associated with the Philips RC5 protocol. Note that it operates from the ST+5V rail to enable the AVR400 to be woken up. It does not demodulate the IR – this is done by the system microprocessor.

The headphones amplifier IC902 drives external headphones directly via the 330µF series capacitors C935 and C936. IC902 has a gain of about 4, meaning that the headphones output will be about 4V rms when the volume control is set to clip the L and R main power amplifiers (equivalent to about 120WPC into 8 ohms). IC902 is a JRC NJM5556AL capable of driving 7V rms into150 ohm loads and about +/-100mA peak current into lower impedances. Mute transistors Q904/905 in series with 100R resistors are fitted in front of its input to minimize switching transients and it is powered from the +/-15V supplies generated on the Power Supply Board.

The L and R headphones outputs go via BN93 to the Headphones Board, after passing through relay RL902 which is normally off. A positive voltage from the µP at the emitter of pnp Q911 turns on Q911 and generates the same positive voltage at the base of the npn transistor Q909. Because its emitter is connected to the -15V rail this pulls the relay on.

The FRONT AUX and MIC inputs come from the Headphones Board and through the microphone relay RL901. When the relay is off the AUX line level L and R signals are switched through to the unity gain bµFfer IC904 and then on to the Input Board via pins 3 and 1 of CON101. When the relay is closed (in

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the same manner as described above for RL902) then the L front input is routed to the low noise microphone amplifier IC903. This operates as two cascaded virtual earth amplifiers, each with a voltage gain of approximately 21 (R961/960 and then R965/962). Note the MIC line is biased at +6V via resistors R956, R957 and R958. The amplified signal is output to the Input Board on pin 5 of CON101.

AVR400 Input Board Circuit Description

The Input Board comprises a 4 layer PCB; this is attached directly to the back panel via its various sockets and to the heatsink by two steel brackets. It is positioned underneath the HDMI Board and above the Main Board. 5 ribbon cable sockets connect it to the other 4 boards. CN71 connects it to a daughter board containing two 9 Pin D socket connectors (an RS232 serial port and an iPod dock interface), plus two 12V trigger sockets and 2 IR receiver sockets. Note some passive components are mounted on the underside of the PCB.

The Input Board circuitry is shown on pages 2 – 5 of the schematic diagram.

Page 2 covers the analogue inputs, volume control and line level outputs.

Page 3 covers the SPDIF (digital) inputs, clock recovery, audio DSPs and the codec (stereo ADC plus 8-channel DAC).

Page 4 covers the system microprocessor and a slaved support microprocessor

Page 5 covers interfaces to the DAB/Ethernet module, and the boot loader microprocessor used to update the system SW via USB.

Analogue inputs, volume control and outputs

IC101 is a Renesas R2A15218FP analogue multiplexer and volume control, with a gain range of +42 to -95dB in 0.5dB steps. It is digitally controlled from the system microprocessor via the I2C bus on pins 49 and 50. A high logic signal on pin 51 enables the system mute. IC101 has +/- 7V supplies generated from the +/-15V rails with the regulators IC102 and IC103.

All stereo external line level inputs using phono sockets are routed to IC101 via 100R/220pF low pass CR filters. IC101 also handles the AUX-L, AUX-R and the (mono) MIC_SIGNAL setup microphone inputs coming from the front panel, plus the internal stereo outputs from AM/FM tuners (TUN-L and TUN-R) and the DAB/ethernet receiver (VENICE_L and VENICE_R). IC101 additionally switches two multichannel signals - the 8 channel direct input and the outputs from the 8 post-DAC filters. Note that the +/- 7V power supply limits the input signals to approximately 4V rms before overload occurs.

The post-DAC filters comprise 4 low noise NJM2068 dual op amps, running from the +/- 7V supplies. One op amp is assigned to each channel and performs the dual functions of converting a differential input from the DAC to a single ended output, whilst simultaneously functioning as a three pole 50kHz active filter.

The AM/FM tuner module's outputs pass through the inductors L310 and L302 (providing 19kHz notch and 38 kHz low pass filtering) and the shunt mute circuits formed by the 330R resistors R354/R369 and the two halves of Q306 plus Q307.

IC101 has a fixed level stereo output for Zone 2 (SUB_L and SUB_R) and a second one, adjustable from 0dB to -18dB in 6dB steps, for the AVR400's analogue to digital converter (ADC_L and ADC_R).

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IC101 has one 8 channel variable level output bus labelled VOL01 through to VOL08. Capacitors C295-8 and C231-4 float the ground ends of the associated internal potentiometers to minimize clicks This bus goes via specially selected 100µF/25V capacitors to the dual op amps IC121-124, wired as voltage followers and running from the +/- 15V supplies. The C, SL, SR, SBL and SBR outputs are shunt muted when required via the 560R resistors R383-388 and the dual transistors Q303-305.

The subwoofer output SW has two shunt mute circuits. One using Q311 works in parallel with the rest of the channels. The other, using Q308 and half of Q303 allows muting of the SW channel alone.

The FL and FR channels take off the stereo headphones amplifier feed from IC121 (it goes via the connector WF101 to the Front Panel Board), then add an extra dual voltage follower IC125 and a double pole shunt mute switch using 4 x 270R resistors and Q301-302. All the above ICs are JRC NJM2068s or equivalent.

All 8 of these outputs go to via the connector WF103 to the preamplifier output sockets and (except for the subwoofer output) to the 7 power amplifier inputs located on the Main Board.

The ADC input amplifiers use a JRC NJM2068 for each channel, operating as a single-ended input to differential output converter, with HF filtering above about 400kHz. This is sµFficient for anti-aliasing purposes as the analogue modulator of the ADC samples at 6.144 MHz and only needs to keep out frequencies above 6MHz.

The array of 12 switching transistors in the bottom right hand corner of the schematic is arranged in 4 blocks of 3 devices (two npn and one pnp per block). The array is used to control the muting of 4 specific groups of audio outputs, taking into account the presence of AC mains via P_U (the pull up line from the Power Supply board) and the MUTE_POWER line derived from the power amplifiers' Vcc rail – this is normally high when Vcc is high. The output lines are SB_MUTE2 (for the surround back channels SBL and SBR), ZONE2_MUTE2, HP_MUTE2 (for the headphones relay on the Front Panel board) and FUNC_MUTE2 (for the 6 main audio channels excluding SBL and SBR).

Zone 2 volume is independently adjustable in 1dB steps via IC131 (rohm BD3812F). Its outputs are bµFfered and amplified 15dB by the dual op amp IC132 and can be muted when required by Q402. The output goes directly to two phono sockets forming half of JK11 on the back panel.

SPDIF inputs, ADCs, DACs and Audio DSPs

The AVR400 has 4 coaxial 75 ohm SPDIF (Sony/Philips Digital InterFace) inputs and 2 TOSLINK optical inputs on its back panel. A further optical input is located on the front panel as part of JK92 (this socket also includes the AUX and MIC inputs). There are 6 further external SPDIF inputs - one per HDMI input socket and one on the HDMI output socket (the Audio Return Channel or ARC).

Each of the 4 coaxial inputs is bµFfered by two NOR gates, contained in IC159 and IC160, before being switched by one half of the dual 4 input multiplexer IC147. The output on pin 7 is then sent to the 8 input multiplexer IC140. Its other 6 inputs comprise the 3 optical receivers already mentioned, the HDMI input (multiplexed down from 5:1 on the HDMI board), the HDMI ARC and the output of the Venice 6 DAB/Ethernet module. The 8th input is unused. The output MUX_SPDIF is sent to the SPDIF receiver IC153.

IC153 is a Wolfson WM8804 run in hardware mode. It uses X707 to generate its own 12MHz internal clock. IC153 automatically identifies and dejitters incoming SPDIF signals with sample rates of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192kHz. Its output, still in SPDIF format, WM_SPDIF, is sent to pin 43 of the system codec IC143.

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IC143 is the Cirrus Logic CS42548. It includes an SPDIF receiver, 2 channel ADC and 8 channel DAC. Only one input (pin 43) of the SPDIF receiver is used; the others are grounded.

IC143 has +5V analogue supplies, locally decoupled to analogue ground by C721/722 for VA (pin 24) and C703/704 for VARX (pin 41). The digital supply is also +5V, decoupled to digital ground by C705/706 (pin 5) and C750/756 (pin 51). The control port power VLC (pin 6) is 3V3, decoupled to digital ground by C752/773 and the serial port power VLS (pin 53) is also +3V3, decoupled to digital ground by R726 and C753/754. The 3V3 is generated from the +5V supply by the linear regulator IC148.

The system master audio clock is generated by IC143 on pin 55 whenever an SPDIF signal is present (i.e. in all cases except when an HDMI multichannel signal in I2S is required to be processed or when using the ADC). Although IC143 has no jitter rejection below 20kHz its master clock is kept clean from incoming jitter by IC153. The PLL filter is located at pin 39. When SPDIF is not in use IC143 inputs its clock on pin 59 – this can be 24.576 MHz from the crystal oscillator X701 associated with DSP1 when ADC mode is engaged, or the recovered clock from the HDMI Board. This is switched by the 4 way change over multiplexer IC145 on pins 9, 10 and 11. IC145 also routes IC143's recovered master clock or the HDMI master clock to DSP1 on pins 5, 6 and 7.

Pins 1, 62, 63 and 64 receive the 24 bit serial audio data that has been processed by the DSPs.

The DAC's 8 analogue outputs are in differential mode, so making 16 output lines in total, from pins 20-23 and 26-37. These feed the post-DAC filters IC111-114, described above.

The main audio DSP is a Cirrus Logic CS 497024, IC141.This is a 300MIPS dual core 32 bit fixed point DSP, with 72 bit accumulators. The first core is used for decoding standard and high definition audio formats (Dolby, DTS etc) and the second is reserved for post processing such as bass management, delay and room correction. The secondary DSP, IC142, is a Cirrus Logic CS49DV8, responsible for the Dolby Volume processing. IC141 gets the 1.8V for its core from the 3-terminal regulator IC149. IC142 gets its 1.8V from IC150. The 3V3_1 and 3V3_2 supplies for these regulators are generated on the Power Supply Board.

IC141, 142 and 143 communicate with the system microprocessor via an SPI bus. For IC141 and IC142 the chip select lines are on pin 6, the clock is on pin 126, the MISO line on pin 124 and the MOSI on pin 123. For IC 143 the corresponding pins are pins 10, 7, 8 and 9. Note that the 3 chips receive data on a common line but transmit to the µP on two separate ones (DSPDATA for both DSPs and D_OUT for IC143).

IC141 communicates with its external memory via a 36 line data bus running at 150MHz. This is needed when providing lip sync delay for audio accompanied by video. IC144 is a 200MHz 16Mbit SDRAM, organized as 512Kbits x 16bits x 2. It is powered from the board's 3V3 line via 6 pins, with local decoupling provided by C758-763.

The DSPs' programs are stored in two external 3V3 SPI flash memory chips – IC106 (8Mbit) for IC141 and IC107 (4Mbit) for IC142.

IC141 has two sets of I2S data inputs. DAI (pins 23, 24, 26, 27 for data, pin 29 for the system clock and pin 30 for the LR clock) is for up to 8 channels from the HDMI Board via connector WF104.

DA2 (pins 32 for the LR clock, 33 for system clock and 34 for data) is for audio from the codec IC143. This includes bitstream SPDIF such as Dolby Digital, uncompressed two channel I2S audio decoded from SPDIF and ADC generated I2S two channel audio.

The DSP master clock is input on pin 40 of IC141 from pin 9 of IC145 as noted earlier.

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IC141 also has two sets of I2S data outputs. DA1 is an 8 channel I2S signal (pins 47, 48, 49 and 51) shown as part of the bus DA0(04:07). This feeds the input of the second DSP IC142 (on pins 23, 24, 26 and 27). The system clock is on pin 52 of IC141 and the LR clock on pin 54. These go to pins 29 and 30 of IC142.

DA2 is a stereo I2S output (pin 43 for data, pin 44 for the system clock and pin 46 for the LR clock). This feeds the HDMI board via WF104 and the octal bus switch IC146. The DSP master clock output from pin 9 of IC145 follows the same route. An SPDIF output from pin 35 of IC141 goes directly to pin 12 of WF104.

There is one set of 8 channel I2S outputs from IC142 – DA1 (pins 47, 48, 49 and 51). These form part of the data bus DA0(00:03) where they are routed back to the DACs in IC143 (pins 62, 64, 63 and1 respectively). The I2S system clock and LR clock (pins 52 and 54) also go directly to IC143 (pins 2 and 3).

System Control Microprocessors

There are 3 microprocessors on the Input Board, the main, the sub and the USB micro. The latter is also kept separate in order to perform upgrades over USB.

The AVR400's **main system microprocessor IC151** is a Toshiba T5CN5 microcontroller. This has an ARM Cortex 3 core with 512KB of ROM and 32KB of flash memory. It is a 3V3 part, with this power supply being derived from the main 5V supply via the 3-terminal regulator IC156. It has a 40MHz system clock derived from crystal X702 and a real time clock from the 32.768 kHz crystal X708.

IC152 is a 32Kbit EEPROM for retaining system settings at power down.

IC155 is a MOSFET switch to enable the HDMI CEC (Consumer Electronic Control) bus when the unit is powered up, and to isolate the parts of the bus external to the AVR400 when it is powered down.

IC151 has several sets of comms busses - SPI, I2C and UARTs - depending on which system or peripheral ICs are being addressed. SPI (Serial Peripheral Interface) is a fast 3-wire interface (clock, transmit and receive) with chip select being addressed by individual I/Os. I2C (Inter Integrated Circuit) is a relatively slow bidirectional 2-wire interface, with open-collector/source clock and transmit/receive busses, each with a pull up resistor, and a limited number of embedded chip addresses. UART stands for Universal Asynchronous Receiver/Transmitter and is a form of bus that takes bytes of information and turns them into serial data on a bus before reassembling them into bytes at the other end.

SPI is used to talk to the codec IC143 and the two DSPs IC141 and IC142.

I2C is used for both the main and zone 2 volume controls IC101 and IC131. I2C also connects to the sub micro IC154 and to the NJW1321 video input decoders IC81 and IC81.

IC151's UARTs are used for USB Tx/Rx, the Torino (video processor) Tx/Rx and the external RS232 Tx/Rx.

Further UARTs on the **sub micro IC154** communicate with the Venice 6.2 DAB/Ethernet receiver and the iPod external interface. IC154 is a Toshiba M333FWFG ARM Cortex 3 microcontroller with 128K ROM and 8K of flash, effectively used as a helper for IC151. Its 3V3 power supply regulator IC158 runs from the board's main 5V supply.

The **USB micro ("Bolero")** IC162 is a Toshiba TMP92FD28FG, a 32-bit CISC microcontroller with a built-in USB2 host controller capable of supporting 12Mbps. Its primary function is to provide a "bullet-proof" system updating process via an external USB stick. When the AVR400 is powered up IC162 first self boots, then interrogates the rest of the system – if it receives the wrong response (e.g. if a previous update failed part way through) then the unit will appear dead. However IC162 will be constantly inter-

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rogating the USB socket and insertion of a clean USB stick containing only the system firmware will initiate a complete recovery automatically.

IC164 is a MiniLogic ML61C282PR precision voltage detector, with a threshold of 2.8V, built in hysteresis and a CMOS output, used to reset IC162 at power on.

IC163 is an Intersil USB switch, type ISL54220, which routes the USB socket on the rear panel either to the Venice 6.2 module, for normal audio applications, or to IC162 when the system SW is being upgraded from a USB stick. Note that it is positioned underneath the Venice 6.2 module, close to the USB socket.

The USB high side power switch IC168 is close to IC163. It is a Richtek RT9702A fed from the main +5V power supply. It is rated at 1.1 amps output and can flag up a fault condition on the USB bus from pin 3; this is routed to IC162.

The **Frontier Silicon Venice 6.2WB module** is plugged into the input board via a 64 way connector CN62. This WB version of the module supports Band 3 DAB/DAB+ digital radio for use in Europe, Australia, Canada, Korea and other Digital Radio markets. It also supports USB2, and Ethernet up to 100 Mb/s, enabling the AVR400 to be a network audio client. A spare copy of the AVR400's unique MAC (Media Access Controller) address can be found on the screening can of the Venice 6.2 module. Its FM radio function is not used.

The Venice 6.2 is operated in slave mode via the UART pins 9 and 10 on CN62. These connect to the sub micro IC154. The USB I/O signal pins are 11 and 12, routed to the USB switch IC163. The other USB pins are not used. Pins 26, 27, 28 and 29 make up an SPI bus to work with the Ethernet PHY IC161 (pin 33 receives interrupts from IC161).

Audio is decoded inside the Venice 6 (i.e. from AAC, FLAC, MP3, WMA or WAV) and sent out by two routes. Pin 32 carries an SPDIF signal (at 48ks/s) for the main system and pins 64 and 63 carry L/R linear audio for zone 2 to the volume control IC101.

The Venice 6.2 requires +3V3 at up to 300mA average and +1V2 at 200mA average for the core of its main processor. 3V3 is provided from the main +5V supply via the three terminal regulator IC165 – this also provides the soft start signal to pin 2 of the 1V2 regulator IC167 (also fed from +5V with some voltage drop provided by diodes D803/4). Both regulators are SM types, positioned underneath the Venice 6.2 module.

IC161 is a Micrel KSZ8851 single port Fast Ethernet MAC/PHY controller with an SPI interface. It has a 12KB receive bµFfer and a 6KB transmit bµFfer. It has its own 25MHz crystal oscillator X777. Its 4 I/Osgo to the Ethernet socket JK52 on the back panel. Its +3V3 power rail is derived from the board's +5V supply via the three terminal regulator IC166.

AVR400 RS232 board

This is a daughter board connected to the Input Board via an 18 way plug and socket BN71. The circuitry is shown on page 14 of the schematic diagram.

It contains two 9 way D-type board mounted plugs JK71 and JK72. JK71 is for RS232 control of the AVR400. JK72 is used to control an iPod or iPhone via an Arcam rDock or rLead (the latter also supports iPads).

The RS232 dual transmitter and receiver IC73 is an ST3232 run from the standby +5V supply via D721/R727 and a series pnp transistor Q722 in common emitter mode referred to the +12V rail. Q721 provides

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the necessary level shifting. IC73 includes internal charge pumps to convert CMOS logic level inputs to +/-5V RS232 level outputs and +/-25V tolerant RS232 inputs to CMOS logic level outputs. Maximum rated speed is 300kb/sec.

JK73 is a dual mono 3.5mm jack socket providing two +12V trigger outputs Z_1 and Z_2. The series pass transistors Q712/715 are pnp T0-92 types with emitters referred to the +12V rail via the paralleled 4.7R resistors R714/715 and R711/712. In conjunction with the pairs of diodes D711/712 and D714/715 this provides current limiting at approximately 200mA if the trigger outputs are inadvertently shorted to ground.

JK72 is a dual 3.5mm mono jack socket providing inputs for two modulated infra-red remote control signals. These are connected to the opto-isolators IC72 and IC71. Note the use of the standby power supply ST+5V for the subsequent logic.

AVR400 HDMI Input/Output Board

The HDMI Board is described on pages 6 – 10 of the schematics diagrams. Note that it has components fitted to both sides of the PCB. HDMI stands for High Definition Multimedia Interface. The AVR400's system supports certain parts of the HDMI 1.4a specification (3D video compatibility and Audio Return Channel)

The HDMI Board has 5 type A HDMI input sockets and one type A HDMI output socket, which are flush with the back panel. It gets its power via the hard wired connector and ribbon cable CN61 and communicates with the Input Board via two flex foil cables attached to connectors CN104 (17 ways) and CN105 (19 ways). It is fitted with a 30 way socket BN301 which attaches to a daughter board handling all analogue video I/O signals (the Analogue Video Board).

The HDMI Board contains 10 separately regulated local power supplies, mostly derived from the unregulated but hum filtered +15V supply on the Power Supply Board. This is input on pins 3 and 4 of the hard wired connector CN61 for +15V and pins 5, 6 and 7 for the ground returns. Pins 1 and 2 are not used. See page 10 of the schematic diagram for all but the last of these supplies, as described below.

IC923, IC927 and IC930 are all Sanken SI-8005Q 3.5 Amps step-down switching regulators operating at 500kHz +/-10% and drawing power from the +15V line. They are used to generate +3.3VDD, +1.8VDD and +1.8VH1 (video processor supply) respectively. The potential dividers in their outputs (R839+R844/R847, R838+852/R851 and R841+843/840) are used to set the required voltages.

All other local power supplies use linear SM 3-terminal regulators.

IC922 and IC929 provide +2.5VH1 and +2.5VH2 for the two DDR memory chips supporting the video processor. The source supply is +3.3VDD.

IC925 is a KIA7809 generating +8VA from the system's +15VA line (NOT the unregulated +15V used elsewhere on the board). This is further dropped to +5VA by IC924, a KIA1117S50. Inductor L860 provides decoupling for the +5VH1 line. The video processor digital power supply lines +3.3VH1, +3.3VH2 and +1.8VH2 are sourced from the +3.3VDD and +1.8VDD lines via L-C decoupling.

The video ADC's analogue supplies, +3.3VA and +1.8VA, are generated from the +5VA line via IC926 (NJM2845DL133) and IC928 (NJM2845L118) respectively.

The 10th regulator, IC917, an NJU7754 found on sheet 9 of the schematic, is used to provide +5V to the HDMI output socket. It is enabled via SW_P+5V and derives its input from the +8VA supply described abov

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The HDMI input SOC, IC901, is a 144 pin LQFP Analog Devices ADV3014B. This is a 4 into 1 HDMI 1.4a multiplexer and is connected to inputs 4 and 5 (VCR and PVR) on the rear panel (JK95 and JK96). The other two inputs on IC901 are not used. The core power supply is +1.8V and the receiver terminator supply voltage is +3.3V. Note that most power supply decoupling components are on the underside of the PCB. +5V detect and hot plug assert control is carried out by the complementary pairs of switching transistors Q904/907 and Q910/909. The video system clock is provided by a 28.63636MHz crystal X901 connected across pins 101 and 102.

Pin 63 is set low by R602 meaning IC 901 is controlled by I2C at 3.3V via pins 78 (HDMI_SDA) and 79 (HDMI_SCL) from IC902. The HDMI output from IC901 is sent to input A of IC902.

IC902 is an Analog Devices ADV7844, packaged in a 425 pin BGA. It has a 4-input HDMI 1.3 receiver and one video input supporting standard analogue video formats, from 525/625i up to 1080p, with 12-bit ADCs. Its primary function is to prepare these signals for the main video processor IC906. Its second function is to extract digital audio from the HDMI signals, including the reconstruction of a good quality master clock, and to output all this in I2S or SPDIF format to the DSPs on the Input Board.

JK92 (AV), JK93 (SAT) and JK 94 (BD) connect to 3 of IC902's HDMI input ports. Hot plug detect on these 3 inputs is carried out by the complementary pairs of switching transistors Q905/906, Q908/901 and Q902/903. The 4th input receives the output of the HDMI switch IC 901. The core power supply is +1.8VH2 and the receiver terminator supply voltage is +3.3VH2, with heavy local L-C decoupling. Note that most of these power supply decoupling components are on the underside of the PCB. The video system clock is provided by a 28.63636MHz crystal X902.

IC902 has a 256Mb SDRAM IC904 connected via 9 x 4-way 33 ohm resistor packs. This is used as a line/frame store for digitizing the analogue video signals (CVBS, S-Video and Y, Cr, Cb) received from the external video inputs and also separate i-Pod derived analogue video signals. It runs from the +2.5VH2 supply with further local decoupling components mounted on both sides of the PCB.

The 12-bit RGB video outputs are sent via 10 x 33ohm resistor packs to the tri-state bμFfers IC911 and IC912. A 10-bit subset of these is also sent to the video processor IC906. Note that the critical video clock is expanded to drive two output lines HD_VCLK1 (for IC906) and HD_VCLK2 (for IC911) via IC905 and 3 x 33ohm resistors.

The extracted digital audio outputs are sent as I2S and SPDIF signals to the audio DSPs on the input board via 2 x 33 ohm resistor packs and the switch IC903. IC903 is enabled via Q913.

The video processor IC906 is an ST (formerly Genesis) "Torino" type FLI30336AC in a large 416 pin BGA package. It is used to de-interlace and scale all the AVR400's video inputs to the required output resolution(s) up to 1080p and also to generate the system OSD (on screen display). Note that IC906's analogue video inputs are not used in this application and are either grounded via an array of resistors and coupling capacitors close to one long edge of the heatsink or left open (R879-882 are no fits).

IC906 dissipates considerable power (about 4 watts) and is thus equipped with a heatsink soldered to the PCB via two pins. Its core voltage is +1.8VH1, with +2.5V_DDR being used for its RAM bus and +3.3VH1 for I/O and 19.66MHz crystal clock X903, all followed by copious local L-C decoupling. Note that the decoupling capacitors and series inductors required are mounted on the underside of the PCB.

IC906 supports two 256Mbit DDR-1 500MHz 2.5V SDRAMs (IC908 and IC909) via a mix of 33R and 0R series resistors in the data busses. On the other side of IC906 is its 32Mbit 3.3V flash memory IC907 (Macronix MX29LV320). IC931 is an Atmel AT24C64C 64K EEPROM with +3.3VH1 power.

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Q914 and Q915 (on the underside of the PCB) send BYPASS_ON and BYPASS_OFF logic signals from IC906 to the array of 4 x 20-bit non-inverting line driver/bμFfers with tri-statable outputs, IC911/912 and IC915/916. These are arranged as a 40 way 2-in, 1-out fast switch to bypass IC906 when required (e.g. if 3D video is present). The video is in 12-bit RGB format and 4 more bμFfers are required for the video clock, H and V syncs and the DE (data enable) line, thus using up all of the available 40 ways. See sheet 9 of the schematic diagram. Power is provided via local L-C decoupling from +3.3VH2.

The HDMI output is handled by IC918, an Analog Devices ADV7511 in a 100 pin LQFP package. It is a 225MHz output part that can handle 12-bit 1080p video (up to 165MHz clock speed) and embedded HD audio. It is compatible with certain parts of the HDMI 1.4 specification, supporting 3D video and an ARC (audio return channel).

As with the other Analog Devices parts IC918 uses two power rails, namely +1.8VH2 and +3.3VH2. The necessary decoupling capacitors are mounted on the underside of the PCB.

In the AVR400's implementation the HDMI audio output is limited to stereo rather then 8 channels – via I2S0 (pin 12), plus MCLK (pin 11), SCLK (pin16) and LRCLK (pin 17). SPDIF from the AVR400 is input to pin 10.

The ARC signal, if received from a downstream sink such as a TV, is output from pin 46 of IC918 and sent via back to the input board. Note that IC921 is not fitted.

The HDMI output is via JK97, a type A HDMI socket. As the AVR400's output is partly HDMI 1.4 compliant, pin 14 now becomes the HEAC+ and pin 19 HEAC- as well as HPD (Hot Plug Detect). However, because the Ethernet part of the HDMI1.4 specification is not supported by the AVR400, the ARC is configured by the sink to be carried in single (i.e. non-differential) mode using HEAC+ as the signal line. HEAC+ and HEAC- are then AC coupled to pins 52 and 51 of IC918 via the 1μF series capacitors C439 and C428. R771, R777, R785, R795 and R799 bias the inputs and load the cable correctly.*(Note – HEAC is short for HDMI Ethernet and Audio (return) Channel).*

Q916 is a twin n-channel MOSFET which only turns on when +5VH1 is present. This isolates the DDC clock and data lines when the AVR400 is turned off.

IC917 is a low dropout voltage regulator feeding +5V power to pin 18 of JK97 from the +8VA supply, when enabled by the SW_P+5V line.

Analogue video output of digitized and processed 10-bit video from IC906 is available from the AVR400 via the video encoder IC919 – an Analogue Devices ADV7342B. Composite, s-video and component video are supported, although only component analogue video is output by the AVR400.

IC919 is in a 64 pin LQFP powered from the +18VA and +3.3VA lines. Once again most decoupling components are on the underside of the PCB.

The 6 x 11-bit video DACs inside IC919 are each loaded with 300R to ground before being AC coupled to IC913. This is a JRC NJM2566 6-channel video amplifier for SD and HD signals, powered from the +5VA line. The FS_SEL signal on pin 17 sets the bandwidth on component video to 13.5MHz or 30MHz, to suit progressive SD or HD signals respectively. The composite and s-video bandwidths are fixed at 6.75MHz. The outputs go to the analogue video daughter board via the 30 way socket BN301.

Note that the composite and s-video outputs are not actually used in the AVR400 so are not wired beyond CN301 on the daughter board. The Y, Cr, Cb component video outputs are terminated with 75 ohm series resistors on the Analogue Video daughter board described next.

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AVR400 Analogue Video Board

This is connected into the rest of the system via the HDMI board using CN301.The circuitry is shown on sheet 13 of the schematic diagram.

The purposes of this PCB are:

(1) to switch between the various analogue video inputs (comprising 4 each composite and s-video and 3 component video)

(2) to route the chosen video signal to the HDMI board for processing

(3) to provide one set of zone 1 video component video outputs

(4) to provide one zone 2 video output (composite video, with its own OSD) from any of the 4 composite video signal inputs.

The PCBs power supplies are +9VV and +5VV, generated from the three-terminal regulators IC88 and IC89 from the system's +15VA supply on pin 1 of CN301. Pin 2 carries the system's -15VA supply – this is unused on this PCB.

Note that all video inputs are terminated with 75ohm resistors to ground close to the actual sockets.

IC81 is a JRC NJW1321 – a wide bandwidth video switch with 4 inputs, 2 outputs and a 6dB amplifier. It is used to select between the 4 composite and 4 s-video inputs routed to the HDMI board and also to output any one of the 4 composite video inputs to the On-Screen Display Controller IC83. IC81 runs from the +9VV supply, consuming about 85mA so it gets quite hot. It is controlled by i2C commands on pins 15 and 16.

IC82 is also an NJW1321. It selects between the 3 component video inputs and its fourth input is unused. Its Y, Cr, Cb outputs and the Y, C and CVBS outputs of IC81 are then AC coupled to IC84 – an NJM2566 6 way video amplifier/filter with 6dB gain, powered from the +5VV rail. Its outputs are also AC coupled and terminated with 75 ohm series resistors before being routed to CN301.

IC86 is a hex inverter used to bµFfer the 3V3 logic level OSD control signals from the HDMI board and convert them to 5V level for IC83. This is a Sanyo LC74763 in a 30 pin SM package running from the +5VV rail. It has two crystal oscillators X801 (17.734MHz) and X802 (14.318MHz) to provide composite video outputs for both PAL and NTSC standards.

IC86's video input signal is AC coupled to and bµFfered by the emitter follower Q802 before pin 18. Similarly its output signal (which now includes an OSD) is bµFfered by the pnp transistor Q801 and AC coupled to the video amplifier/switch IC85 (NJM2244), used here purely as a composite video amplifier/filter with 6dB gain. Its AC coupled output to the Z 2 OUT single phono socket JK85 is terminated with a 68 ohms series resistor.

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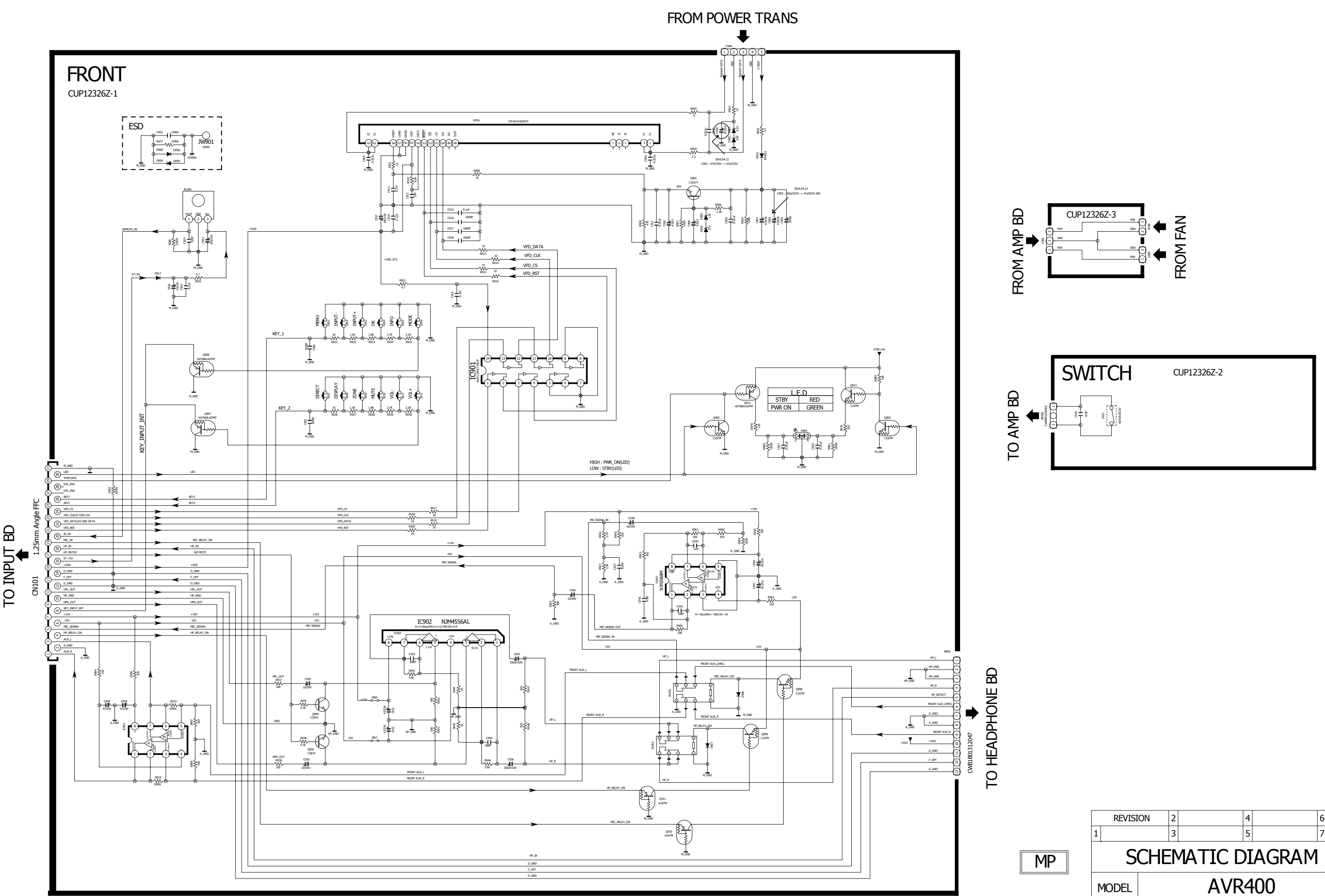

REVISION	2	4	6
1	3	5	7

MP

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR400			1 / 15
DESIGN	CHECK	APPROVE	DRAWING NO	
J.I.H	L.J.H	S.H.S	2326SCMZ (FRONT)	1 / 1
10.11.17	10.11.17	10.11.17		

ARCAM

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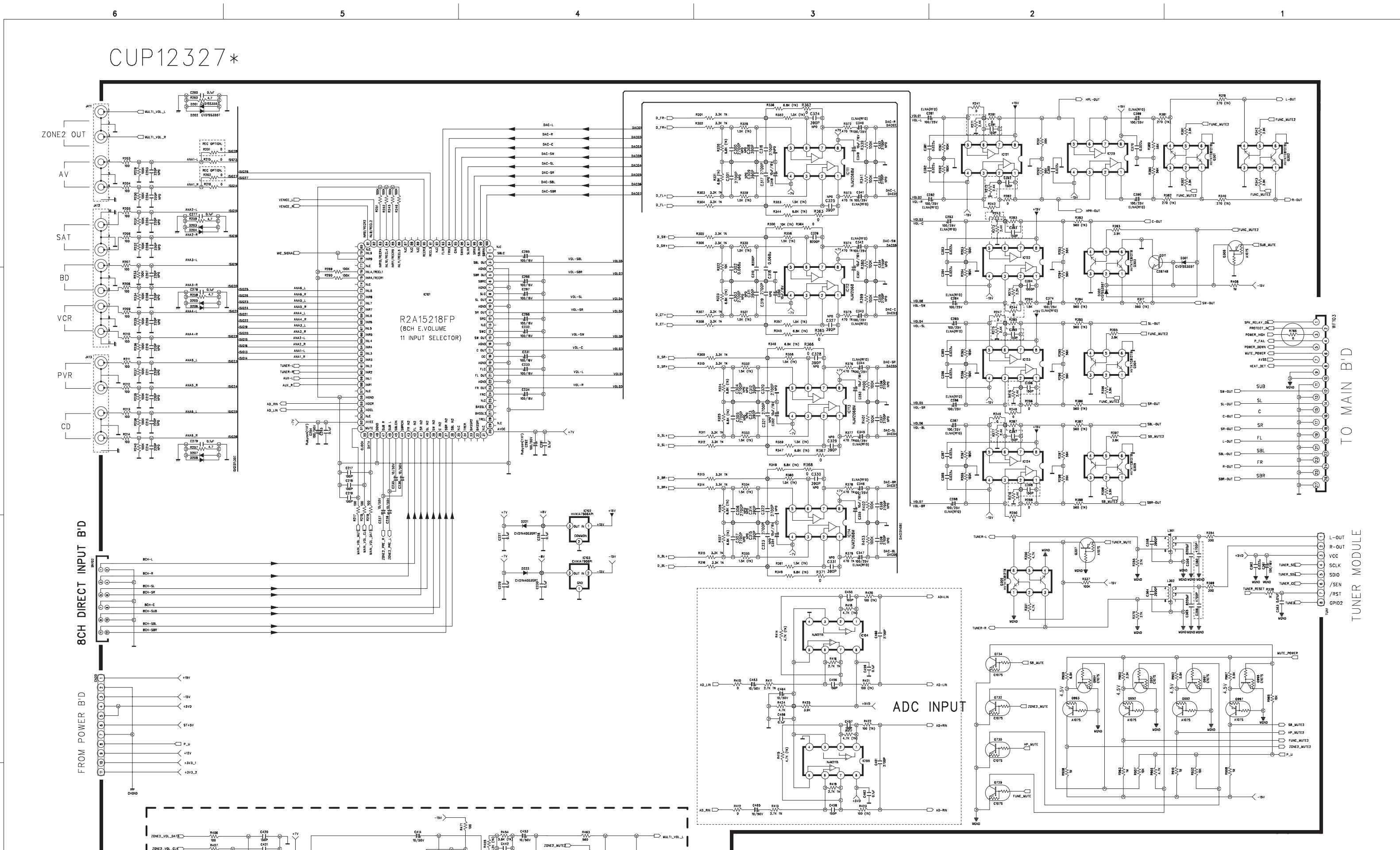

ARCAM

** IMPORTANT SAFETY NOTICES.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
$pF=10^{-6}$ uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE IMPROVEMENT OF PERFORMANCE.

M/P

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR400			2/15
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.LEE	L.J.H	S.H.S	2327SCMZ (INPUT)	1/4
2010.12.09	2010.12.09	2010.12.09		

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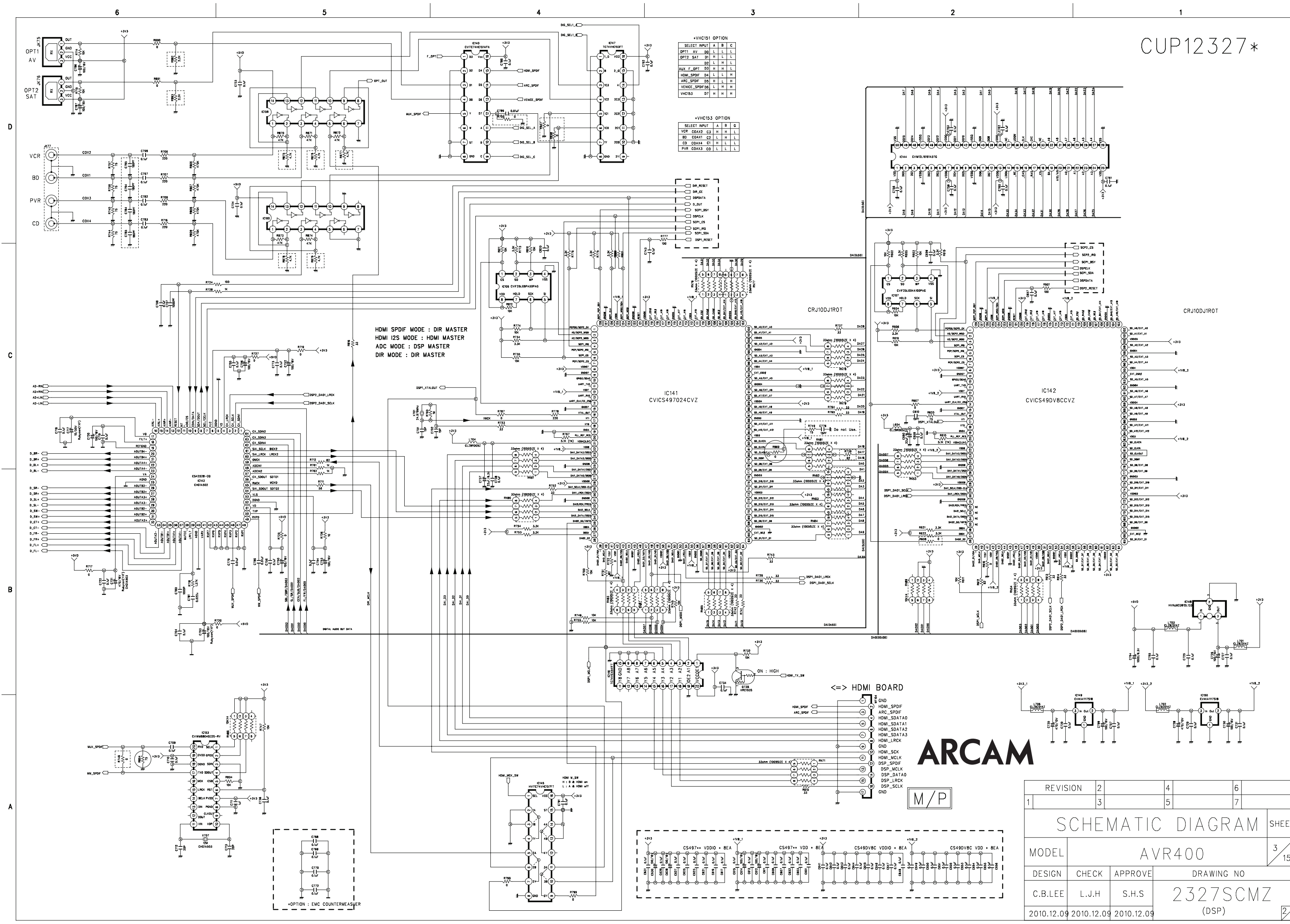

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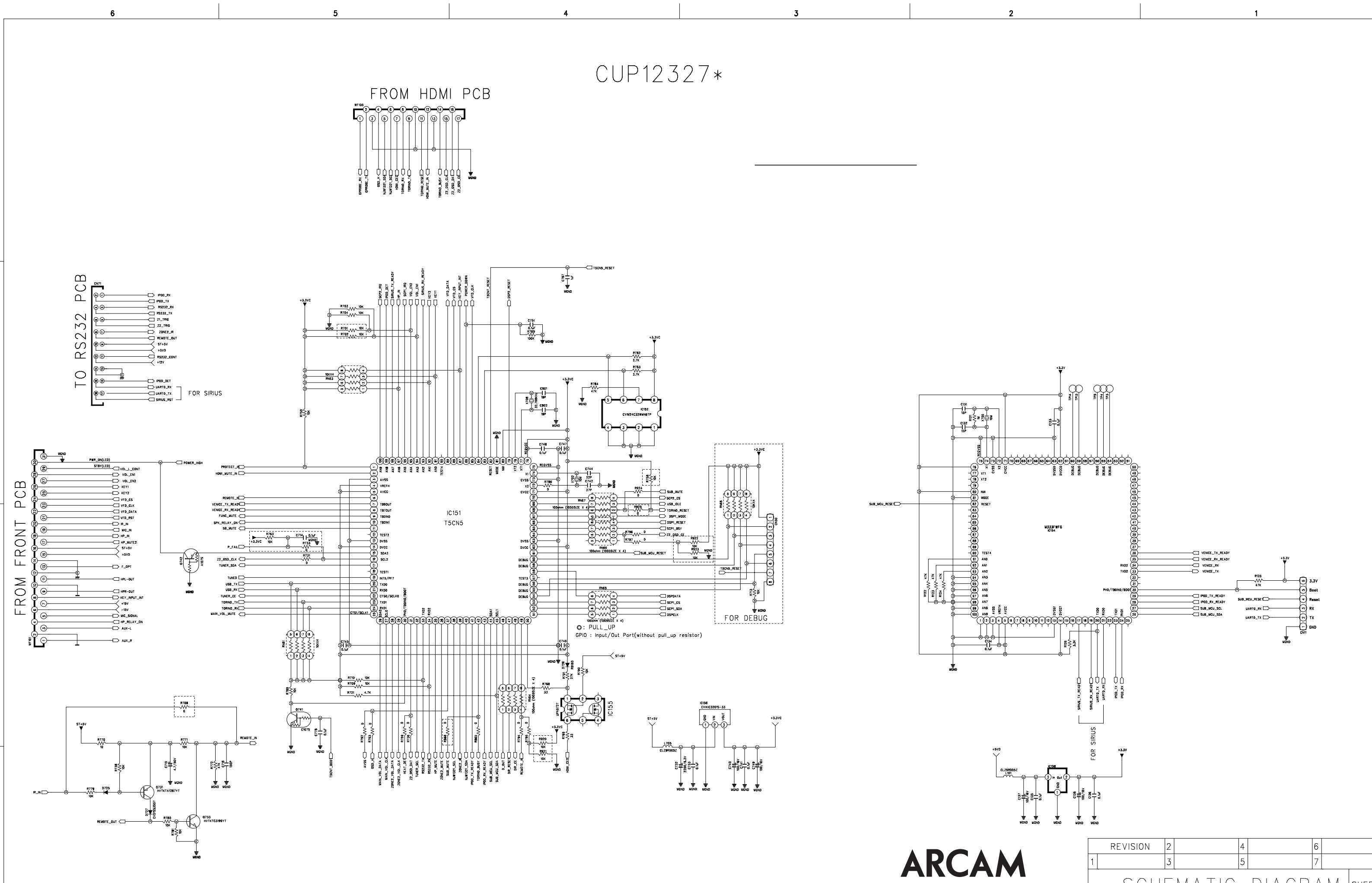

ARCAM

M/P

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET 4/15
MODEL	AVR400		
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	L.J.H	S.H.S	2327SCMZ (CPU)
2010.12.09	2010.12.09	2010.12.09	3/4

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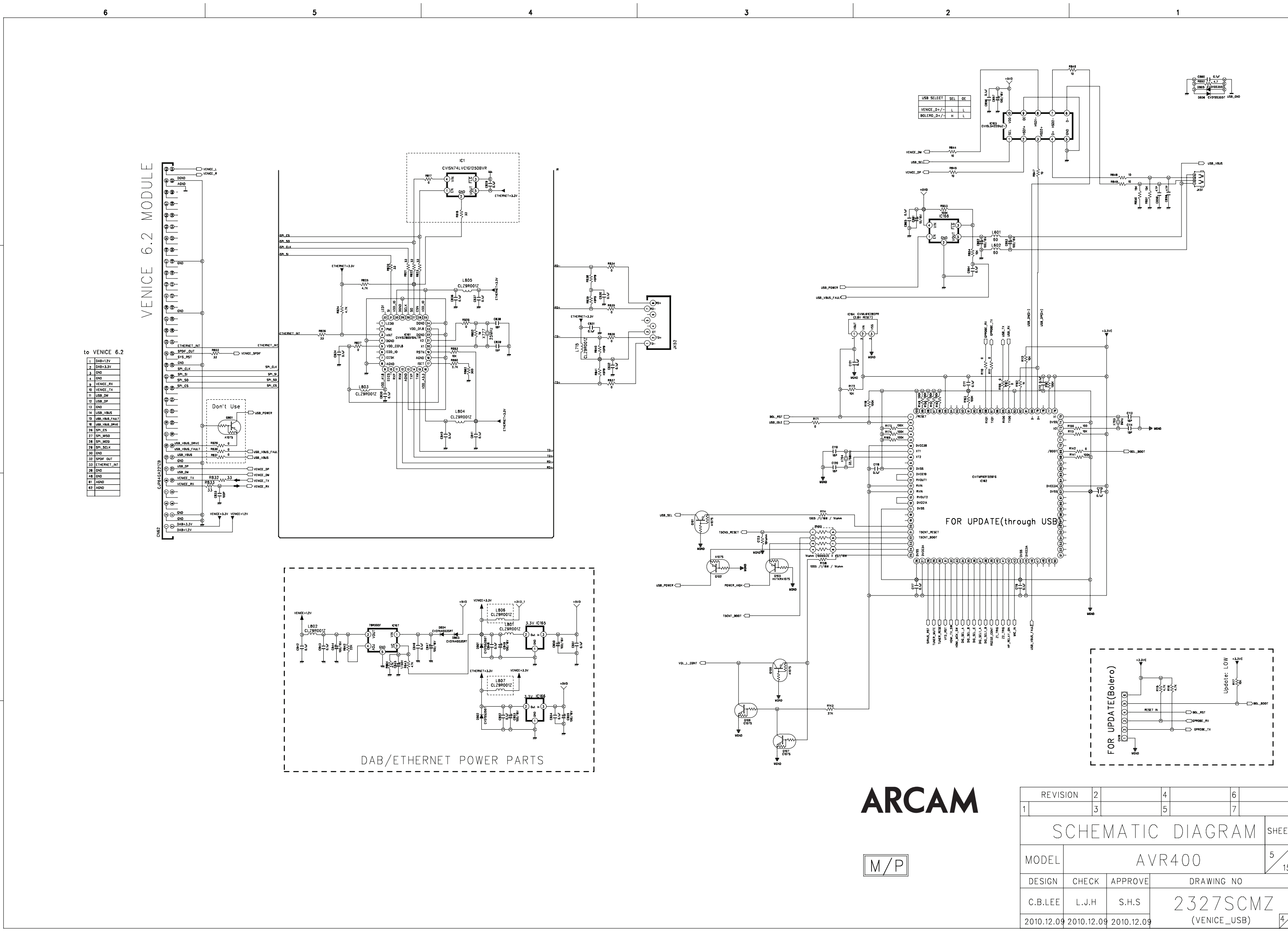

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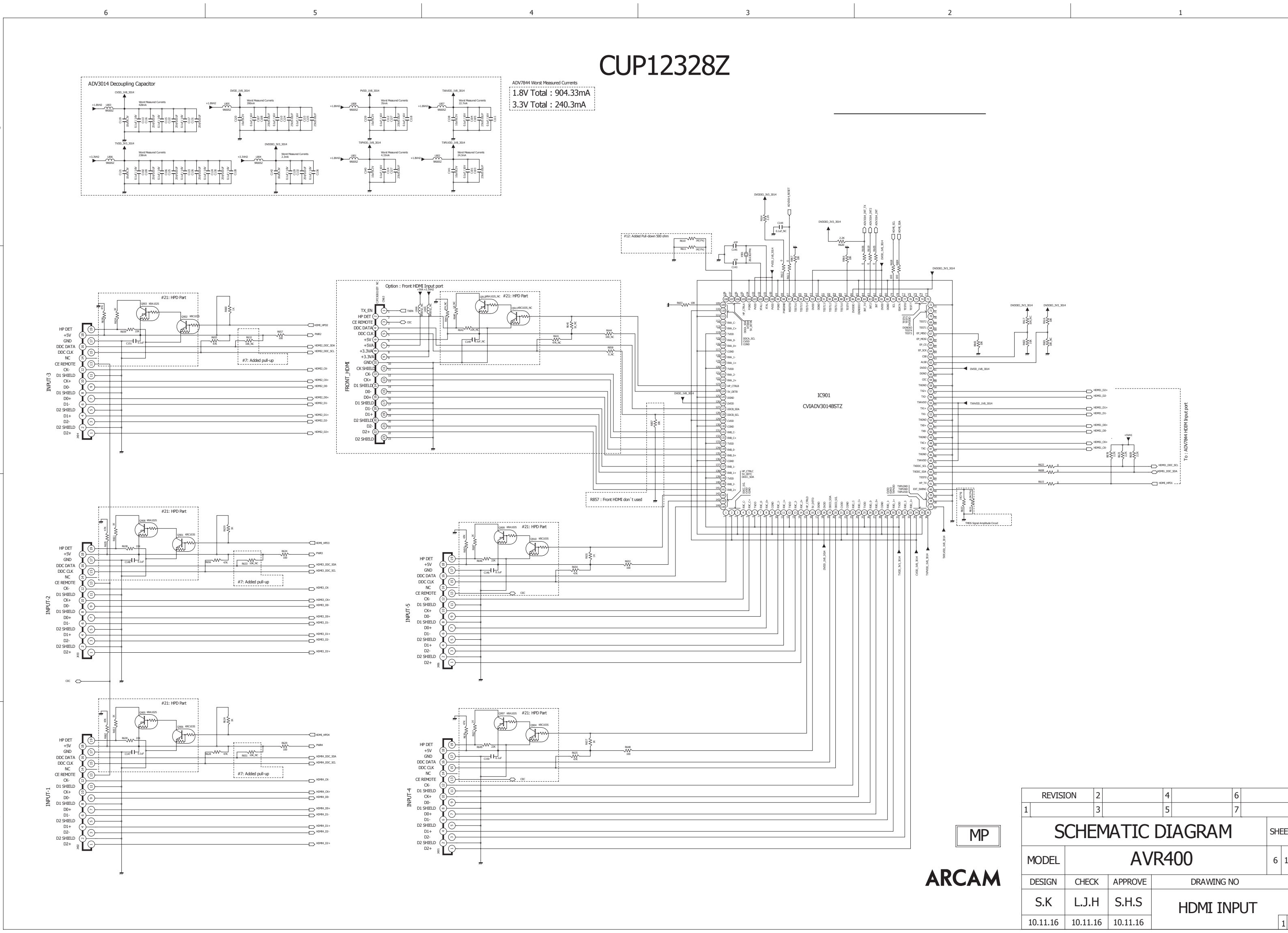

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR400		6 15
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	L.J.H	S.H.S	HDMI INPUT
10.11.16	10.11.16	10.11.16	1 5

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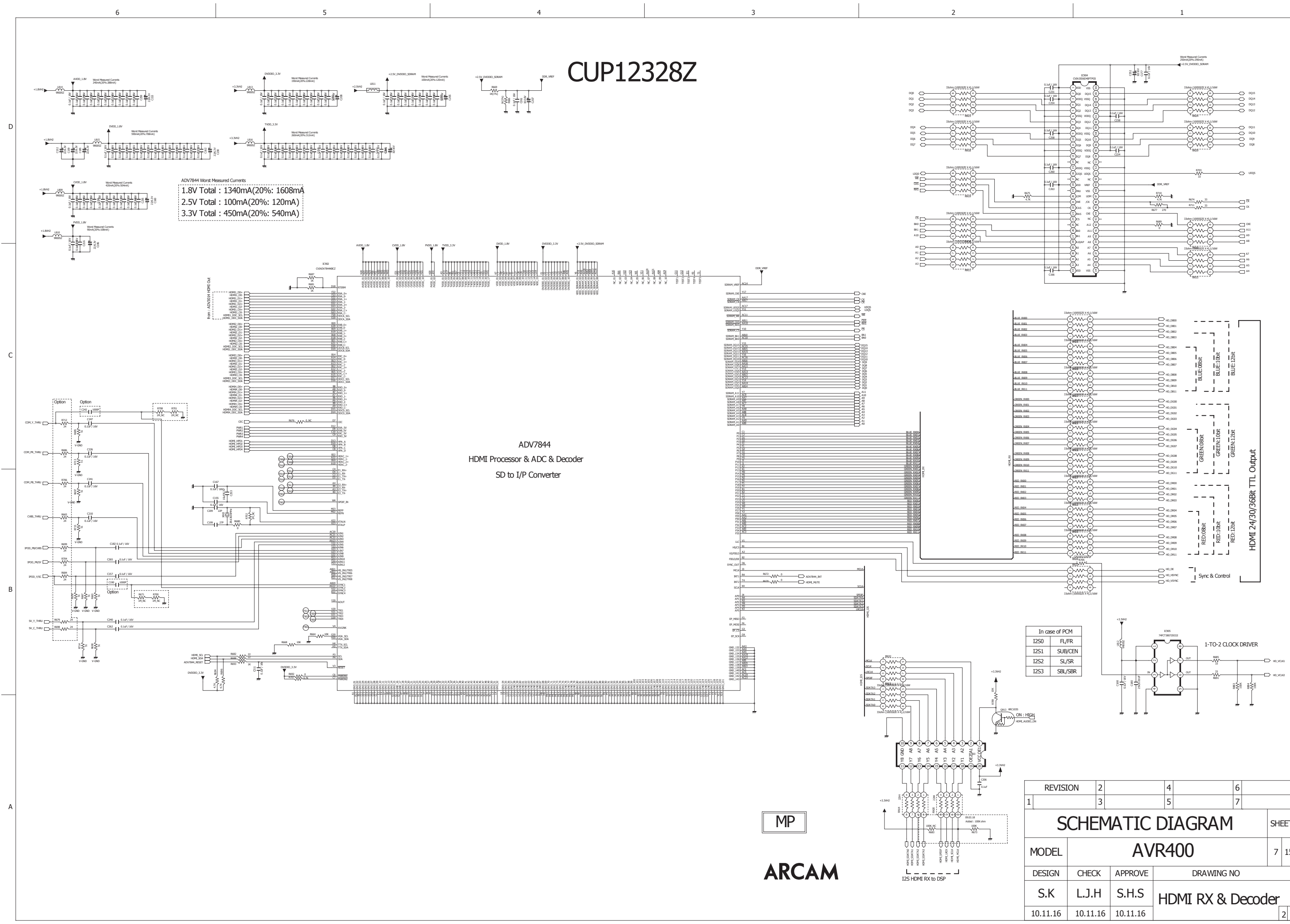

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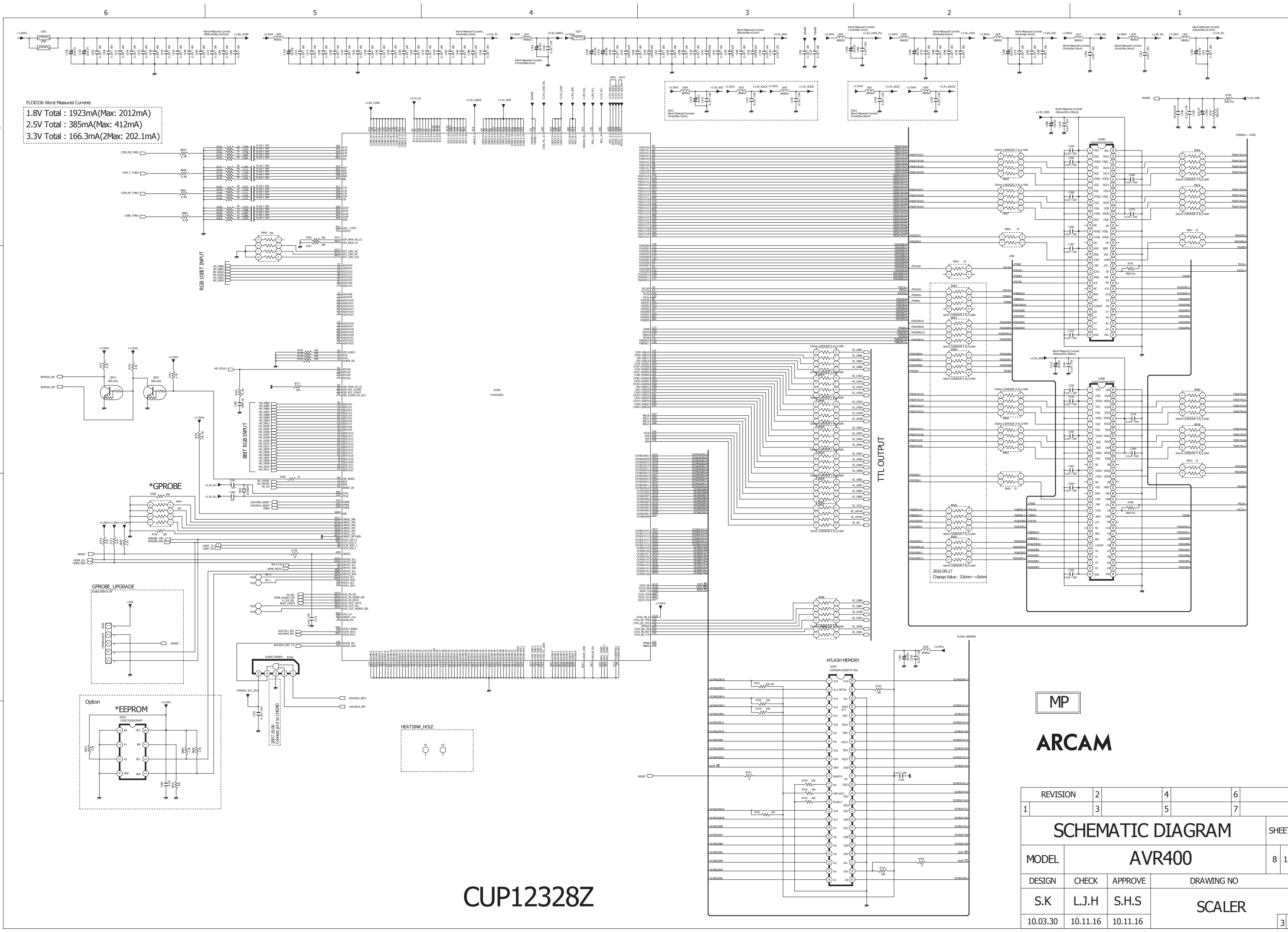

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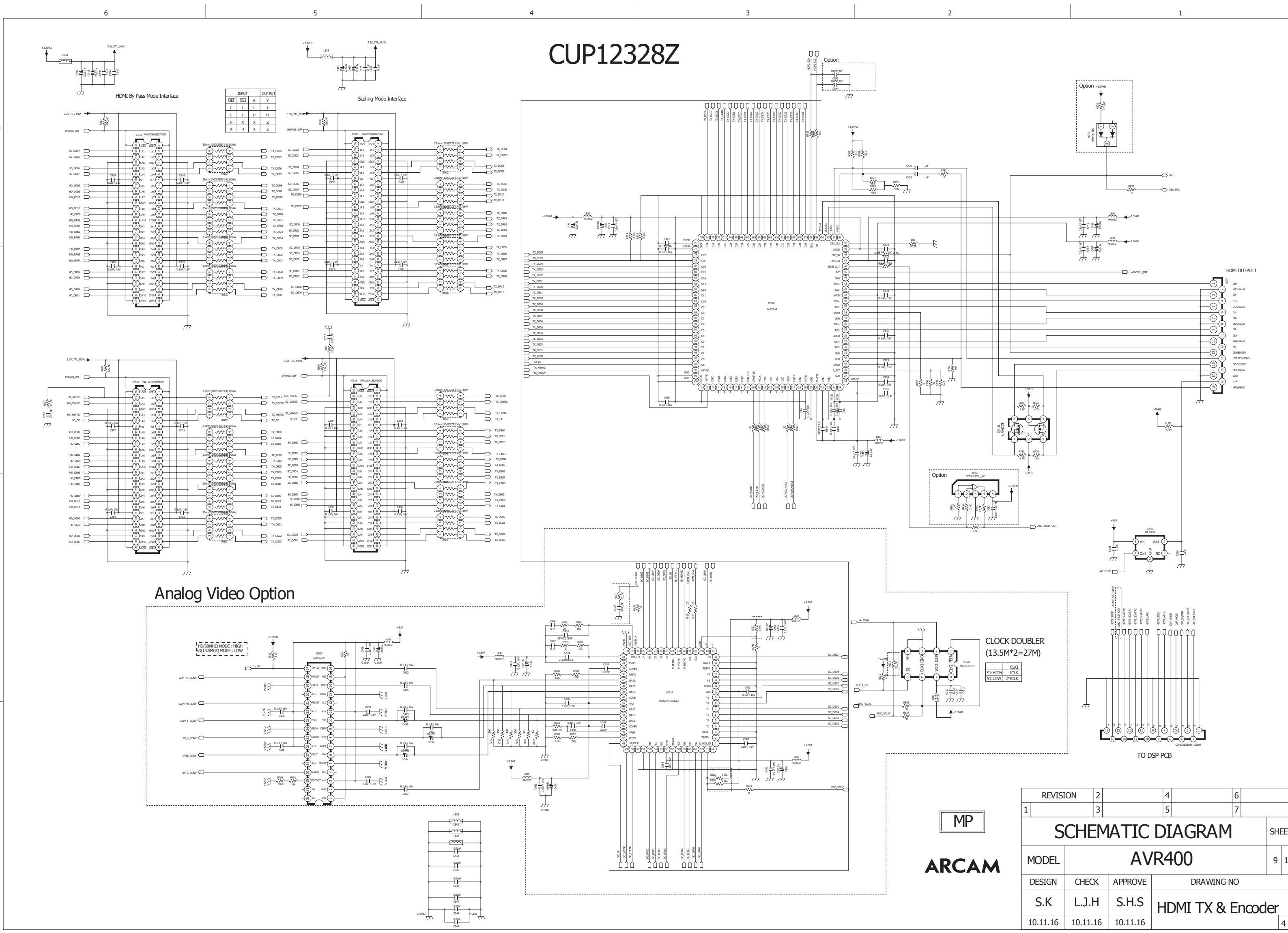

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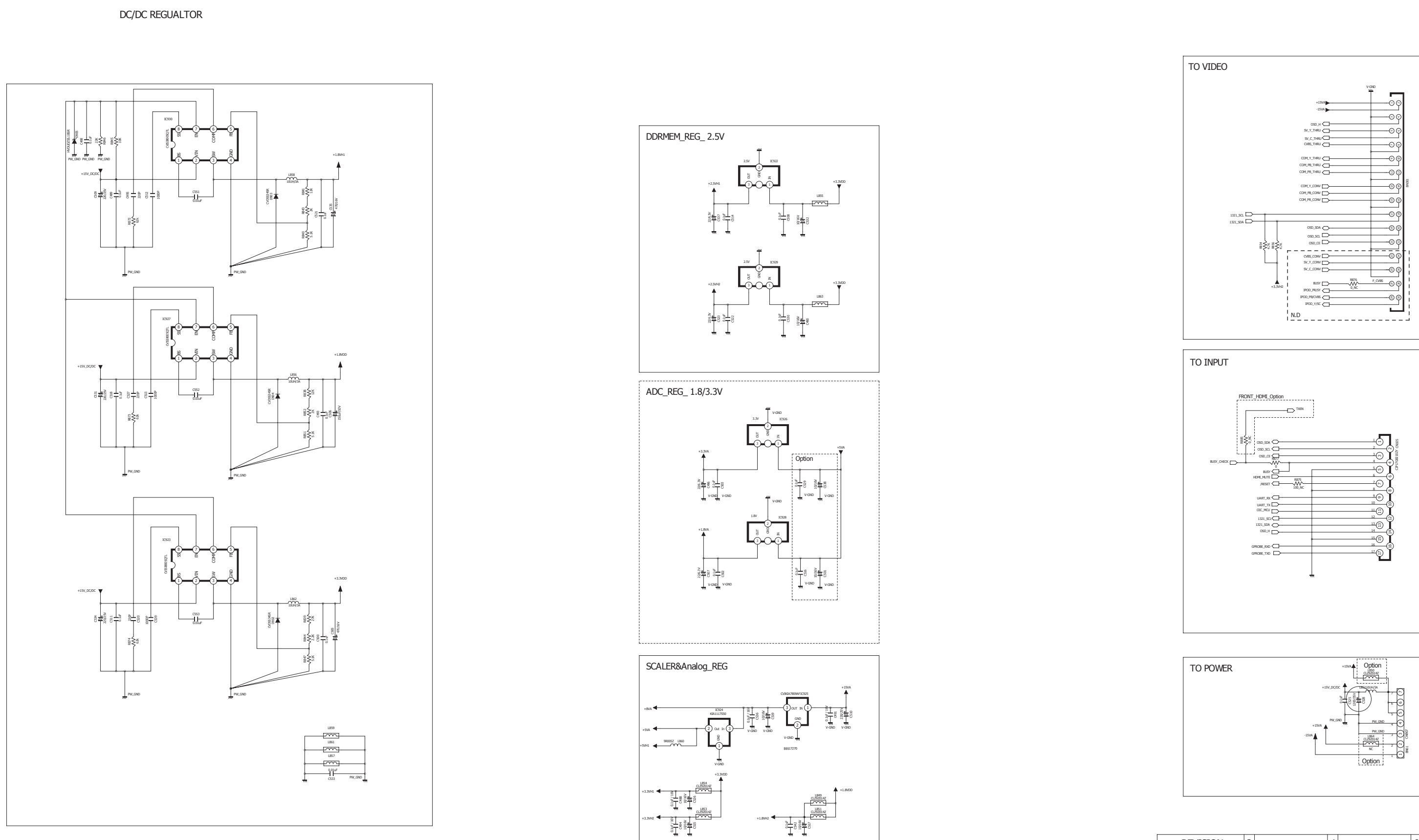
CUP12328Z



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REVISION	2		4		6	
1	3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR400		10 15
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	L.J.H	S.H.S	POWER&CONNECTOR
10.11.16	10.11.16	10.11.16	5 5

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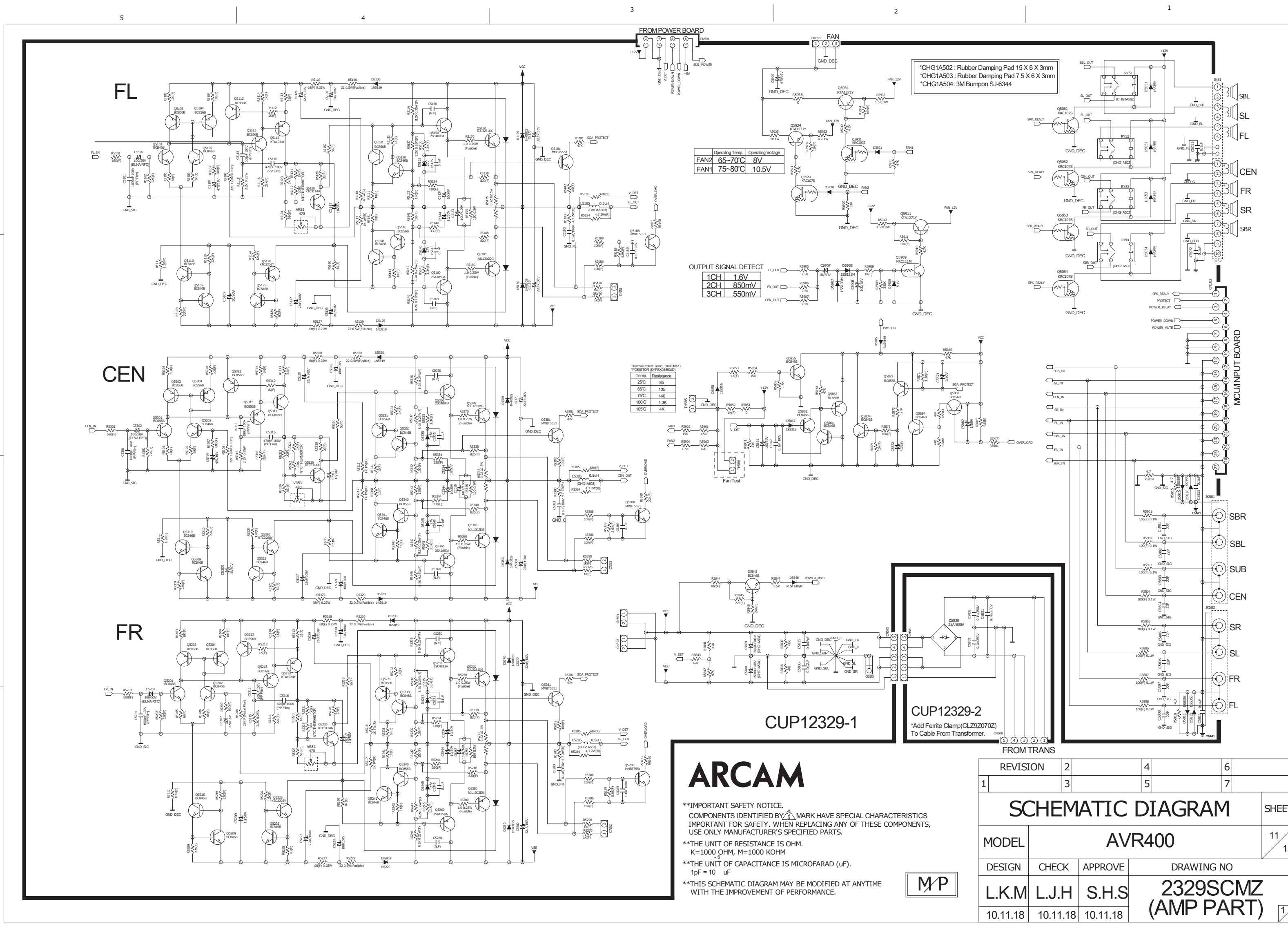

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**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY MANUFACTURER'S SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF).
1pF = 10⁻⁶ uF

**THIS SCHEMATIC DIAGRAM MAY BE MODIFIED AT ANYTIME WITH THE IMPROVEMENT OF PERFORMANCE.

M/P

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 11/15

MODEL	AVR400		
DESIGN	CHECK	APPROVE	DRAWING NO
L.K.M	L.J.H	S.H.S	2329SCMZ (AMP PART) 1/2
10.11.18	10.11.18	10.11.18	

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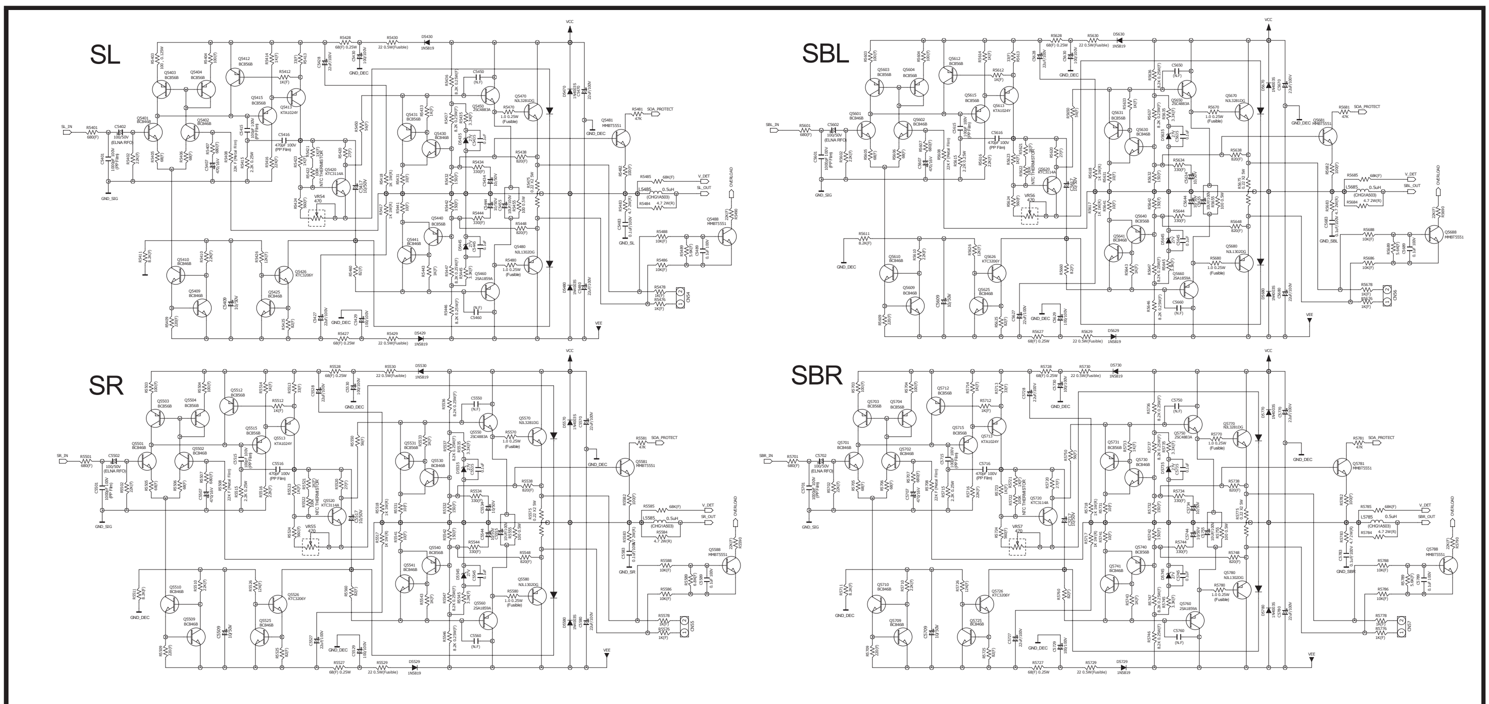

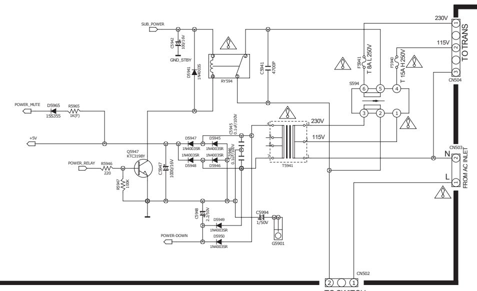

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COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY MANUFACTURER'S SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF).
1pF = 10^{-6} uF

**THIS SCHEMATIC DIAGRAM MAY BE MODIFIED AT ANYTIME WITH THE IMPROVEMENT OF PERFORMANCE.

M/P

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR400		12/15
DESIGN	CHECK	APPROVE	DRAWING NO
L.K.M	L.J.H	S.H.S	2329SCMZ
10.11.18	10.11.18	10.11.18	(AMP PART) 2/2

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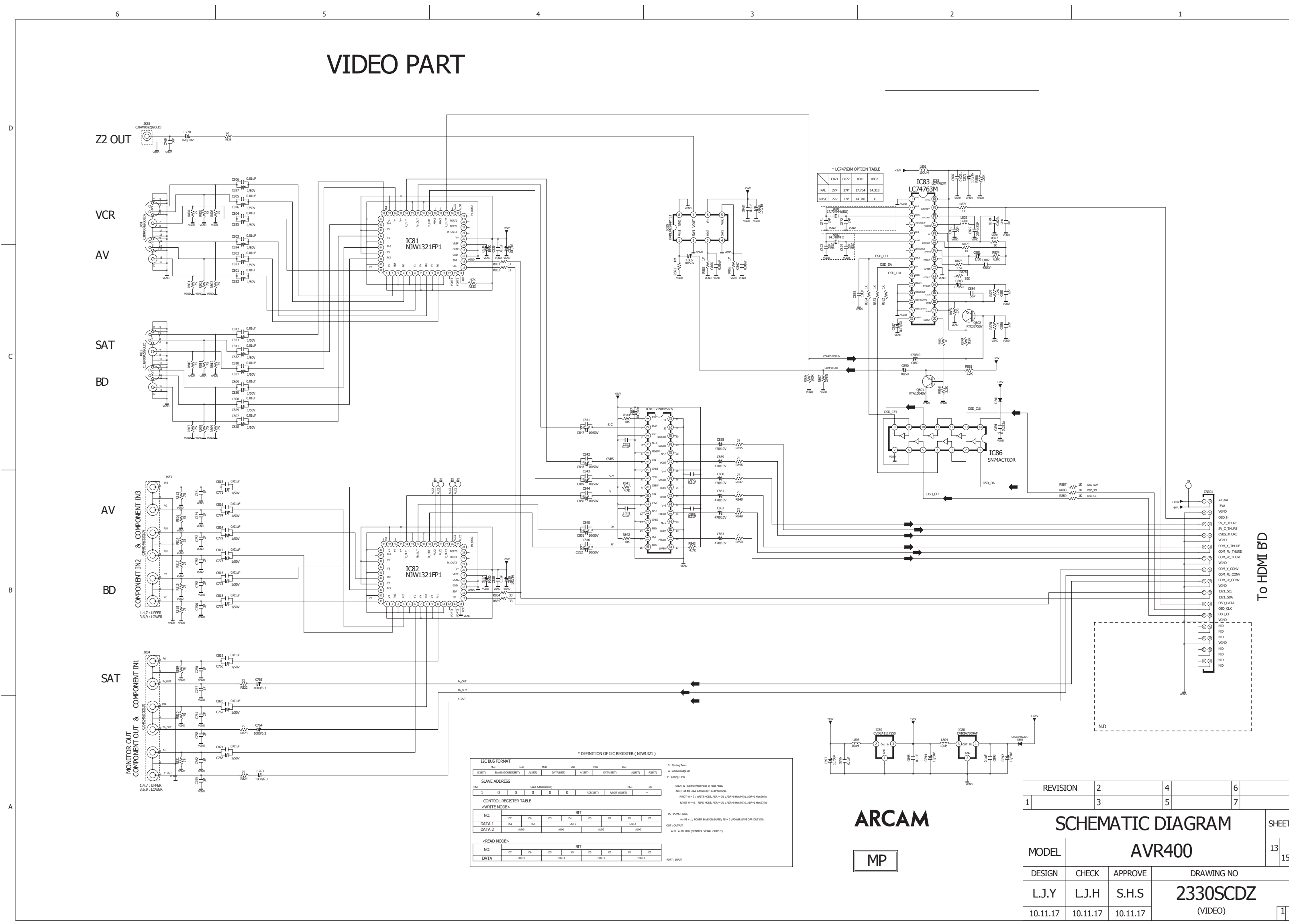

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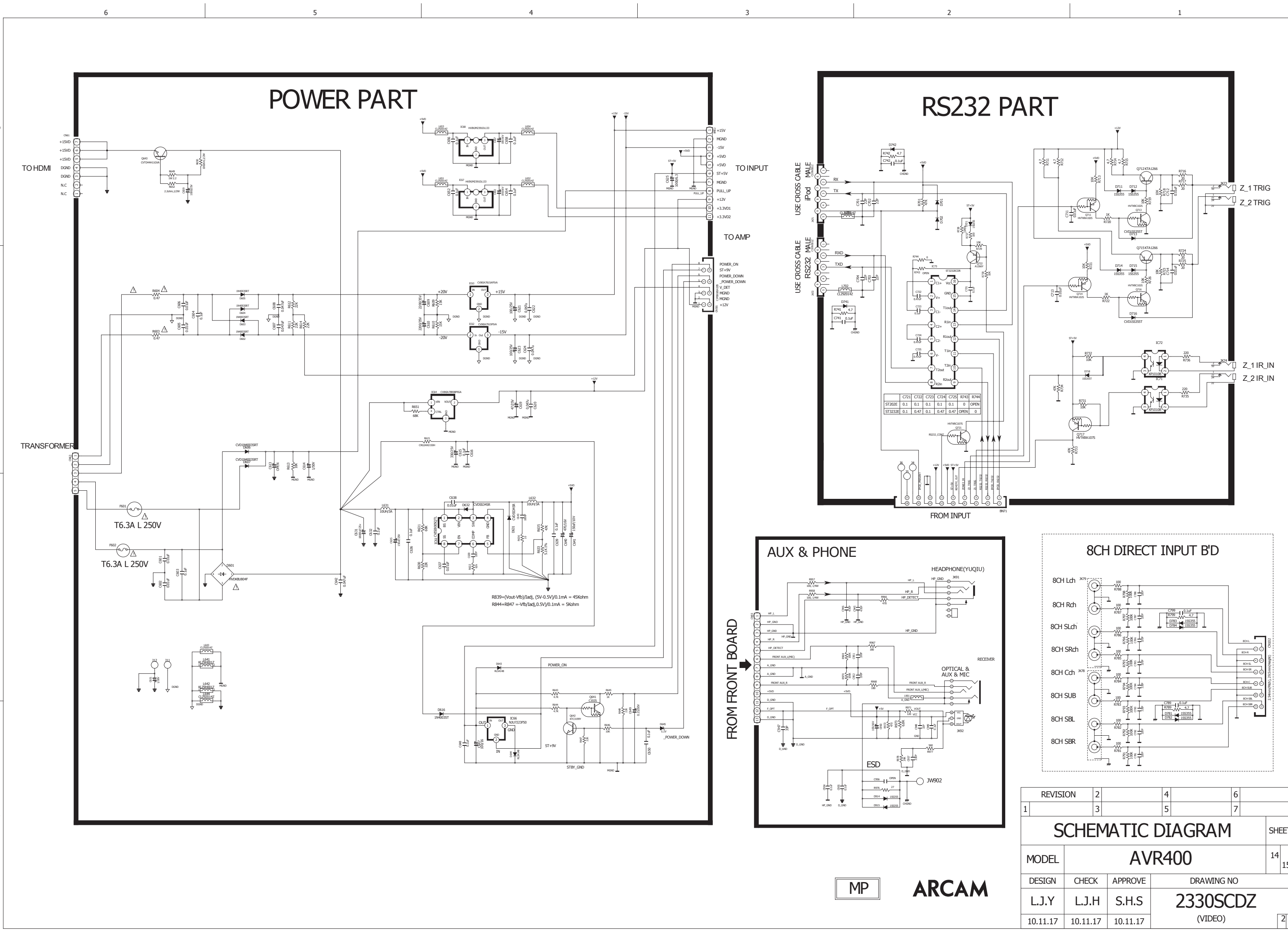

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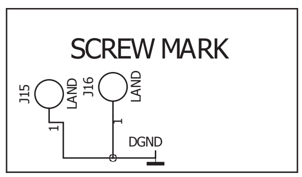

MP

ARCAM

REVISION	2		4		6	
1	3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR400		15 / 15
DESIGN	CHECK	APPROVE	DRAWING NO
L.J.Y	L.J.H	S.H.S	2330SCDZ (VIDEO) 3 / 3
10.11.17	10.11.17	10.11.17	

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