Application Note AN-AT1201-1

AN-AT1201-1: Design and Layout Guidelines for the AT1201

1. Introduction

This document provides detailed design and layout guidelines for the AT1201. The evaluation board schematic and layout files for the AT1201 are useful for reference purposes.

2. Design Overview for the AT1201

2.1 Simplified Reference Schematic

A typical high-level connection to the AT1201 is shown in Figure 1 below.

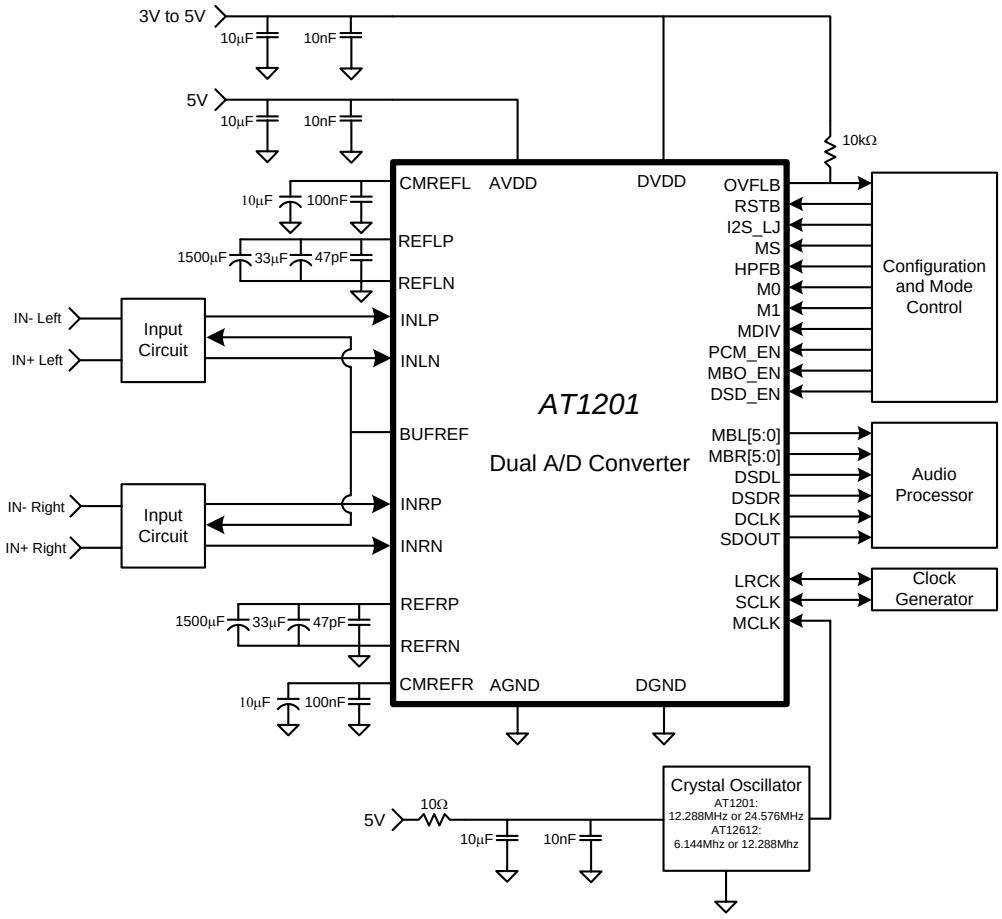


Figure 1: Simplified Applications Circuit

2.2 Pinout

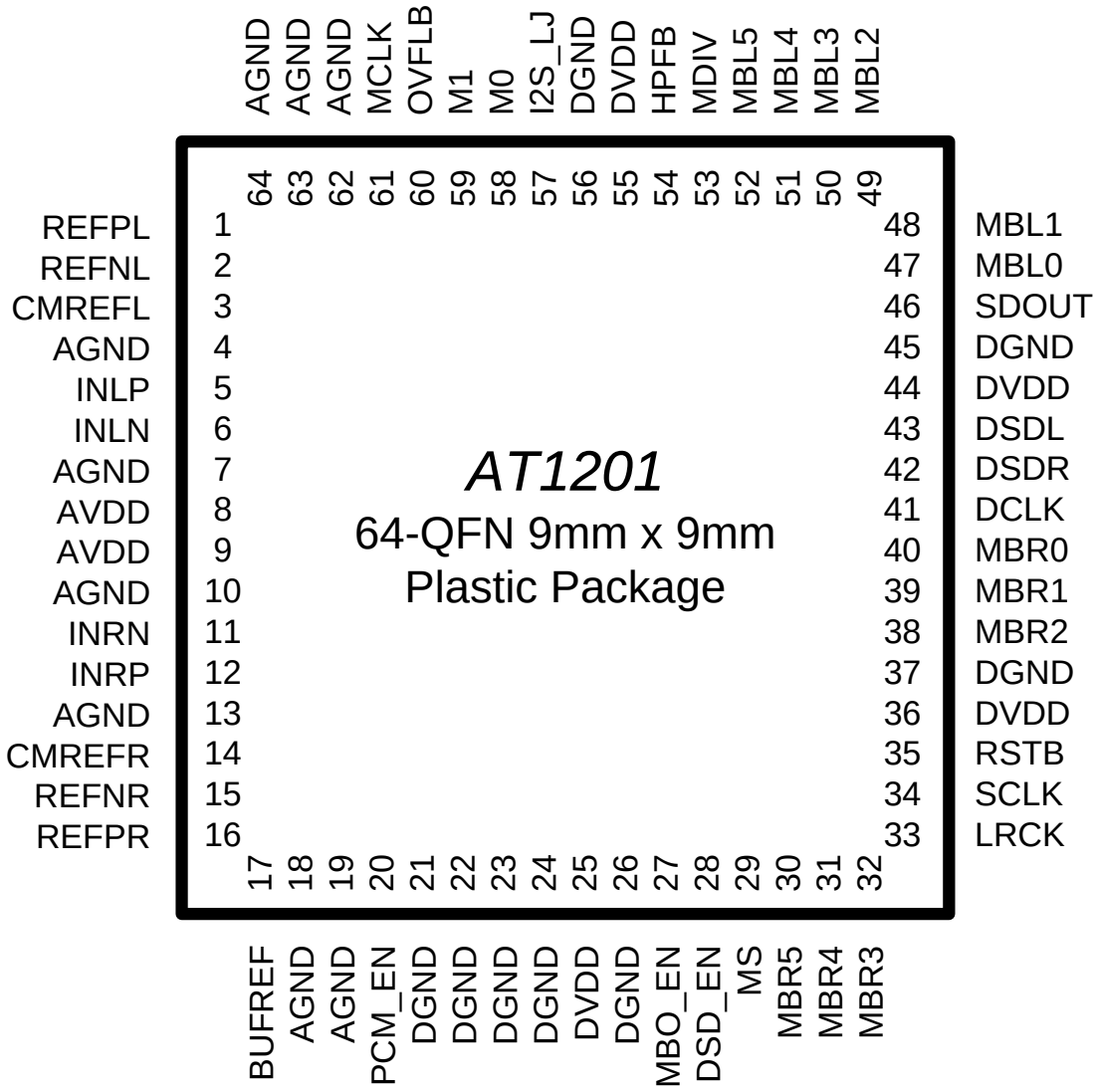


Figure 2: AT1201 Pinout

3. Interfacing Recommendations

3.1 Power Supply

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
4, 7, 10, 13, 18, 19, 62, 63, 64	AGND	Analog Ground	**Analog Ground** – Ground return for analog section
8, 9	AVDD	Analog Supply	**Analog Power** – Positive power supply for analog section
21, 22, 23, 24, 26, 37, 45, 56	DGND	Digital Ground	**Digital Ground** – Ground return for digital section
25, 36, 44, 55	DVDD	Digital Supply	**Digital Power** – Positive power supply for digital section

Table 1: Power Supply Pins

Proper power supply filtering is imperative for achieving the highest level of performance. The analog and digital supplies, AVDD and DVDD, should be generated from separate 5V low-noise regulators. The following circuit shows an example of how this regulated supply can be generated using a low-noise linear regulator such as the LT1762EMS8-5#PBF.

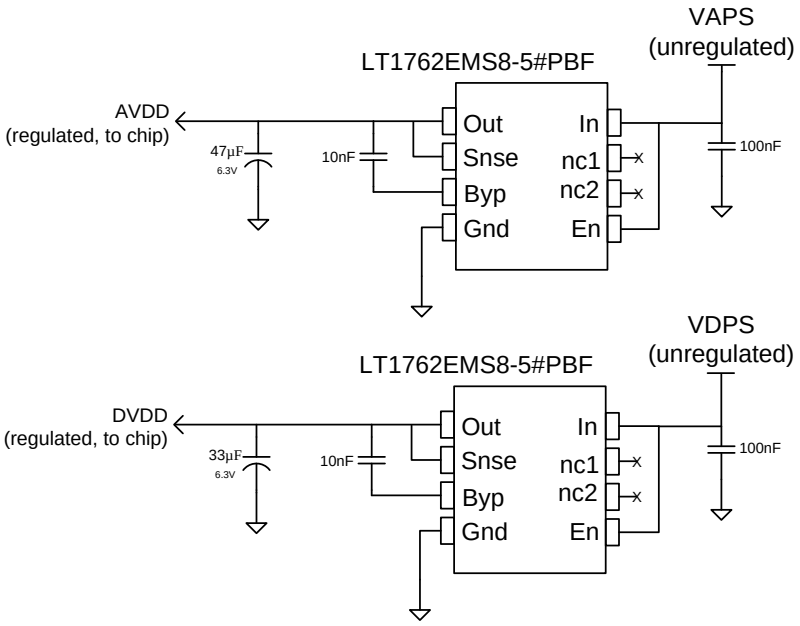


Figure 3: Analog and Digital Power Supply Regulation

3.2 Power-Up Sequence

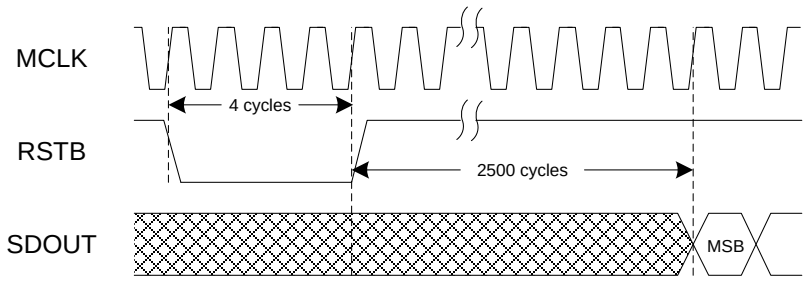
Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
35	RSTB	Digital Input	**Reset** – active low input, places devices in a low power mode
8, 9	AVDD	Analog Supply	**Analog Power** – Positive power supply for analog section
25, 36, 44, 55	DVDD	Digital Supply	**Digital Power** – Positive power supply for digital section

Table 2: Reset and Supply Pins

The AT1201 has an active low reset pin, RSTB. The device should be maintained in reset till power supplies, clocks and configuration pins are stable or be placed in reset if any of the supply voltages drop below their minimum operating voltages. RSTB must be asserted for at least 4 cycles of MCLK.

For the device to produce valid data, all internal reference voltages should be stable. To ensure the output data is valid, there is an internal delay, less than 2500 LRCK cycles, between the reset pin going high and the generation of valid outputs. When RSTB is asserted, SDOUT holds its last state.



Reset to Data Valid Timing

Figure 4: Reset Timing

3.3 Analog Input Network and BUFREF Reference

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
5 6	INLP INLN	Analog Input	**Differential Left Channel Input** – Differential analog input to the left channel ΣΔ modulator
11 12	INRN INRP	Analog Input	**Differential Right Channel Input** – Differential analog input to the right channel ΣΔ modulator
17	BUFREF	Analog Output	**Input Buffer Common-Mode Reference Voltage** – Reference voltage for the buffers driving the analog inputs

Table 3: Input Related Pins

INLP, INLN, INRN, and INRP are the differential analog inputs to the ΣΔ modulator for the left and right channels, respectively. BUFREF is an internally generated reference voltage for the buffers driving the analog inputs. Resistors R1 and R2 trim BUFREF to its optimum value, which must be set precisely to 2.4V for the AT1201.

The OPA1632 analog input buffers shown below have been designed for a 120kHz -3dB, single pole roll-off. The buffer bandwidth can be altered by changing passives around the operational amplifiers.

The signal gain through the input buffers is approximately 0.3 V/V, making the full-scale input level +23dBu. As with the buffer bandwidth, the gain can be altered by changing passives. Arda Technologies can provide assistance if a different gain is desired.

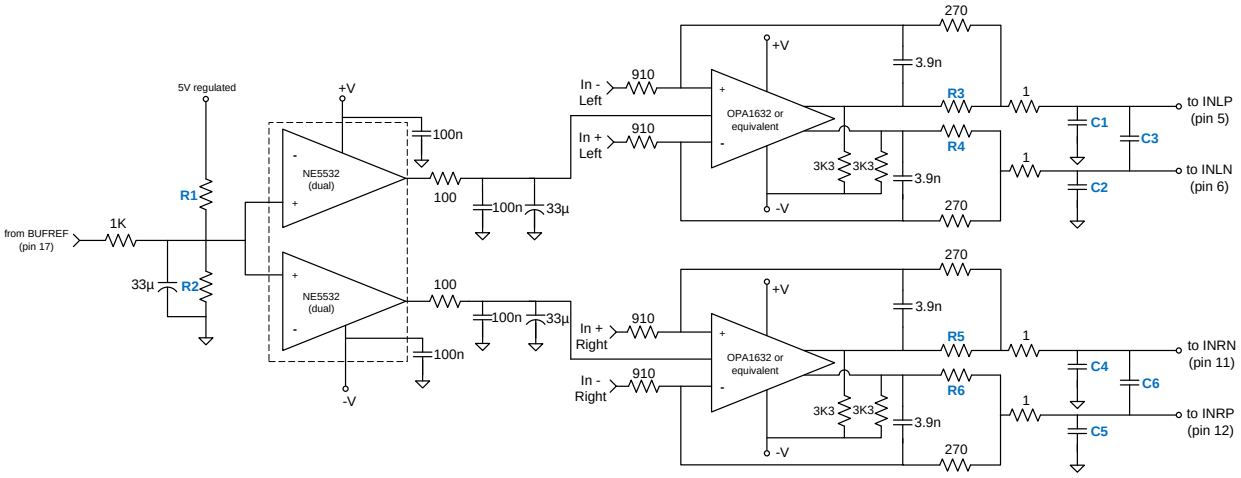


Figure 5: Input Network, AT1201

Component	Values
R1	3.3K
R2	2.61K
R3,R4,R5,R6	40.2Ω
C1,C2,C4,C5	1.2nF
C3,C6	3.3nF

Table 4: Recommended Input Network Component Values

3.4 Reference Network Connection

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
1	REFPL	Analog Input	**High Reference Left Channel** – High reference voltage for left channel, ties to capacitor
2	REFNL	Analog Input	**Low Reference Left Channel** – Low reference voltage for left channel, ties to analog ground
15	REFNR	Analog Input	**Low Reference Right Channel** – Low reference voltage for right channel, ties to analog ground
16	REFPR	Analog Input	**High Reference Right Channel** – High reference voltage for right channel, ties to capacitor

Table 5: Reference Pins

REFPL and REFPR serve as the internally generated high reference voltage for the left and right channels, respectively. REFNR and REFNL serve as the low reference voltage for the left and right channels, and connect to analog ground.

There are two alternatives for reference connections. The can be loaded with capacitors, or driven with an opamp circuit. Both alternatives are described below. The opamp drive allows for smaller capacitors and improved low frequency distortion.

Alternative 1: Capacitor Loading

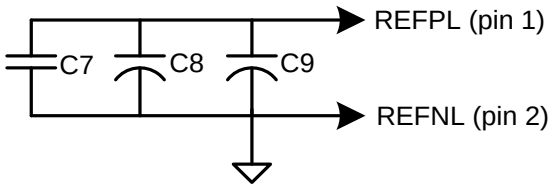


Figure 6: Left Channel Reference

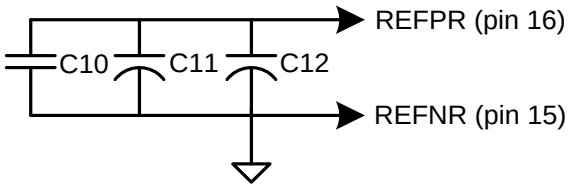


Figure 7. Right Channel Reference

Component	Value	Vendor
C7,C10	47pF	Murata GRM1885C2A470JA01D
C8,C11	33µF	Nichicon F321A336MAA
C9,C12	1500µF	Nichicon UWT0J152MNL

Table 6: Recommended Reference Network Capacitors

Alternative 2: Active Drive

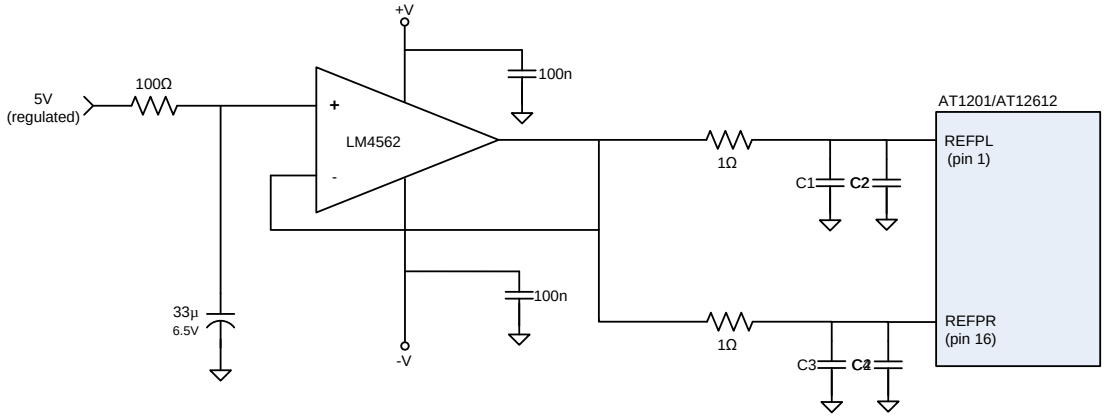


Figure 8: Active Drive for References

Component	Value	Vendor
C1, C3	47pF	Murata GRM1885C2A470JA01D
C2, C4	330µF	Vishay Sprague TR3D337K6R3C0125 or Kemet T520D337M006ATE025

Table 7: Recommended Reference Network Capacitors

Comparison of alternatives

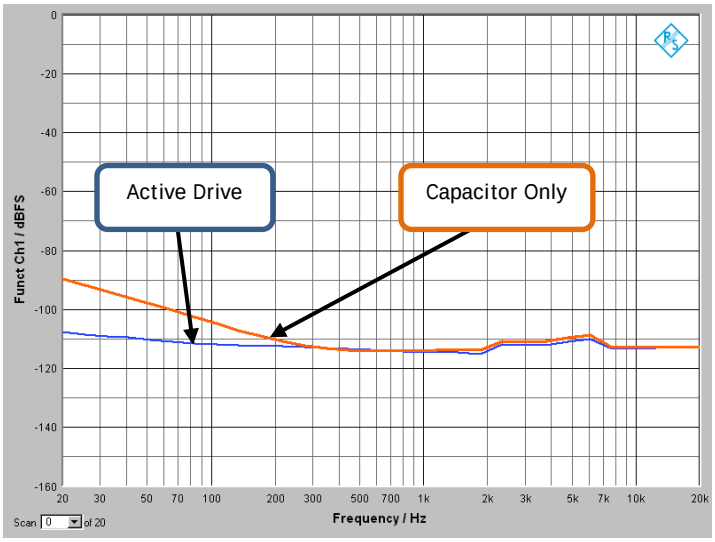


Figure 9: THD+N vs. Frequency (Unweighted), AT1201, Fs = 48kHz, -2dB Input

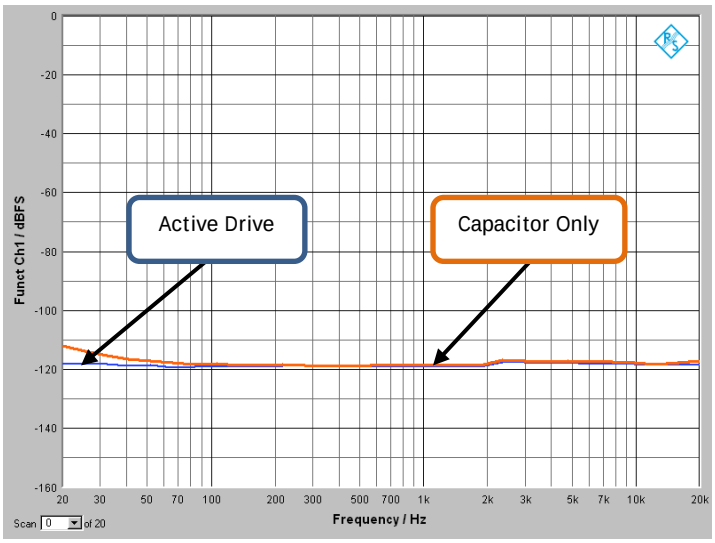


Figure 10: THD+N vs. Frequency (Unweighted), AT1201, Fs = 48kHz, -10dB Input

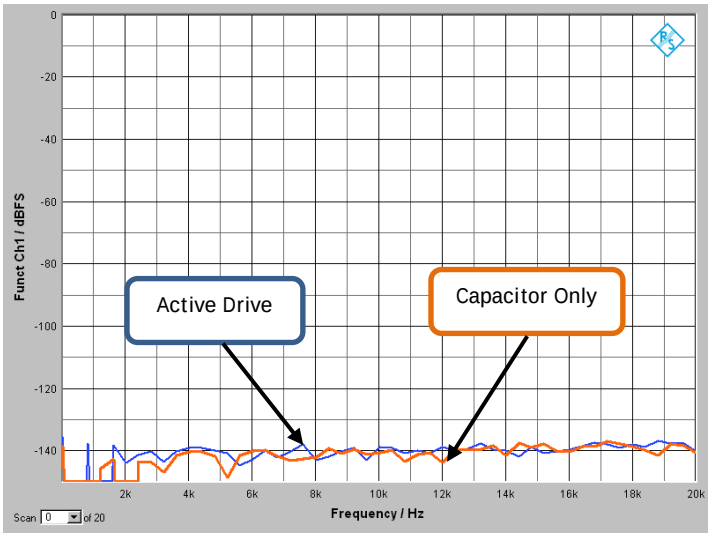


Figure 11: Interchannel Isolation, AT1201, Fs = 48kHz, Right Channel at 0dB and Left Channel Undriven, Left Channel Shown in Diagram

3.5 Common Mode Voltage Outputs

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
3	CMREFL	Analog Output	**Common-Mode Voltage** - Internally generated reference voltage, ties to capacitor
14	CMREFR	Analog Output	**Common-Mode Voltage** - Internally generated reference voltage, ties to capacitor

Table 8: Common Mode Reference Pins

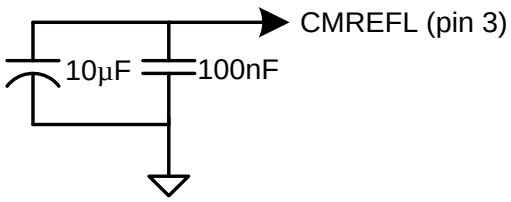


Figure 12: CMREFL Connection

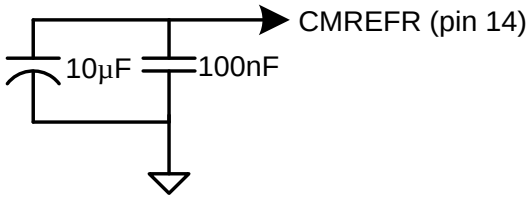


Figure 13: CMREFR Connection

3.6 Clocking Recommendation & Sampling Rate Selection

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
53	MDIV	Digital Input	**MCLK Divider** – Enables divide by 2 of master clock
58 59	M0 M1	Digital Input	**Mode Selection** – Selects among the following sampling rates: Single, double, quad, and octal
61	MCLK	Digital Input	**Master Clock** – Clock for the ΣΔ modulator and digital filters

Table 9: Mode Selection Pins

To ensure the best possible performance, it is recommended that the MCLK crystal oscillator be supplied with a separate low-noise, regulated 5V supply. An LT1762EMS8-5#PBF low-noise linear regulator is recommended.

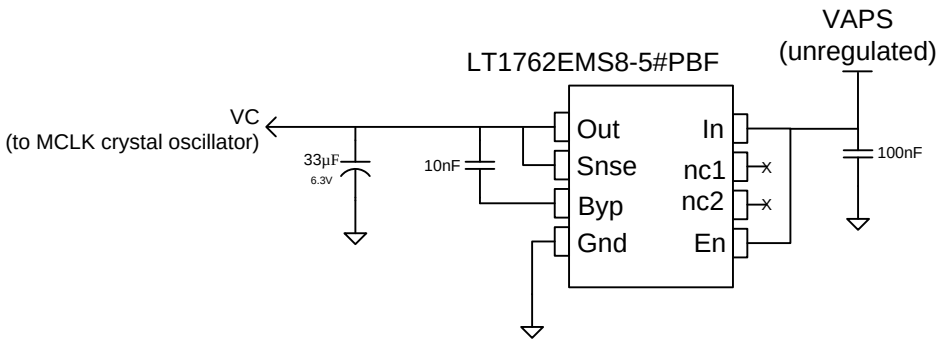


Figure 14: Crystal Oscillator Power Supply Regulation

The AT1201 operates with a 512x or 256x master clock (MCLK). The 512x MCLK is required for octal mode operation but otherwise provides identical functionality to the 256x MCLK.

For a given MCLK, the MDIV, M1, and M0 inputs must be set at the appropriate logic level to obtain the desired output sampling rate Fs. Table 10, Table 11, and Table 12 below show the appropriate logic levels for MDIV, M1, and M0 given a desired output sampling frequency. Note that Octal-speed mode is only supported with the AT1201 running off of the double-rate MCLK.

Configuration	Mode	MDIV	M1	M0	Output Sampling Frequency Fs	Fs for MCLK = 12.288Mhz
AT1201 12.288Mhz	Single-Speed	0	0	0	MCLK / 256	48kHz
	Dual-Speed	0	0	1	MCLK / 128	96kHz
	Quad-Speed	0	1	0	MCLK / 64	192kHz
	Octal-Speed	N/A	N/A	N/A	N/A	N/A

Table 10: Supported Operating Modes for MCLK = 12.288Mhz Input (AT1201 only)

Configuration	Mode	MDIV	M1	M0	Output Sampling Frequency Fs	Fs for MCLK = 24.576Mhz
AT1201 24.576Mhz	Single-Speed	1	0	0	MCLK / 512	48kHz
	Dual-Speed	1	0	1	MCLK / 256	96kHz
	Quad-Speed	1	1	0	MCLK / 128	192kHz
	Octal-Speed	0	1	1	MCLK / 64	384kHz

Table 11: Supported Operating Modes for MCLK = 24.576Mhz Input (AT1201 only)

Combinations of MDIV, M1, M0, and MCLK rate other than those shown above are invalid. Note that the only way to operate at octal speed mode is to use the AT1201 with the MCLK frequency set to be 512x, or nominally 24.576MHz.

3.7 Master/Slave Mode Selection

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
29	MS	Digital Input	**Master/Slave mode** – Selects clock master or clock slave mode for PCM output, high=master / low=slave

Table 12: Master/Slave Pin

The pin, MS, selects operation in PCM master or slave mode. In Master Mode, LRCK and SCLK are generated synchronously on-chip. In Slave Mode, LRCK and SCLK are generated externally and are inputs to the device. In addition, in Master Mode the MDIV input is used to internally divide the master clock.

	MS = 0	MS = 1
Clock Mode	Slave	Master

Table 13: Master/Slave Mode Selection

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Master Mode, AT1201

In Master mode, the internally generated LRCK and SCLK clocks function as outputs. The LRCK is equal to F_S, the sampling frequency, and the SCLK is equal to 64xF_S. Note that for the AT1201 to operate in octal speed mode, MCLK must be a 512x clock, MDIV must be set low, and M1/M0 must both be set high.

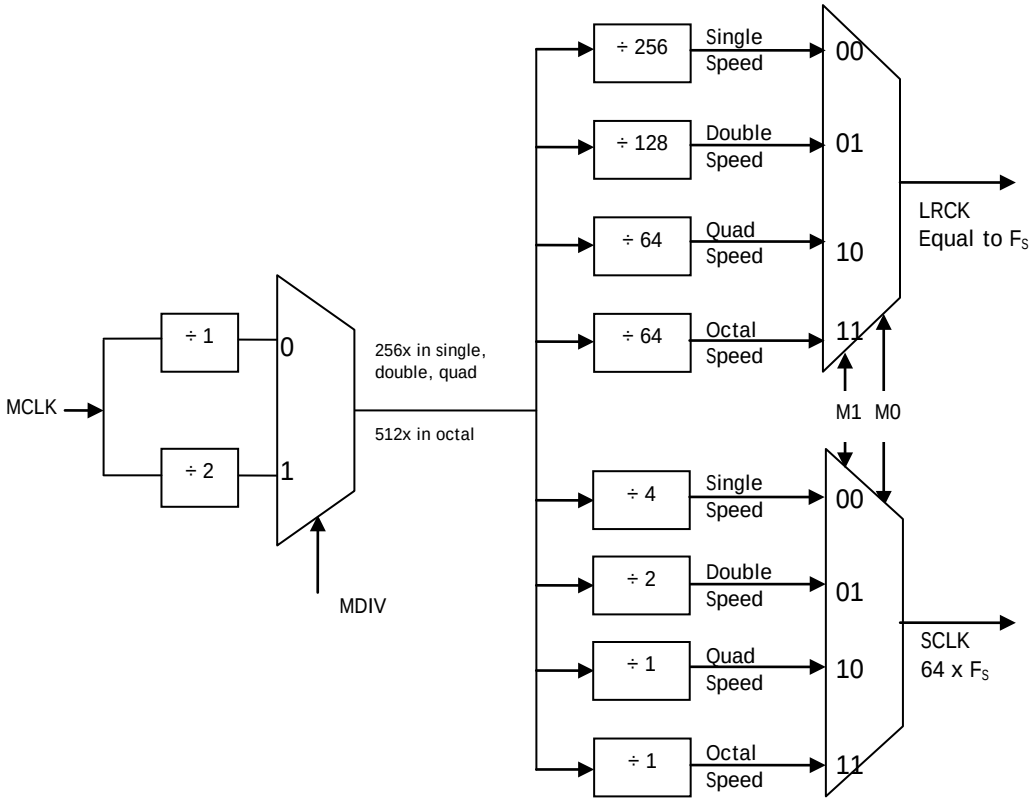

Figure 15: Master Mode, AT1201

Slave Mode, AT1201

In Slave mode, the SCLK and LRCK are inputs. It is recommended that both the LRCK and SCLK be generated synchronously with the MCLK. In addition, it is recommended that LRCK be equal to F_S, the sampling frequency, and the SCLK should be equal to 64 x F_S.

AT1201	Single-Speed F_S=2kHz-54kHz	Double-Speed F_S=50kHz-108kHz	Quad-Speed F_S=100kHz-216kHz	Octal-Speed F_S=200kHz-432kHz
MCLK/LRCK	256x, 512x	128x, 256x	64x, 128x	64x
SCLK/LRCK	64x	64x	64x	64x

Table 14: Slave Mode, AT1201

3.8 Highpass Filter

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
54	HPFB	Digital Input	**Highpass Filter** – Enables digital highpass filter, active low

Table 15: Highpass Filter Pin

A first-order IIR highpass filter is present in the PCM signal path. The -3dB frequency is 0.47Hz at Fs = 48kHz and scales with Fs. The filter is activated when the HPFB pin is pulled low.

The highpass filter can be turned on for a few seconds to acquire the signal path offset then disabled. Once disabled, the offset continues to be subtracted from the signal, but the filter's frequency response is no longer present. Alternatively, the filter can operate continuously.

3.9 Overflow Indicator

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
60	OVFLB	Digital Output	**Overflow** – Detects overflow on either channel

Table 16: Overflow Indicator Pin

The AT1201 detects overflow on each input channel. The active low OVFLB signal is time multiplexed with LRCK for ease of latching. Each channel can enter the overflow condition independently of the other. However, overflow is exited only after both channels have exited the overflow state. The OVFLB signal is asserted one SCLK period after an LRCK transition in left-justified mode. In this mode, the rising edge of LRCK latches the right channel overflow condition, while the falling edge of LRCK latches that of the left channel.

The OVFLB signal is asserted two SCLK periods after an LRCK transition in I^2S mode. In this mode, the rising edge of LRCK latches the left channel overflow condition, while the falling edge of LRCK latches that of the right channel.

The OVFLB signal is an open-drain signal requiring a 10kΩ pull up resistor to DVDD on the PC board. This allows multiple AT1201 devices to share a single pull up resistor to form a wired-OR function.

3.10 Digital Outputs

PCM Mode Outputs

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
20	PCM_EN	Digital Input	**Enable PCM Output** – Enables internal filters and generates serial audio output
33	LRCLK	Digital Input/Output	**Left Right Clock** – Indicates whether left or right channel is active on the serial audio data line
34	SCLK	Digital Input/Output	**Serial Clock** – Clock for the serial audio interface
46	SDOUT	Digital Output	**Serial Audio Data Output** – PCM output for left and right channels
57	I2S_LJ	Digital Input	**Audio Output Format Select** – Selects either the I2S or left justified output format, high=I2S / low=LJ

Table 17: PCM Mode Output Pins

The AT1201 outputs PCM audio data on SDOUT when PCM_EN is pulled high. LRCLK and SCLK serve as outputs in Master mode and inputs in Slave mode (see section 3.7). The AT1201 can produce either I2S or LJ (left justified) formatted PCM output. The format selection is made by setting the package pin, I2S_LJ as shown in the Table below.

	I2S_LJ = 0	**I2S_LJ = 1**
PCM Format	LJ	I^2S

Table 18: Selecting Between I^2S and LJ Modes

The following configuration is recommended on the PCM outputs to minimize the coupling from the digital outputs into the analog inputs:

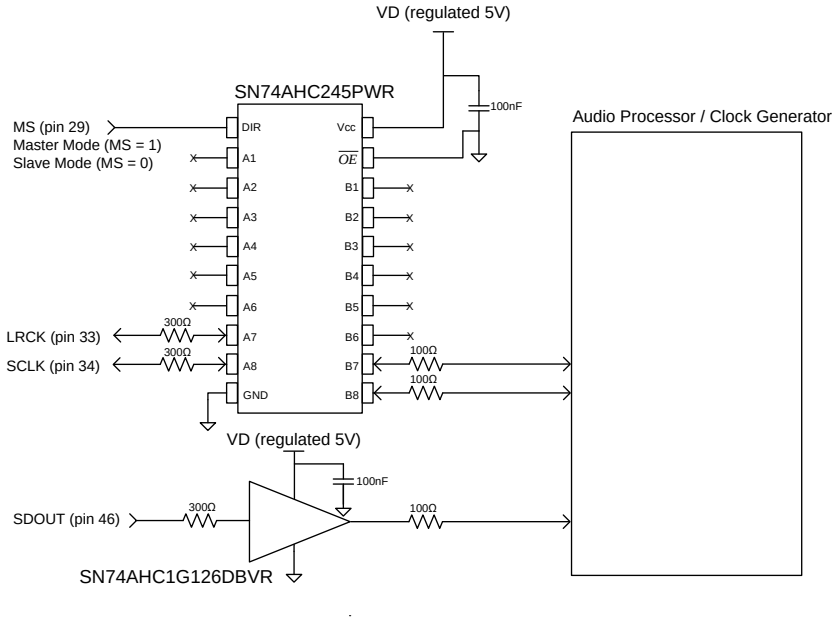

Figure 16: Output Buffer, PCM Inputs/Outputs

Note that the SN74AHC245PWR is a bidirectional buffer, and that the direction is controlled by the DIR pin. When MS = 1 (Master Mode), LRCK and SCLK are outputs of the AT1201 and the direction of the buffer is set accordingly. When MS = 0 (Slave Mode), LRCK and SCLK are inputs into the AT1201 and the direction of the buffer is set accordingly. Since SDOUT is always an output of the AT1201, a unidirectional buffer like the SN74AHC1G126DBVR will suffice.

DSD Output

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
28	DSD_EN	Digital Input	**DSD Output Enable** – Enables right and left channel DSD outputs
41	DCLK	Digital Output	**Clock Out** – Clock for DSD and Multibit outputs
42	DSDR	Digital Output	**DSD Output** – Right channel DSD output
43	DSDL	Digital Output	**DSD Output** – Left channel DSD output

Table 19: DSD Pins

The AT1201 enters DSD output mode when the DSD_EN pin is pulled high. Bit streams running at MCLK or MCLK/2, depending on the state of MDIV, are generated at the DSDL/DSDR pins. Furthermore, a full rate clock signal, DCLK, is provided to facilitate the acquisition of the DSD data. The DSD output rate is 256x.

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The following configuration is recommended to minimize the coupling from the digital outputs into the analog inputs:

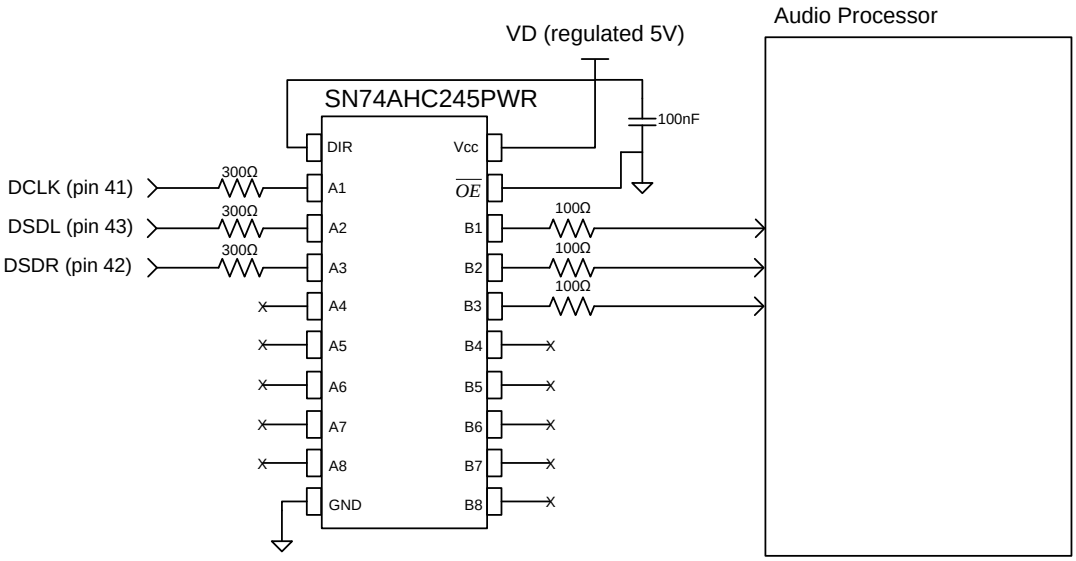

Figure 17: Output Buffer, DSD Outputs

Multibit Output

Relevant Pins:

Terminal No.	Terminal Name	Type	Pin Description
27	MBO_EN	Digital Input	**Multibit Modulator Output Enable** – Enables right and left channel multibit modulator outputs
30	MBR5	Digital Output	**Multibit Modulator Output** – Right channel output bit 5
31	MBR4	Digital Output	**Multibit Modulator Output** – Right channel output bit 4
32	MBR3	Digital Output	**Multibit Modulator Output** – Right channel output bit 3
38	MBR2	Digital Output	**Multibit Modulator Output** – Right channel output bit 2
39	MBR1	Digital Output	**Multibit Modulator Output** – Right channel output bit 1
40	MBR0	Digital Output	**Multibit Modulator Output** – Right channel output bit 0
41	DCLK	Digital Output	**Clock Out** – Clock for DSD and Multibit outputs
47	MBL0	Digital Output	**Multibit Modulator Output** – Left channel output bit 0
48	MBL1	Digital Output	**Multibit Modulator Output** – Left channel output bit 1
49	MBL2	Digital Output	**Multibit Modulator Output** – Left channel output bit 2
50	MBL3	Digital Output	**Multibit Modulator Output** – Left channel output bit 3
51	MBL4	Digital Output	**Multibit Modulator Output** – Left channel output bit 4
52	MBL5	Digital Output	**Multibit Modulator Output** – Left channel output bit 5

Table 20: Multibit Output Pins

The AT1201 enters multibit output mode when the MBO_EN pin is pulled high. Bit streams running at MCLK or MCLK/2, depending on the state of MDIV, are generated at the MBL[5:0]/MBR[5:0] pins. Furthermore, a full rate clock signal, DCLK, is provided to facilitate the acquisition of the multibit data. The multibit data is represented in two's complement form. The multibit modulator output rate is 256x for the AT1201.

	MDIV = 0	MDIV = 1
MCLK/DCLK	1	2

Table 21: MCLK/DCLK Ratio

The following configuration is recommended to minimize the coupling from the digital outputs into the analog inputs:

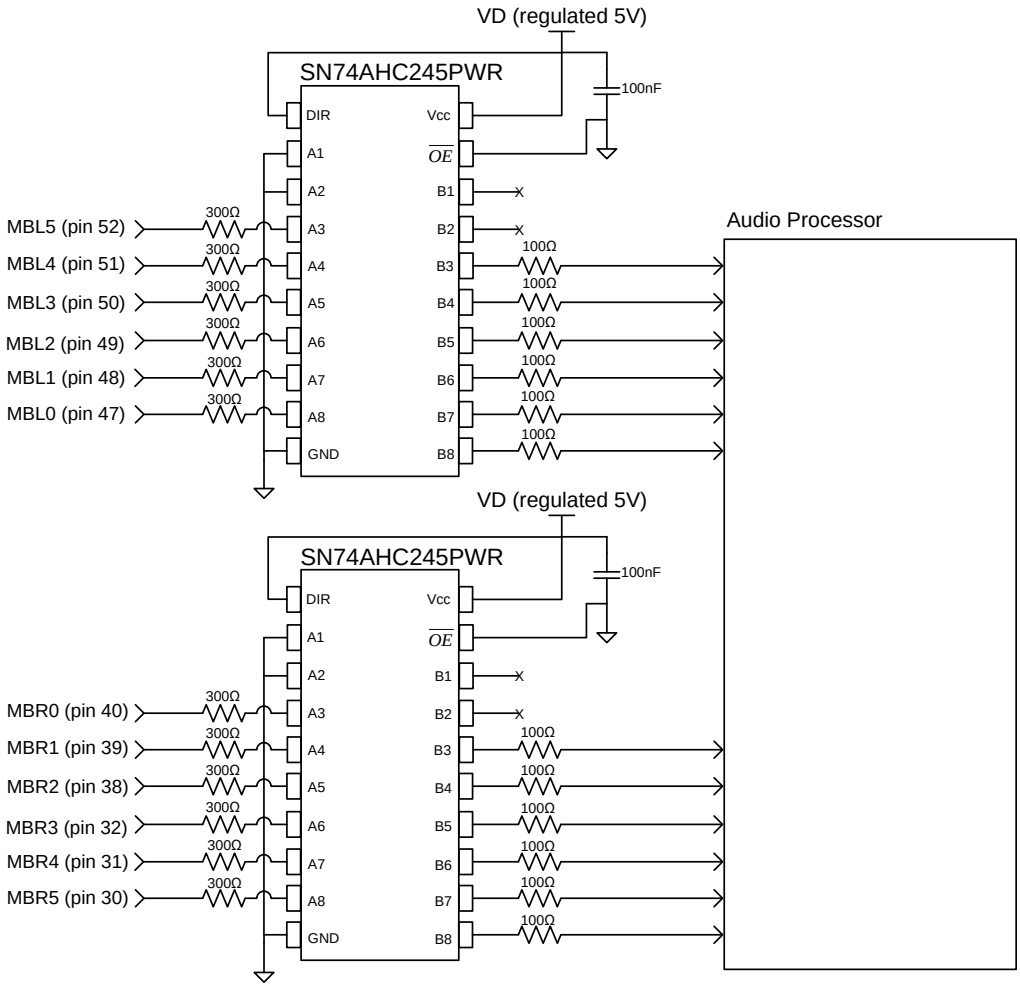

Figure 18: Output Buffers, MBO Outputs

For optimal performance, a low-noise linear voltage regulator like the LT1762EMS8-5#PBF should be used to power the PCM, DSD, and MBO output buffers as shown below:

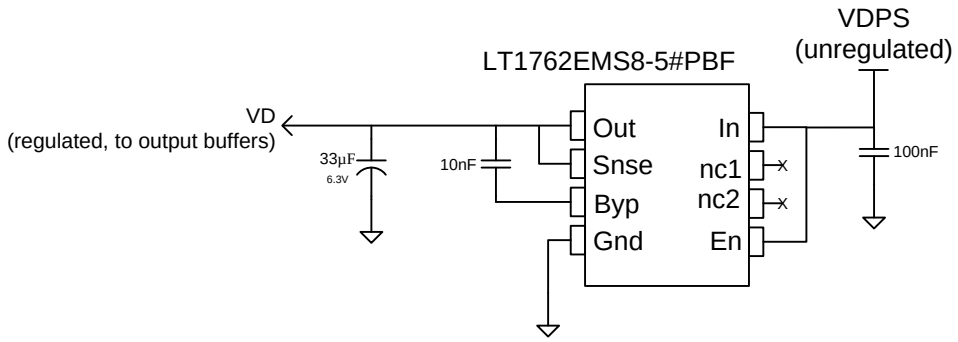

Figure 19: Regulated Supply for Output Buffers

4. Layout Guidelines

The following PCB layout guidelines were used when designing the AT1201 Evaluation Kit. The schematic and layout files for the Evaluation Kit are available upon request.

Input Network/Input Lines

1. Layout component placement should be symmetrical about p, n throughout the signal path.
2. Left/Right channels should be isolated with a ground trace on the same layer as the signal.
3. Trace lengths should be matched about p, n.
4. Signal crossovers should be avoided.
5. Digital signals should stay clear of this input section to avoid coupling.
6. Input capacitor pi-network and series resistors should be placed as close to the chip as possible, as shown below:

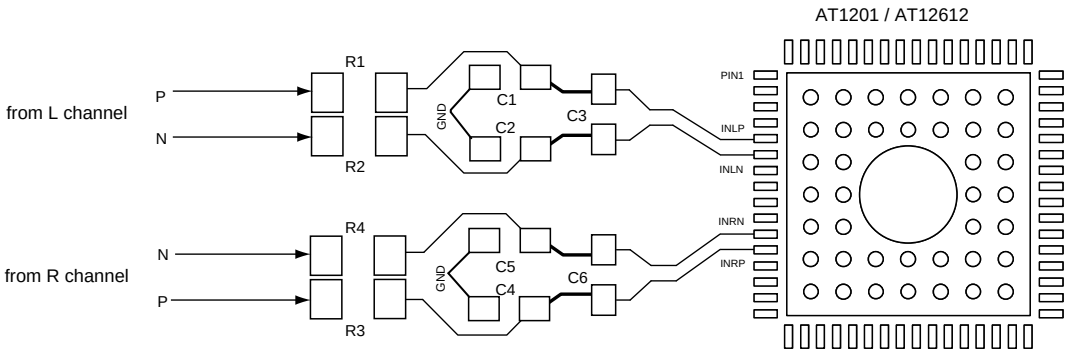

Figure 20: Input Network Layout Placement Example

Reference Capacitors

7. Reference capacitors should be placed as close to REFP as possible, as shown in the figure below:

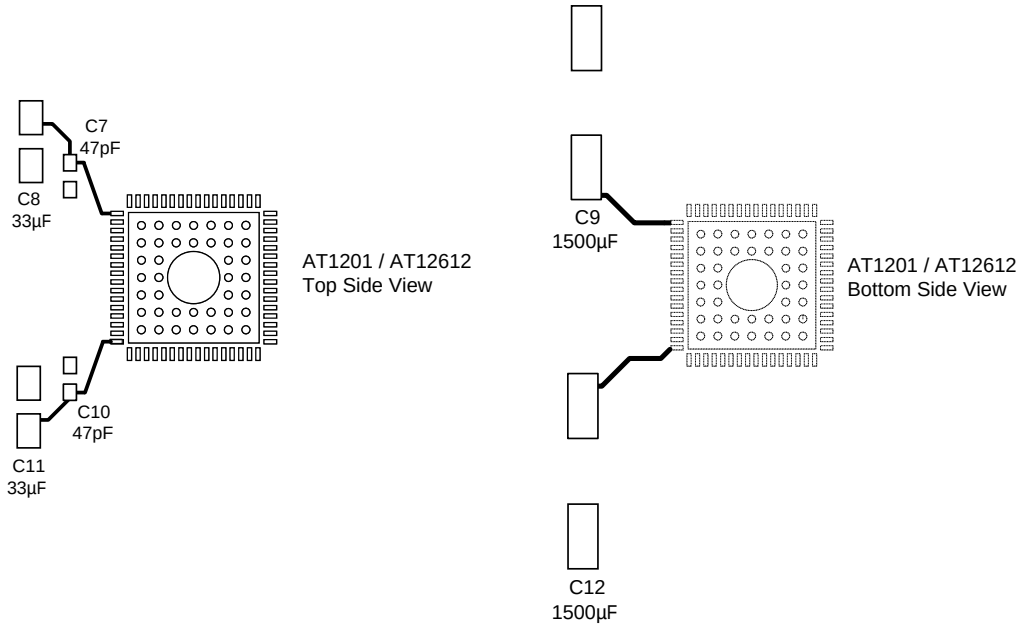

Figure 21: REFP Capacitor Layout Placement Example

Clocking Circuitry

8. The clocking circuitry should be kept away from the analog input and digital circuitry.

Power Plane

9. The AT1201 Evaluation Board uses a split power plane to keep AVDD and DVDD separate. This helps to prevent noise coupling between the different supplies.
10. Avoid routing critical signal traces over the split power planes. Otherwise return current needs to find a long path to ground, adding additional inductance in the return path.

Grounding/Bypass Capacitors

11. Bypass capacitors should be placed as close to the AT1201 as possible.

Ground Vias

12. Ground routing on top and bottom layers should be kept as short as possible. Ground vias should be used to connect from the top and bottom layers to the adjacent ground plane.

Ground Paddle

13. A ground paddle is necessary for good heat dissipation for the chip and low ground inductance. See the figure below for more details.
14. The hole in the center of the footprint is to facilitate assembly rework.

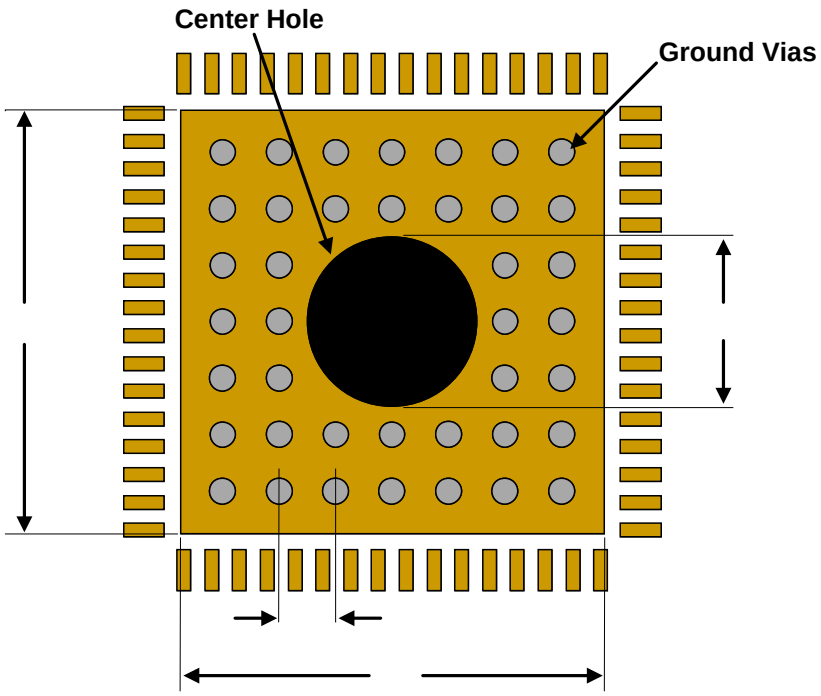

Figure 22: Ground Paddle Diagram

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