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Analysis, simulation and circuit implementation of a precise high-output impedance analog current mirror

N. CHARALAMPIDIS¹, K. TSIKMAKIS¹, M. SPASOS¹, K. HAYATLEH² AND N. MALLIOS¹

¹ Department of Electronics

Alexander Technological Educational Institute (ATEI)

Sindos, Thessaloniki

GREECE

² School of Technology

Oxford Brookes University

Oxford, OX33 1HX

UNITED KINGDOM

ncharalampidis@gmail.com

Abstract: - The decision for the most appropriate current mirror topology when designing a circuit is a matter of trade-offs between impedance, current transfer ratio, area on chip, power consumption and voltage-headroom, expandability etc. Current mirrors are mainly used for biasing, for transferring current from one part of the circuit to another or as load for amplifier stages. This paper presents the theoretical analysis, the simulation and the circuit built of a current mirror with excellent performance characteristics compared to conventional designs at the expense of voltage-headroom. Great emphasis in the analysis of the circuit has been paid on the current transfer ratio and the output impedance of the configuration.

Key-Words: - Current mirror, Current transfer ratio, High impedance

1 Ideal and practical current mirror

A simplified block diagram of a current mirror (CM) is shown in Fig. 1. It is a topology with three terminals and ideally the output current is identical to the input current, the input voltage is zero and the output impedance is infinite. Thus, when is used instead of passive components it provides insensitivity to power supply variations and temperature [1].

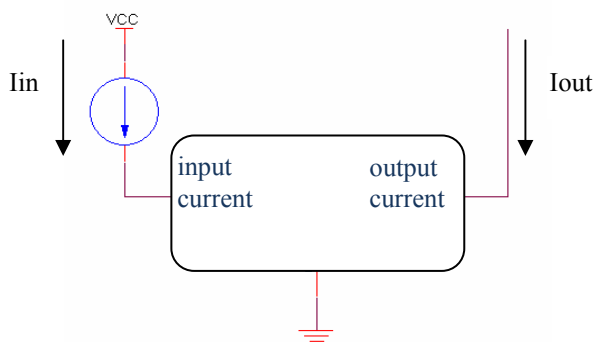


Fig. 1. The ideal current mirror

In practice no such ideal unit exists. The output current changes when altering the output voltage hence the output AC impedance of the configuration

is not constant. A voltage drop is created in the input terminals, which is subtracted from the voltage applied to the current source, consequently the output current is different than the expected [2]. Input and output currents are different due to the gain-error source, which is divided into the systematic and the random gain error, too. Finally, the performance of a current mirror depends on the biasing of the output transistors, which should be high enough to keep transistors in the active region and low enough to maximize the range of output voltages where the output impedance is constant.

2 Precise high output impedance CM

The proposed current mirror is shown in Fig. 2. The circuit shown can be used as a current sink and the PNP version of that can be used as a current source. The only drawback, as it will be shown below, is that the output resistance of the current source, which depends on the current gain and the Early voltage of the devices used, will be slightly reduced. Although complementary transistors can assure that $\beta_p \approx \beta_n$, it does not follow that the Early Voltage VAP will be equal to VAN, which affects the output impedance. The magnitude of the operating current (I_{in}), for both source and sink, can be set by a single resistor which can be either on-chip or externally connected for more operational flexibility or silicon area saving.

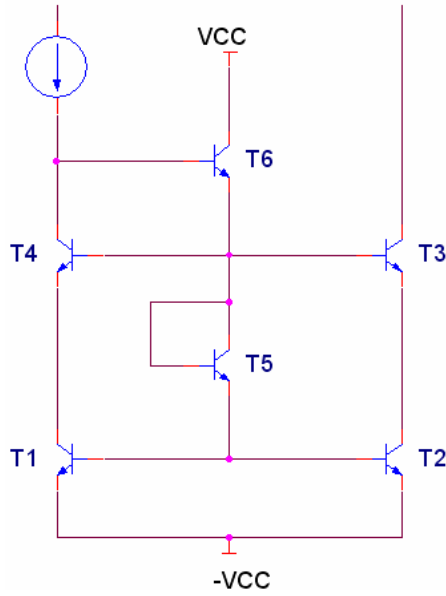


Fig. 2. Precise high output impedance CM

2.1 Analysis of the current transfer ratio

The analysis of the current transfer ratio of the presented current mirror can be carried out by identifying the current in every branch of the circuit.

Starting from the base of T3, the current will be

$$I_{B3} = \frac{I_E}{\beta_3 + 1} \quad (1)$$

Thus, the currents in the collector and the emitter of the same transistor will, respectively, be

$$I_{C3} = \frac{\beta_3 I_{E3}}{\beta_3 + 1} \quad (2)$$

$$I_{E3} = \frac{I_{CE}(\beta_3 + 1)}{\beta_3} \quad (3)$$

since,

$$\frac{(\beta + 1)}{\beta} = \frac{1}{\alpha} \quad (4)$$

and

$$I_{out} = I = I_{C3} \quad (5)$$

The current in the base of T3 will be,

$$I_{B3} = \frac{I_{C3}}{\beta_3} = \frac{I}{\beta_3} \quad (6)$$

and

$$I_{E3} = (\beta_3 + 1)I_{B3} = \frac{(\beta_3 + 1)I}{\beta_3} = \frac{I}{\alpha} \quad (7)$$

which is the current in the collector of T2.

Hence,

$$I_{B2} = \frac{I_{C2}}{\beta_2} = \frac{\frac{I}{\alpha}}{\beta_2} = \frac{I}{\alpha\beta_2} \quad (8)$$

Transistors T1 and T2 form a Widlar current mirror. If their collector current is

$$I_{C1} = I_{S1} e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE1}}{E_{A1}} \right) \quad (9)$$

and

$$I_{C2} = I_{S2} e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE2}}{E_{A2}} \right) \quad (10)$$

assuming that the Early voltage is very high, compared to the V_{CE} of T1 and T2, the collector current will be [3],

$$I_{C1} = I_{S1} e^{\frac{V_{BE}}{V_T}} \quad (11)$$

and

$$I_{C2} = I_{S2} e^{\frac{V_{BE}}{V_T}} \quad (12)$$

The V_{BE} is identical, so

$$I_{C1} = \frac{I_{S1}}{I_{S2}} I_{C2} \quad (13)$$

Setting $\frac{I_{S1}}{I_{S2}} = n$ and since $I_{E3} = \frac{I}{\alpha}$ and $I_{E4} = I_{C1}$,

$$I_{E4} = \frac{I_{S4}}{I_{S3}} \frac{I}{\alpha} = \frac{nI}{\alpha} \quad (14)$$

and

$$I_{B1} = \frac{I_{C1}}{\beta_1} = \frac{\frac{nI}{\alpha}}{\beta_1} = \frac{nI}{\alpha\beta_1} \quad (15)$$

Furthermore,

$$I_{C4} = \frac{\beta_4 I_{E4}}{\beta_4 + 1} = \alpha I_{E4} = \alpha \frac{nI}{\alpha} = nI \quad (16)$$

and

$$I_{B4} = \frac{I_{C4}}{\beta_4} = \frac{nI}{\beta_4} \quad (17)$$

Using Kirchhoff's current law,

$$I_{E5} = I_{B1} + I_{B2} = \frac{nI}{\alpha\beta_1} + \frac{I}{\alpha\beta_2} \quad (18)$$

Since all transistors apart from T6 have almost the same collector current and base-emitter voltage, it can be assumed that the β parameter of transistors T1-T5 will be the same. Transistor T6 has relatively smaller collector current as it will be shown later.

Hence,

$$I_{E5} = \frac{I}{\alpha\beta}(n+1) \quad (19)$$

and

$$I_{B5} = \frac{I}{\alpha\beta}(n+1) \quad (20)$$

Using Kirchhoff's current law in the emitter of T6

$$I_{E6} = I_{B4} + I_{B3} + I_{B5} = \frac{nI}{\beta} + \frac{I}{\beta} + \frac{I}{\alpha\beta}(n+1) \quad (21)$$

Hence,

$$I_{B6} = \frac{I_{E6}}{\beta_6 + 1} = \frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1 + \frac{1}{\alpha}\right) \quad (22)$$

and the input current will be,

$$I_{IN} = I_{B6} + I_{C4} = \frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1 + \frac{1}{\alpha}\right) + nI \quad (23)$$

Thus, the current transfer ratio will be,

$$\lambda = \frac{I_{OUT}}{I_{IN}} = \frac{I}{\frac{I}{\beta(\beta_6 + 1)}(n+1)\left(1 + \frac{1}{\alpha}\right) + nI} \quad (24)$$

For $\beta \gg 1$ and $(\beta_6 + 1) \approx \beta_6$, it can be written as,

$$\lambda = \frac{1}{n\left[1 + \frac{(n+1)2}{n\beta\beta_6}\right]} = \frac{1}{n\left[1 + \frac{2 + \frac{2}{n}}{\beta\beta_6}\right]} \quad (25)$$

and finally, for $\frac{2}{n} \approx 2$, $n = \frac{I_{S1}}{I_{S2}} \approx 1$ and $\beta_6 \approx \beta$,

$$\lambda = \frac{1}{1 + \frac{4}{\beta^2}} \quad (26)$$

Eventually, the current transfer ratio will be very close to unity, since $4 \ll \beta^2$.

For comparison reasons a similar analysis has been carried out for several well-known current mirrors. Their current transfer ratio and their output impedance, which will be analyzed in the next paragraph, are shown in Table I. Figure 3 shows the proposed current mirror including all currents as derived from the theoretical analysis.

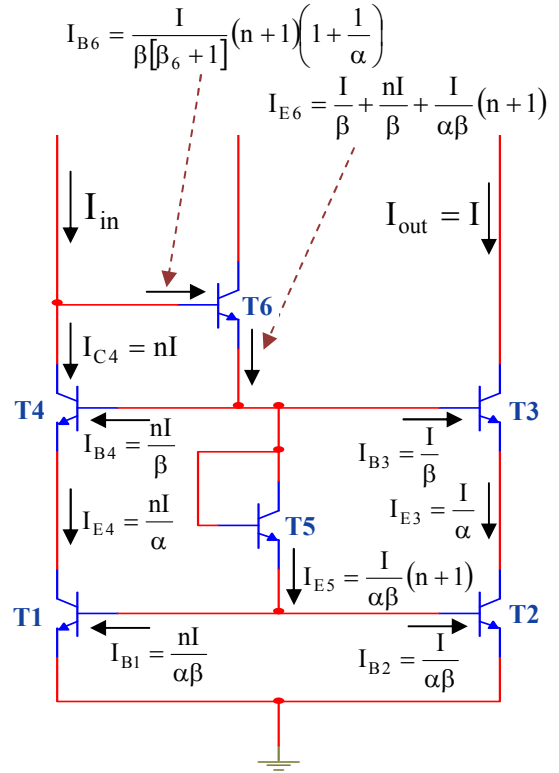


Fig. 3. Proposed CM including currents

2.2 Analysis of the output impedance

The analysis of the proposed current mirror will be carried out using the small signal equivalent circuit of the configuration. Ignoring the output resistance r_{CE} of each transistor apart from T3, which is the output transistor, the small signal circuit will be as shown in Fig. 4.

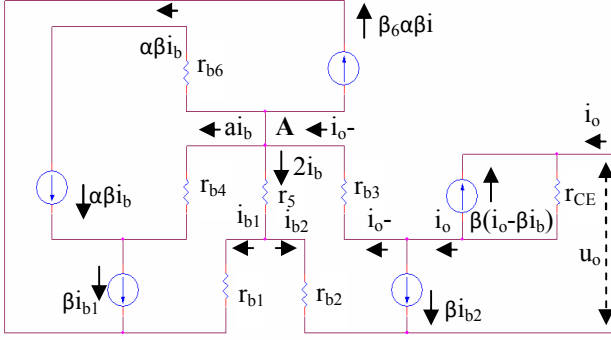


Fig. 4. Small signal equivalent circuit of the proposed CM

Assuming that a small in magnitude current, i_o , is applied to the output of the circuit and that parameter β is identical for all transistors apart from that of T6, the analysis can begin from the base current of T1 and T2 which is i_b . Thus, in the output of T2 the current will be βi_b . Hence, the base current of T3 will be,

$$i_{bT3} = i_o - \beta i_b \quad (27)$$

For transistor T1, the collector current is again βi_b , thus the collector current of T4 will be,

$$I_{C4} = \frac{\beta \beta i_b}{\beta + 1} \text{ or,}$$

$$I_{C4} = \alpha \beta i_b \quad (28)$$

Hence, the base current of T4 is αi_b and the base current of T6 is equal to I_{C4} .

Using Kirchhoff's current law in point A,

$$i_o = i_b (\beta + \alpha + \alpha \beta + \alpha \beta \beta_6 + 2) \quad (29)$$

Assuming that $\alpha = \frac{\beta}{\beta + 1} \approx 1$ and that $\alpha \beta \beta_6$ is the biggest term in the parenthesis,

$$i_b = \frac{i_o}{\alpha \beta \beta_6} \quad (30)$$

In the output of the circuit, the current that is passing through r_{CE} is given by,

$$i_{r_{CE}} = i_o + \beta(i_o - \beta i_b) = \frac{u_o - u_{C2}}{r_{CE}} \quad (31)$$

Substituting (30) in (31),

$$i_o + \beta \left(i_o - \frac{\beta i_o}{\alpha \beta \beta_6} \right) = \frac{u_o - u_{C2}}{r_{CE}} \quad (32)$$

and

$$\frac{u_o - u_{C2}}{r_{CE}} = i_o \left(1 + \beta \left(1 - \frac{1}{\alpha \beta_6} \right) \right) \quad (33)$$

since $\frac{1}{\alpha \beta_6} \ll 1$ and solving for u_o ,

$$\frac{u_o}{i_o} = r_{CE} (\beta + 1) + \frac{u_{C2}}{i_o} \quad (34)$$

In the above equation, the term u_{C2} is positive but very small in magnitude, so it can be ignored. Thus, (34) can be written as,

$$\frac{u_o}{i_o} \approx r_{CE} (\beta + 1) \approx r_o \beta \quad (35)$$

This will be the output impedance of the circuit. It can be seen that it is at least twice the output impedance of a Wilson current mirror, ignoring the second term in (34). Table I presents a comparison between the output impedance of the proposed mirror and several other well-established mirrors, analyzed in a similar manner. The superiority of the proposed current mirror is obvious.

TABLE I
Current transfer ratio and output impedance

Conf.	Current transfer ratio, λ	R_o
Widlar	$\frac{I}{\frac{I_{S1}}{I_{S2}} + 1 + \frac{1}{\beta_1} + \frac{1}{\beta_2}}$	$\frac{E_A}{I_{OUT}}$
Buf. Widlar	$\frac{I}{\frac{I_{S1}}{I_{S2}} (1 + \frac{1}{\beta_1(\beta_3 + 1)}) + \frac{1}{\beta_2(\beta_3 + 1)}}$	$\frac{E_A}{I_{OUT}}$
Wilson	$\frac{I}{\frac{I_{S1}\beta_2(\beta_3 + 1)}{I_{S2}\beta_3(\beta_2 + 1) + \frac{I_{S1}\beta_2\beta_3}{\beta_1}} + \frac{1}{\beta_3}}$	$\frac{\beta_o r_o}{2}$
Mod. Wilson	$\frac{I}{\frac{I_{S1}}{I_{S2}} + 1 + \frac{1}{\beta_1} + \frac{1}{\beta_2}}$	$\frac{\beta_o r_o}{2}$
Cas/de	$\frac{I}{\frac{I_{S1}}{I_{S2}} + 1 + \frac{1}{\beta_1} + \frac{1}{\beta_3} + \frac{1}{\beta_1\beta_3} + \frac{1}{\beta_2} + \frac{1}{\beta_3} + \frac{1}{\beta_2\beta_3}}$	$\frac{\beta_o r_o}{2}$
Prop. CM	$\frac{1}{1 + \frac{4}{\beta^2}}$	$r_o \beta$

3 Circuit Simulation

Following the theoretical analysis, a circuit simulation has been set up to investigate the current transfer ratio and the output impedance of the proposed current mirror compared to conventional mirrors. The simulation has been carried out in room temperature for 1mA operating current. Prior to the simulation, the β parameter of the transistor model used has been measured via simulation, to specify its value under these simulation conditions [4].

TABLE II

Theoretical and simulated output impedance and simulated current transfer ratio

Conf/tion	Theoretical output impedance	Simulated output impedance	Simulated current transfer ratio
Widlar	90K Ω	85K Ω	1.022
Buffered Widlar	90K Ω	83K Ω	1.03
Wilson	2.43M Ω	1.83M Ω	0.991
Modified Wilson	2.43M Ω	1.81M Ω	1.005
Cascode	2.43M Ω	1.9M Ω	0.993
Proposed CM	4.86M Ω	3.5M Ω	0.999

Table II presents a comparison between the theoretical output impedance and the simulated one, for six current mirrors, including the proposed circuit. Additionally, it presents the current transfer ratio derived by simulation for each circuit. The superiority of the proposed current mirror is obvious.

4 Circuit implementation

Having finished the theoretical analysis and the circuit simulation, the proposed current mirror as well as the rest of the conventional current mirror circuits built on PCB and tested in the lab. The HFA3096 transistor array from Intersil has been used, to make sure that all transistors in the circuits will have as similar as possible performance characteristics. The operating current has been set by an external potentiometer, to achieve precision in the input current. The circuits of the conventional mirrors are shown in Fig. 5 while the circuit of the proposed current mirror is shown in Fig. 6, respectively.

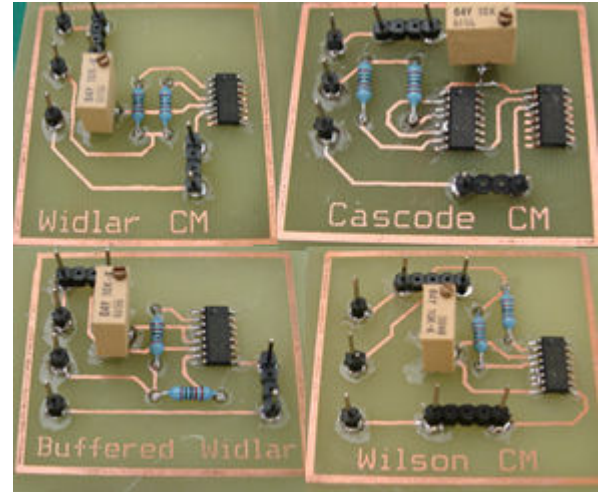


Fig. 5. Conventional CM circuits built for evaluation

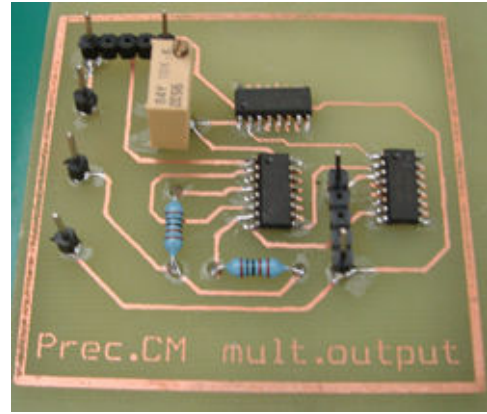


Fig. 6. The proposed precise CM built on PCB

Table III presents the current transfer ratio measured in the lab for all current mirrors. The performance of the proposed current mirror was better than the rest, as expected. The only drawback is the increased V_{BE} drops necessary for the circuit to operate properly.

TABLE III
Measured current transfer ratio

Conf/tion	Output current for 1mA input current	Current transfer ratio
Widlar	$I_{out}=0.979\text{mA}$	1.02
Buffered Widlar	$I_{out}=0.987\text{mA}$	1.013
Wilson	$I_{out}=0.996\text{mA}$	1.004
Cascode	$I_{out}=0.996\text{mA}$	1.004
Proposed CM	$I_{out}=0.999\text{mA}$	1.001

Figure 7 presents a snapshot of the evaluation of the proposed current mirror, as far as the current transfer ratio is concerned. The power supply used was 3.3V and the circuit was set to operate with 1mA of current. The amp-meter on the left indicates the input current and the one on the right the output current of the mirror. The lab-measurements agree with the simulation results. The current transfer ratio of the proposed current mirror is 0.999.

5 Conclusion

The analysis, simulation and implementation of a precise high output impedance current mirror have been presented. The performance characteristics of the proposed current mirror have been compared with those of conventional circuits theoretically, in simulation and in the lab, to justify its superiority over them. The proposed mirror offers overall better performance at the expense of additional voltage-headroom for biasing.

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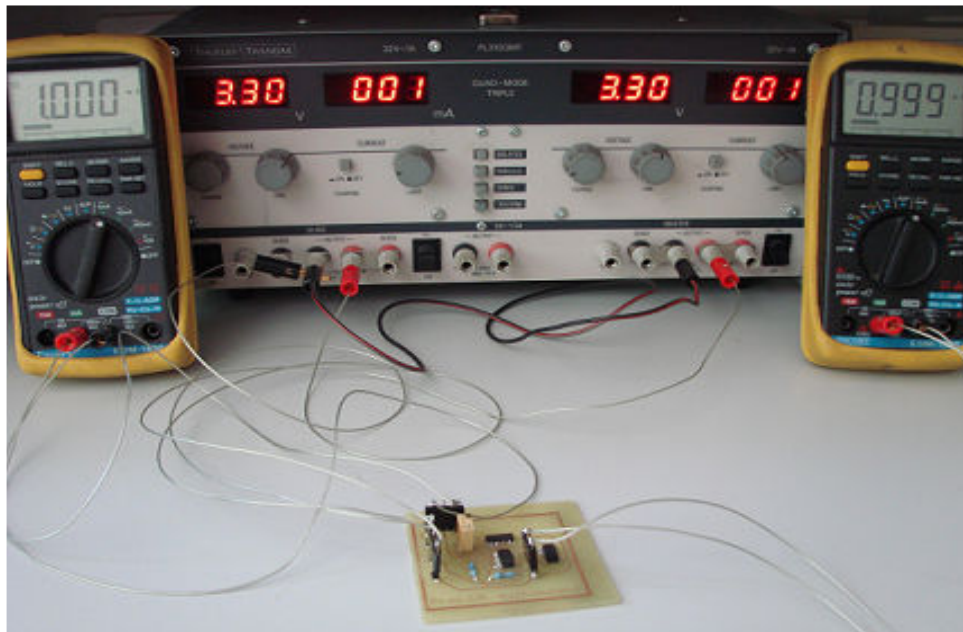


Fig. 7. Evaluation of the proposed current mirror in the lab