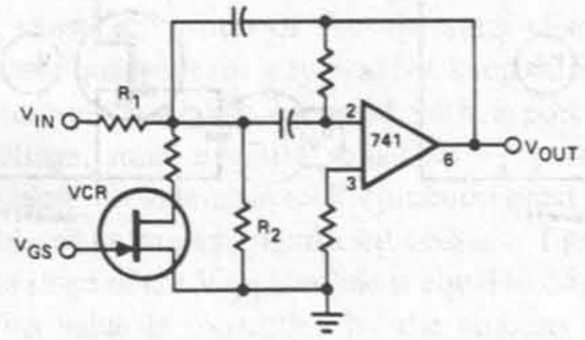
The highest value is

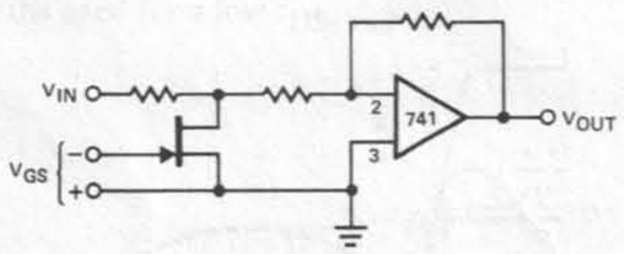
$$V_{OUT(max)} = V_{in} \quad (3)$$

since r_{DS} can be extremeley large.

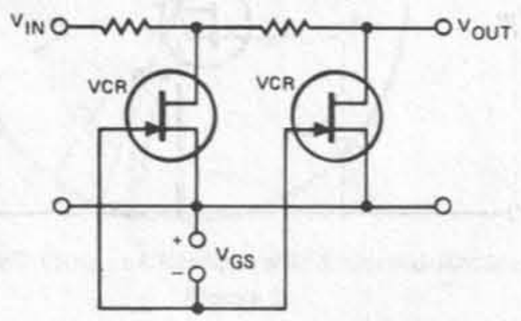
A number of other FET VCR applications are shown in Figures 9-16.



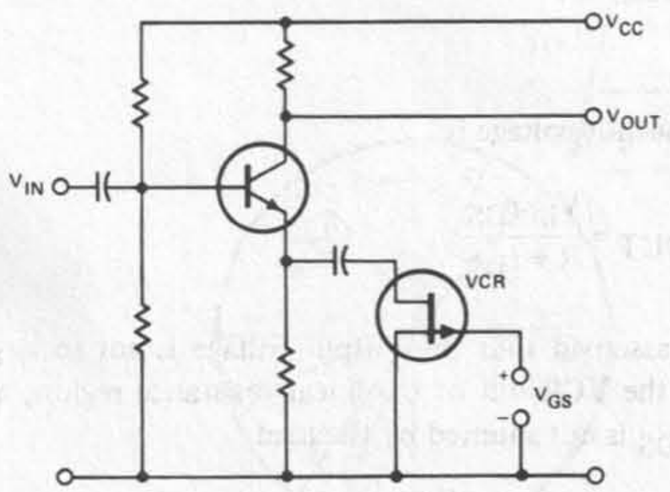
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



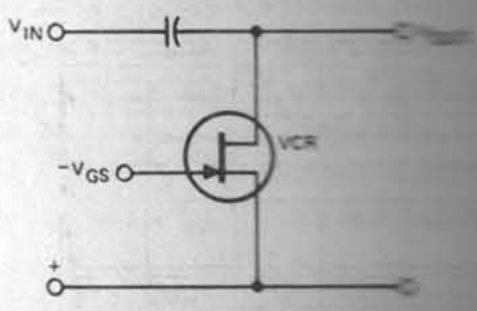
Electronic Gain Control
Figure 10



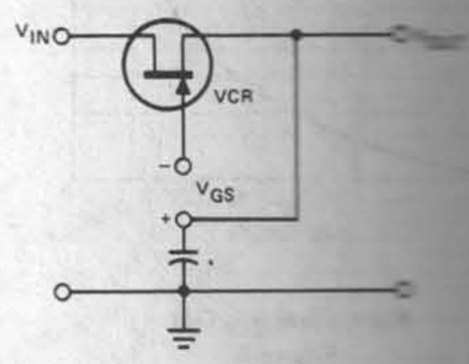
Cascaded VCR Attenuator
Figure 11



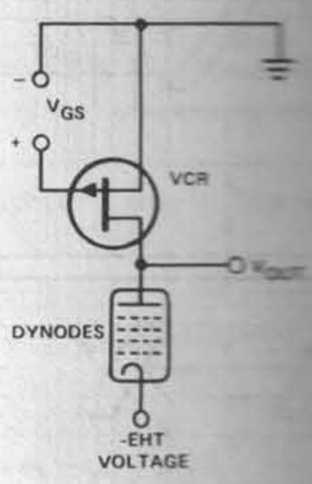
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



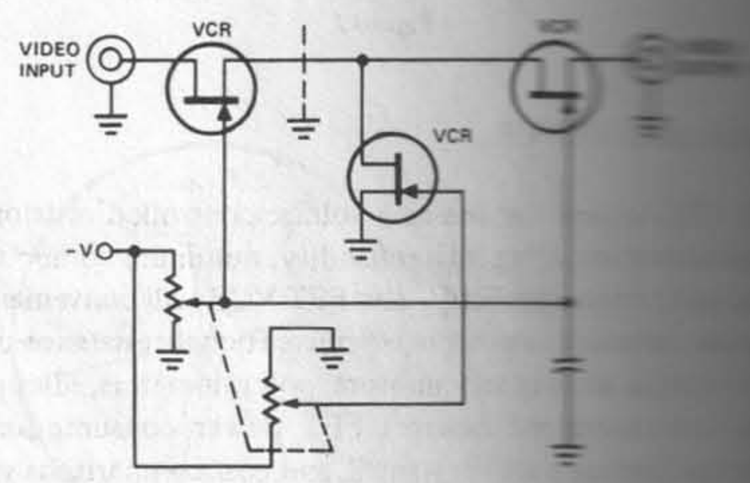
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



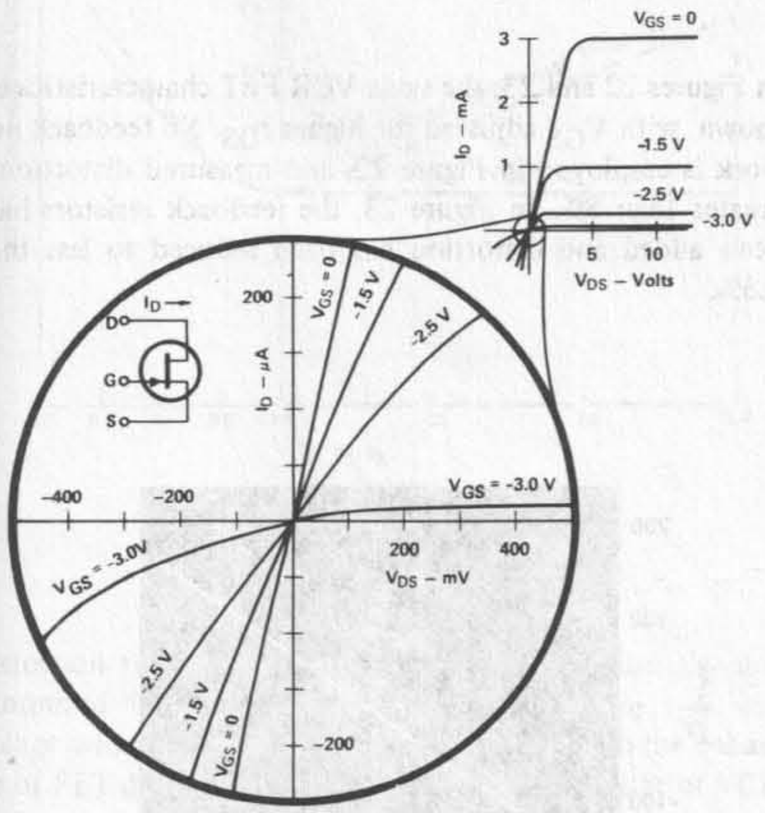
P-Channel VCR Photomultiplier Load. Required Low-Photomultiplier Anode Current (Usually < 1 μA) Implies that VCR will Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Two Antiparallel VCR's Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$

Figure 17A

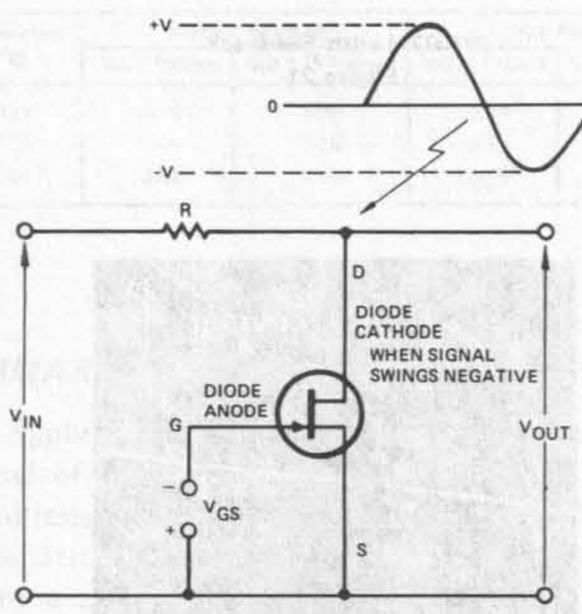


Figure 17B

in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

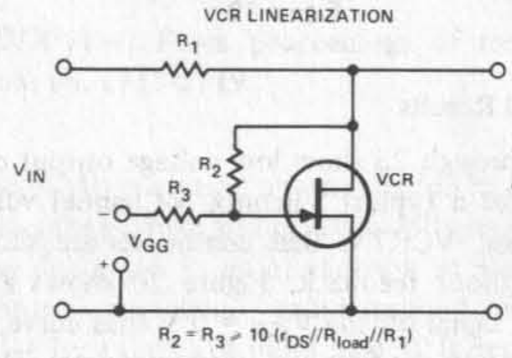


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geqslant 10\ [R_1 \,||r_{ds}\,(\max)\,||R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)}\,||R_L$ to $[(r_{DS(on)}\,||R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \ \frac{r_{DS(on)}\,||R_L}{(r_{DS(on)}\,||R_L) + R_1} \ . \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

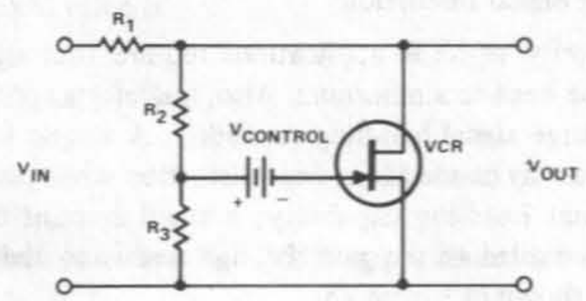


Figure 19

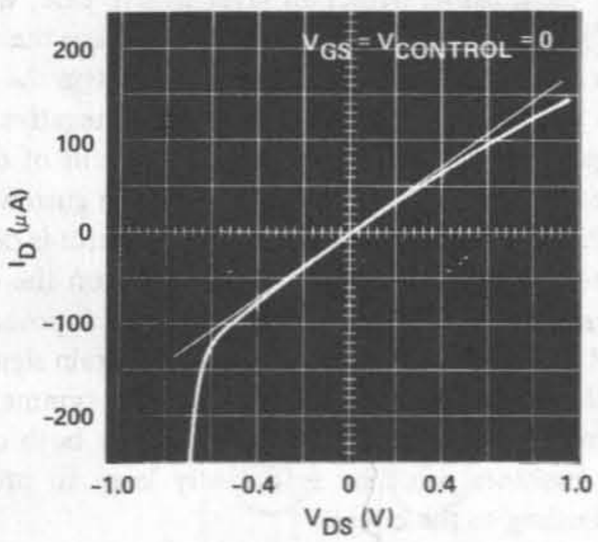
Experimental Results

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the V_{GS} = 0 V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

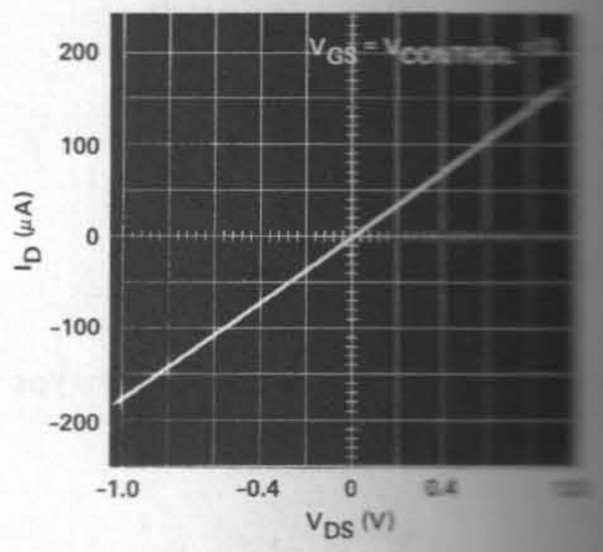
The forward-biased gate-drain PN junction [illegible] approximately –0.6 V, and bending of the [illegible] apparent in the third quadrant. The photo also [illegible] the comparison between a fixed resistor (the [illegible] superimposed on the bias curve) and the [illegible] in the VCR without feedback compensation; the [illegible] is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown [illegible] the addition of the feedback resistors. Distortion [illegible] reduced to less than 0.5%, and the characteristics [illegible] are now closely comparable to those of a fixed resistor.

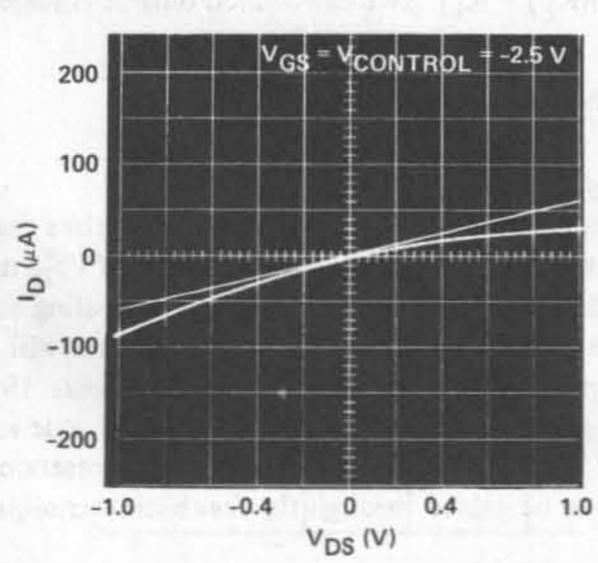
In Figures 22 and 23, the same VCR FET [illegible] shown, with V_{GS} adjusted for higher r_{DS}. No feedback work is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



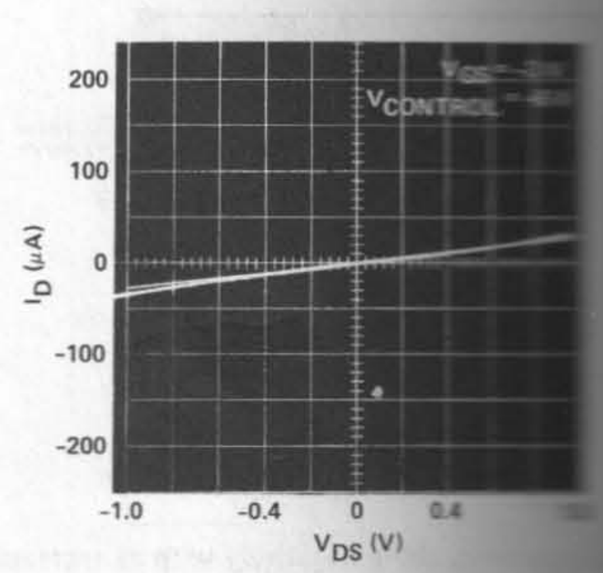
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21



VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23