Siliconix

APPLICATION NOTE

FETs As Voltage-Controlled Resistors

INTRODUCTION

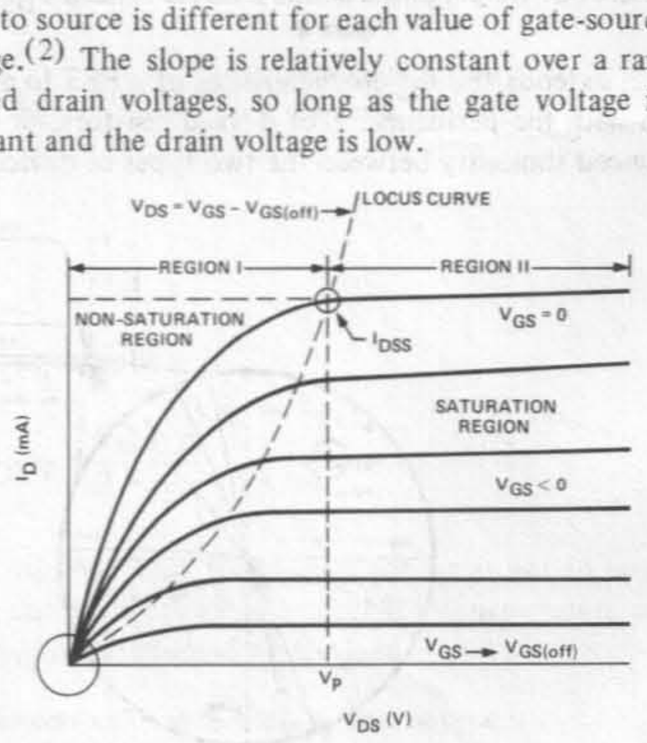
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

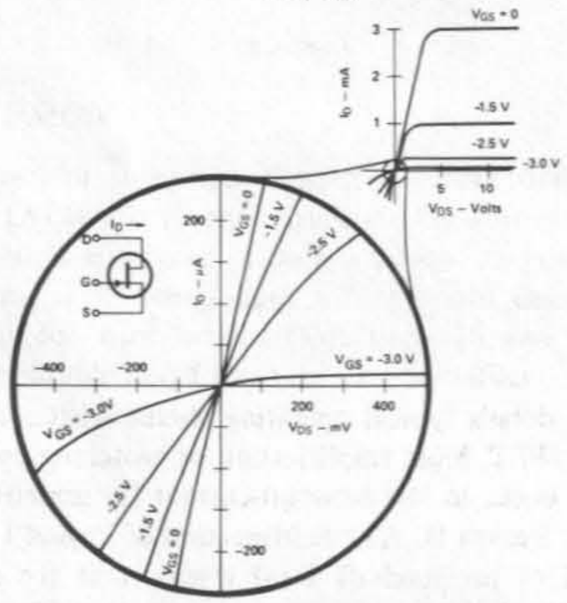


Typical N-Channel JFET Operating Characteristics
Figure 1

Resistance Properties of FETs

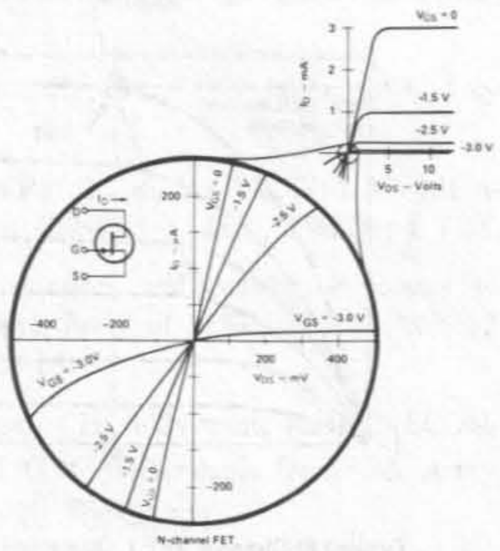
The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.(3)

Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



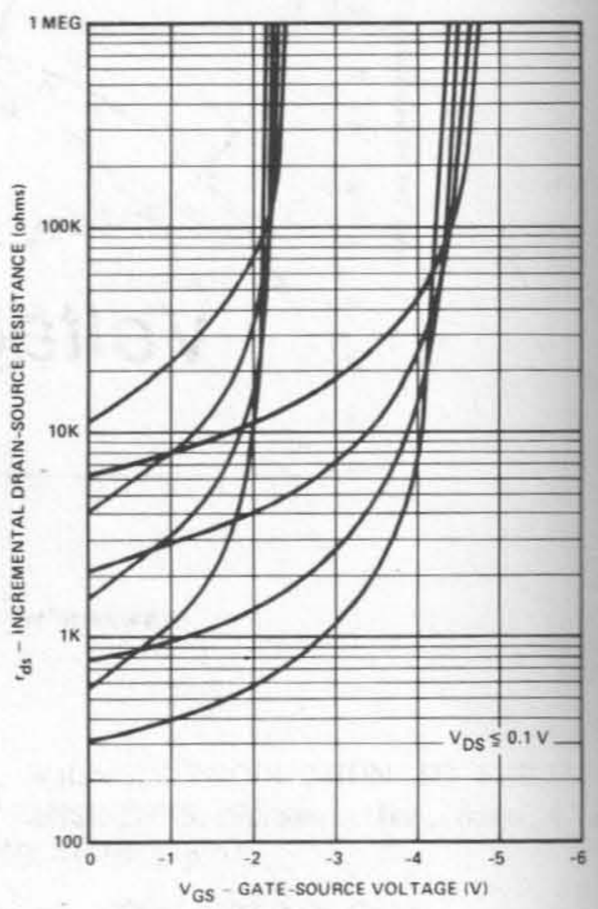
N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.



Comparison of FET and Resistor Characteristics
Figure 3

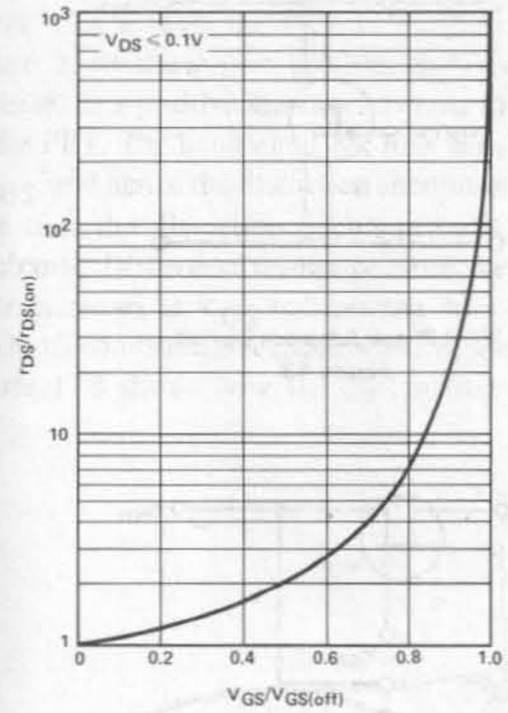
Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.(4) The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefore desirable to convert Figure 4 to a normalized plot. This



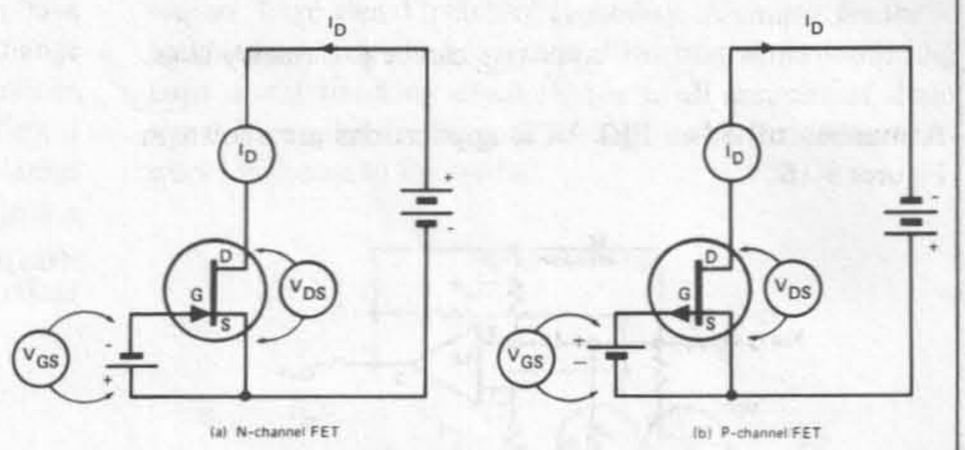
Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of the ordinate is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

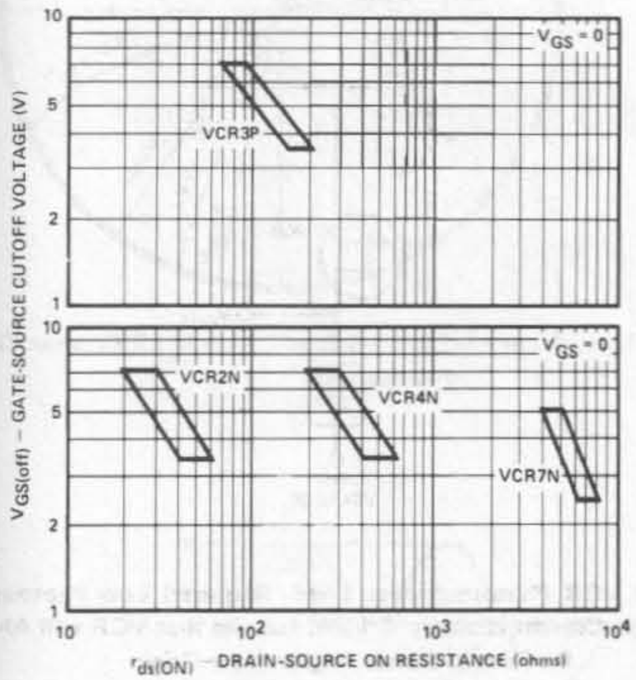
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



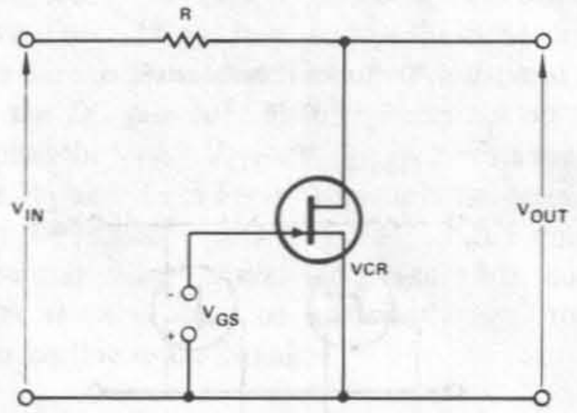
Normalized r_{ds} Data
Figure 5



Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.(5)

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \qquad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \qquad (2)$$

5