

TRIPATH AMPLIFIER LAYOUT GUIDELINES

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Tripath Class-T amplifier drivers offer the designer a nearly complete amplifier solution in a small package. Internal to the Tripath module is the entire driver stage for a bridgeable high-power Class-T stereo amplifier, with component selection and layout optimized for the power level chosen. The components internal to the module have been laid out for the highest possible performance. External to the module, however, there are design issues that must be considered in order to ensure the highest performance from the finished amplifier. This paper addresses those considerations.

Output FET Considerations

A Class-T design benefits greatly when the output FETs operate as closely as possible to their data sheet specifications. To achieve this level of performance, careful attention must be paid to the location and orientation of the output FET's and their surrounding circuitry.

- Keep the FET's (M1 - M4) as close as possible to the output side (pins 20-27) of the Tripath driver.
- When all four of the FETs are located side-by-side on the same panel or heatsink, the "high-side" FET's (those connected to the positive rail) should be located next to one another (in the middle), and the "low-side" FETs should be on the outside. This L-H-H-L arrangement works best for routing of power and signals from the module.
- The .1uF decoupling capacitors (C18 – C21) on the output FET's **must be as close as possible** to the FETs. Keep the lead lengths of the FETs and the capacitors short. Attaching the capacitors to the FET leads is an optimal implementation. This will reduce the ringing of the FETs and greatly improve the reliability of the design. If the capacitors are as much as two inches away from the FETs, they may be useless.
- Similarly, the diodes (D1 - D4) on the output FETs should be located as close as possible to the FETs themselves. Lead and trace lengths are important here, as well. Keeping the diodes close to the FETs will minimize overshoot.

A layout which locates the output FET's on the edge of the board may run into some constraints when it comes to signal routing. Locating the FETs in some central location on the PCB will likely provide for better routing. Locating the FETs on the backside of the board is a good way to provide for easy panel and heatsink mounting.

Signal Routing

Some of the signals in a Class-T design are sensitive to noise/crosstalk. These nodes have been specially designated as “Kelvin” connections in the reference schematic, meaning that the connections to these nodes should be made directly from component to component, with no other components sharing that connection. Other potentially sensitive nodes are described below.

- Do not connect digital and analog grounds at any point external to the Tripath module. These nodes have been optimally connected internal to the module.
- All analog ground lines should be routed separately back to pin 1 on the module.
- The current sensing resistors (R8 and R3 on the schematic) should be “Kelvin” connected back to their appropriate pins on the module. These are sensitive nodes, and while (ostensibly) at V+ and V-, using these lines for any other purpose could inject noise sufficient to cause false overcurrent conditions or prevent true overcurrent operation.
- The overcurrent sense lines (pins 13/14 and 33/34) should be taken directly from the ends of the overcurrent sense resistors and not from any other points on the node(s). The overcurrent circuitry relies on being able to reliably read the drop across this fixed resistor value. Connecting the sense lines to any other point on the node will compromise the accuracy of this reading.
- The overcurrent sense lines (pins 13/14 and 33/34) should be routed in parallel from the sense resistors back to the module. This will minimize the level of differential noise seen by the sense pins.
- The feedback circuits (pins 18 and 29) should be connected to the output filters DIRECTLY at the inductor, and not at some other point on the same node. If the feedback is taken from some point in between the output FET's, for example, the crosscurrents between the FETs will create noise in the feedback signal.

The gate drive loops should be minimized in area. These loops are formed by the traces connecting the outputs of the Tripath module (pins 20, 22, 25, and 27) to the output FET gates (including the gate resistors) and the FET's source returns to the Tripath module. Tight loops here are important to minimize ringing at the gates of the FETs.

Other

- The overcurrent sense resistors (R3, R4, R7, R8) should be of a non-inductive construction. An inductive resistor will interact with the bypass capacitors and will not yield an accurate peak current value.
- Make sure that the gate resistors (R10 – R13) are appropriately sized. Although there is little DC present in the gate circuit, the high-frequency charge/discharge cycles of the gate capacitance requires a gate resistor with a power rating of least 1Watt.
- A good approach to the initial design is to first route the Gate and Source connections, and then the overcurrent nodes. Beginning with other componentry or circuits will compromise the layout of these two critical areas.