
How to improve the robustness of operational amplifiers against electromagnetic interferences (EMI)

Introduction

In such application as wireless infrastructure, switching power supply AC motor, or even microcontroller electronic designers must deal with Electromagnetic Interference (EMI). Even if the EMI concept is well known it is often considered only when the final application does not work as expected on paper, sometimes it is too late to add corrections.

Wireless devices increase day by day, and thus, EMI is increasingly part of the electronics system. This application note reviews EMI sources and discusses classical, but sometimes forgotten tricks, to improve the robustness of the operational amplifiers against electromagnetic interference. It also addresses the new generation of ST, EMI hardened op amps.

1 EMI origin

Electromagnetic interference can be considered as frequency parasitic largely outside the bandwidth interest of the op amp, which can affect the performance of the device.

This EMI can affect the behavior of an [operational amplifier](#) either by radiation or by conduction through PCB tracks.

The radiated EMI often becomes a conducted EMI as it can irradiate a PCB and use the tracks to flow directly inside the op amp.

Sources of perturbation are numerous, and generally come from the radio frequency systems working from several kHz to GHz, but also from transient signals with very sharp edges. Effectively, switching regulators, motors, or even 50 Hz can be considered as a source of EMI.

Generally, coupling is what allows the source of EMI to have an impact. There are several types of coupling.

An inductive or capacitive coupling can be considered when the signal applied on a conductor induces a parasitic signal to another.

In addition, a variable electric field can induce a current in a conductor, and even a variable magnetic field can induce a voltage drop in a conductor.

It is important to keep in mind that the impedance of a conductor is never null and a small current flowing through it automatically generates a voltage drop.

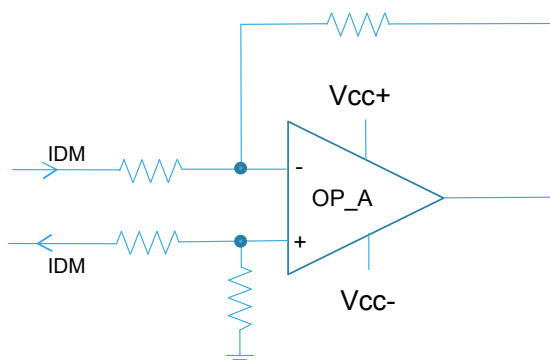
2 Differential and common mode interference

The interference issue appears most when the interconnects are long and the signal level low.

The interference can be picked up either from common mode or differential mode.

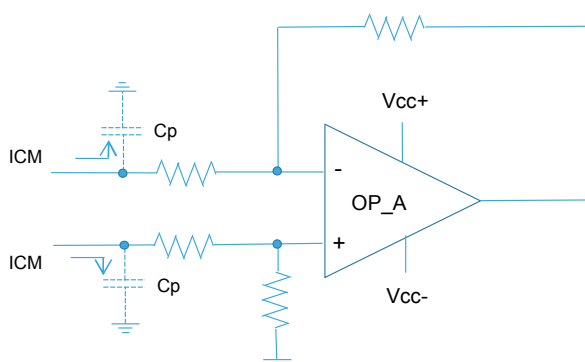
Differential mode is the normal way to transmit a signal, and the current, called IDM, flowing in each wire of the pair in an opposite direction. The magnetic field generated by each wire has the same amplitude but opposite polarity, so they cancel each other out.

Figure 1. Differential mode



Common mode current ICM flows in both wires in the same polarity and returns to GND via parasitic capacitance C_p . Contrary to differential mode, the electromagnetic field generated by each wire of the pair cannot be canceled out and so the common mode signal generates interference along the cable. It is generally considered as the worst case for EMI issues.

Figure 2. Common mode



3 What is the impact of EMI on an op amp?

Op amps using a bipolar technology are very sensitive to EMI as the diode of the junction p-n acts as a rectifier and transforms the HF parasitic signal in a DC voltage. This unwanted DC signal is then amplified and can be considered as an offset error, as well as a V_{io} , which is an intrinsic parameter of the op amps. We can determine that CMOS op amps are less sensitive to the EMI, which may be true, but unfortunately the input ESD protection diode acts in the same way.

A domain of EMI where the op amps are the most sensitive is the UHF band from 300 MHz to 3 GHz. The frequency band of 400 MHz is, for example, dedicated to weather, radar, mobile radio, mobile satellite, space operation.

Let us have a look of the effect of such parasitic frequency on op amps. The radiated EMI becomes the most part of the time conducted through the wires, or PCB tracks. In order to have a reproducible test, a sinus signal superposed to a burst signal is sent directly on the input pin of the op amp.

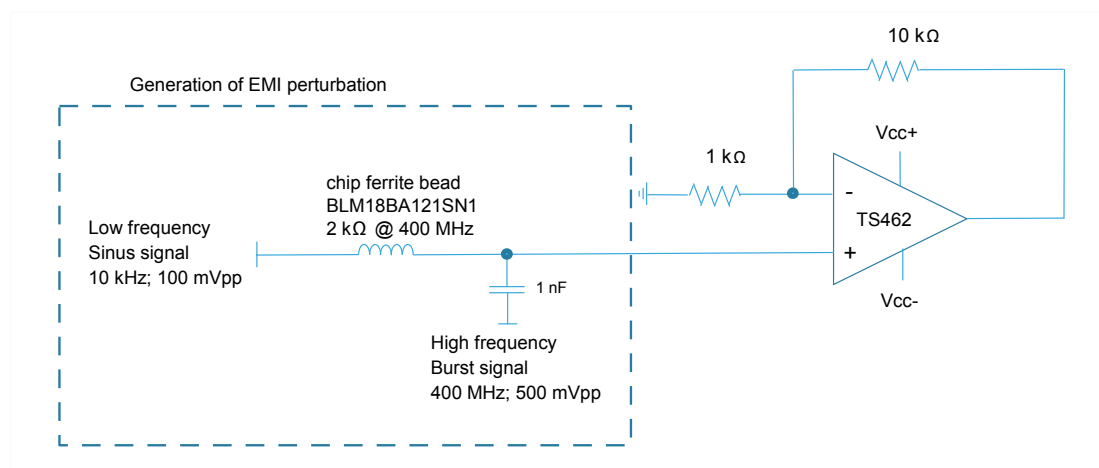
The schematic in Figure 3 describes the application test. A non-inverting amplifier schematic is used with a gain of 11. An input signal of 100 mVpp and 10 kHz is applied on the non-inverting input pin. A parasitic signal, emulating an EMI source, is also injected on the input pin +. This EMI perturbation is a square burst signal of 400 MHz and 500 mVpp. The sharp edge of the parasitic signal is very aggressive and generates a high level of EMI perturbation.

This noisy signal is applied to the victim, TS462, a dual bipolar op amp.

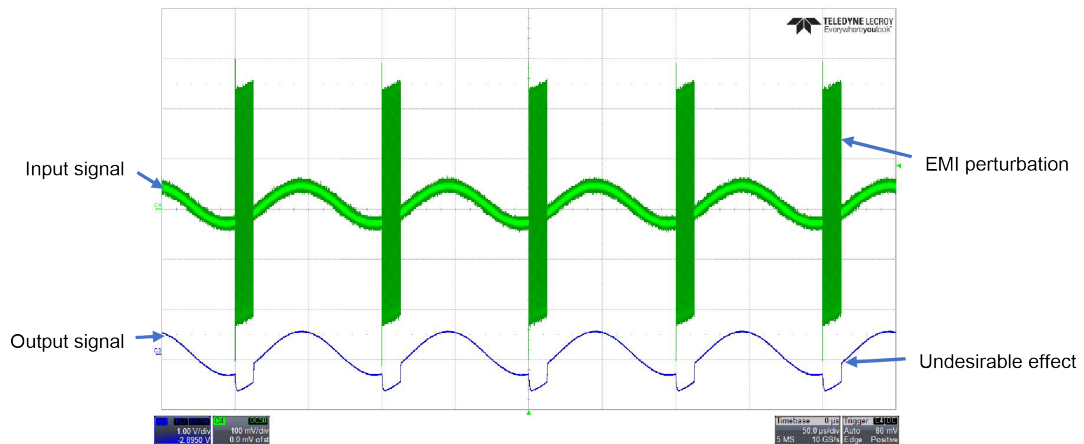
Common mode noise is the worst case in terms of perturbation. But an ideal op amp should be able to reject this perturbation if we consider that its own CMRR vs. frequency is infinite. It is unfortunately wrong, even if most op amps can show a good rejection of common mode noise, this parameter gets worse while the frequency of the perturbations increases. Above 1 MHz very few op amps are able to completely reject common mode noise. In this case, a filtering solution must be found.

3.1 Common mode perturbation for a non-inverter schematic

Figure 3. EMI test with a bipolar op amp



The results are described on the scope probe, see Figure 4. EMI effect on bipolar op amp without any protection, and show an output signal distortion.

Figure 4. EMI effect on bipolar op amp without any protection


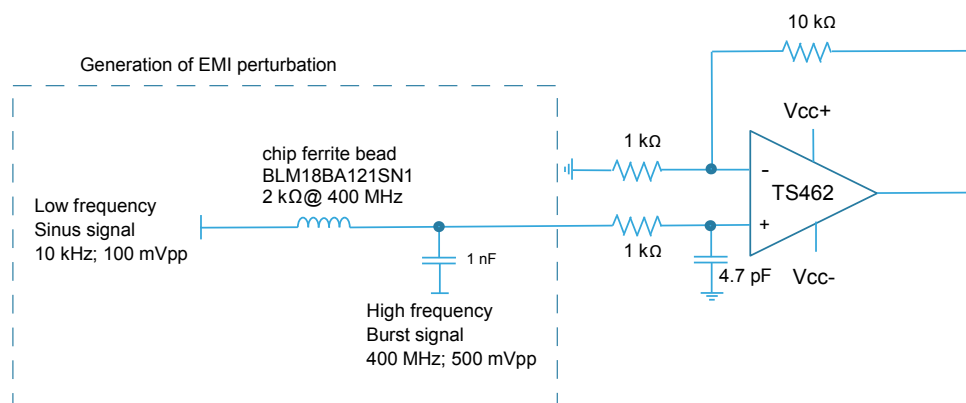
A simple and classical solution is to use an external filter in order to protect the inputs of the op amp and avoid any high frequency entering into the devices. The filter should certainly be placed as close as possible to the input to protect.

The low-path filter can be done as described in Figure 5. EMI test with a bipolar op amp and RC filter with a resistance and a capacitor.

The cutoff frequency of such filter is defined by equation (1):

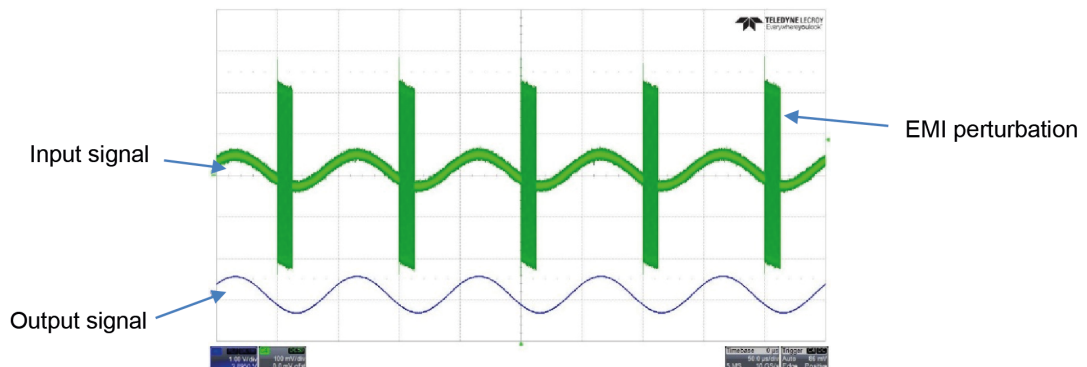
$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} \quad (1)$$

The gain bandwidth product of the TS462 is 12 MHz; as the gain is set to 11, the maximum input signal frequency may not exceed 1.1 MHz in order to not be attenuated. It is important to take high margin when a low-path filter is calculated. In this case, the cutoff frequency is fixed to 33 MHz to not attenuate the input signal. To equilibrate the input bias current on both input pins of the op amp, the value of the filter resistance is the same as the input resistance of the non-inverting pin, here 1 kΩ. So, following Eq. (1), the capacitor of the low-path filter is calculated at 4.7 pF.

Figure 5. EMI test with a bipolar op amp and RC filter


The results are illustrated by the scope screenshot, Figure 6. EMI effect on bipolar op amp with RC filter, and show that the output of the op amp is no longer distorted and thus the input RC filter has removed the EMI signal.

Figure 6. EMI effect on bipolar op amp with RC filter



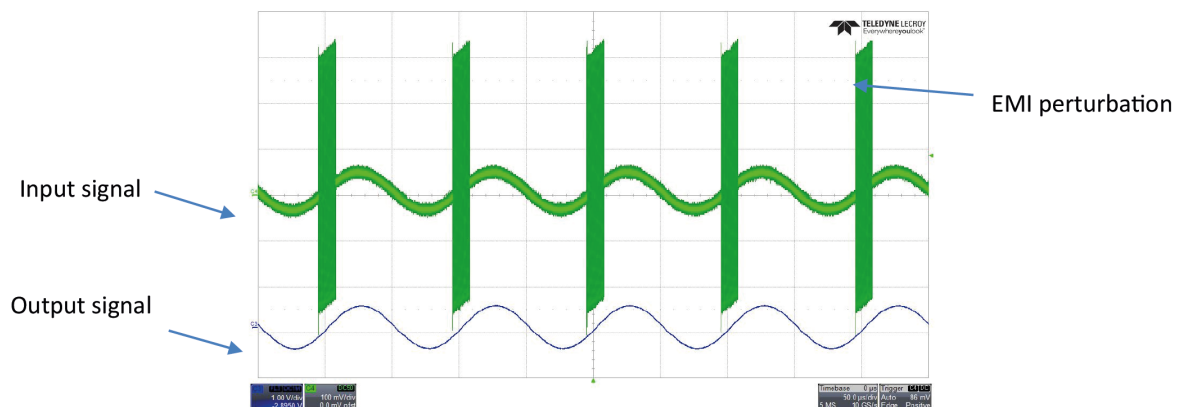
Another option is to use the latest generation of amplifier developed by STMicroelectronics, which are EMI-hardened. Effectively, this kind of op amp integrates a filter able to reject high frequencies from several hundred MHz up to several GHz.

The section on EMI Hardened describes in more detail this kind of op amp.

Anyway, thanks to this EMI-hardened op amp, the capacitance added on the schematic, [Figure 5. EMI test with a bipolar op amp and RC filter](#), can be removed.

For the following test, the TSV632 op amp is used.

Figure 7. EMI effect with the TSV632 EMI-hardened op amp and without RC filter



The results described by the scope screenshot, [Figure 7. EMI effect with the TSV632 EMI-hardened op amp and without RC filter](#), show that the output of the op amp is no longer distorted even without any RC filter (schematic of [Figure 3. EMI test with a bipolar op amp](#) has been used for this test).

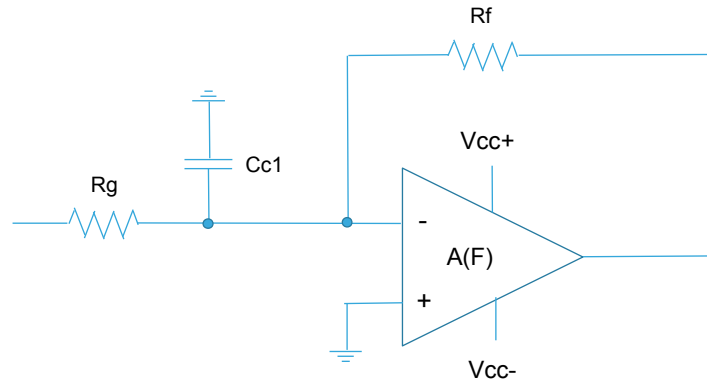
3.2

Common mode perturbation for an inverter circuit

When the amplifier is used in an inverter the protection against EMI remains the same. Adding a capacitance as described in the schematic [Figure 8. Filtering of an inverter schematic](#) helps to protect the op amp.

But in this inverter configuration, as the capacitance is placed on the inverting pin of the op amp, special care must be taken on the stability of the system.

Figure 8. Filtering of an inverter schematic



Let us analyze the open loop transfer function (2) of the schematic described in [Figure 8. Filtering of an inverter schematic](#):

$$-A(F) \frac{Rg}{Rg + Rf} * \frac{1}{1 + j\omega \left(\frac{Rg \cdot Rf}{Rg + Rf} \cdot Cc1 \right)} \quad (2)$$

Where A(F) is the open loop transfer function of the op amp.

Cc1 creates a pole, which could lead to instability.

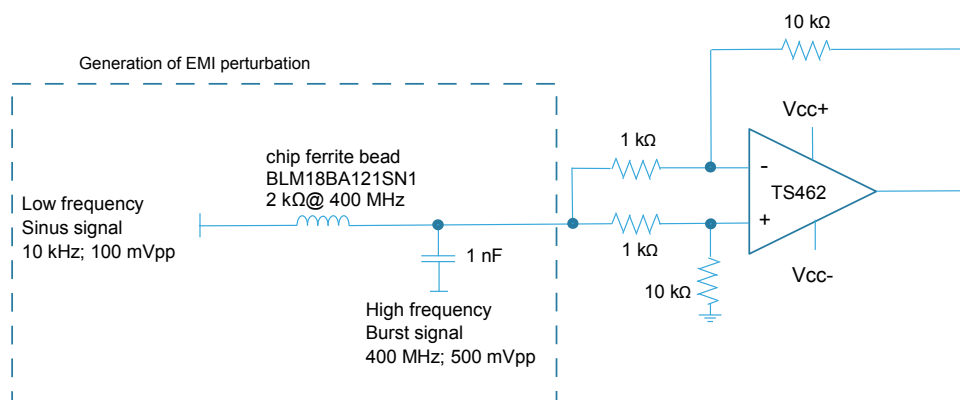
$$fp = \frac{1}{2\pi \cdot \frac{Rg \cdot Rf}{Rg + Rf} \cdot Cc1} \quad (3)$$

In addition to this pole, we have to consider the low-frequency pole of the open loop transfer function of the op amp.

$$fop = \frac{GBP}{Avd} \quad (4)$$

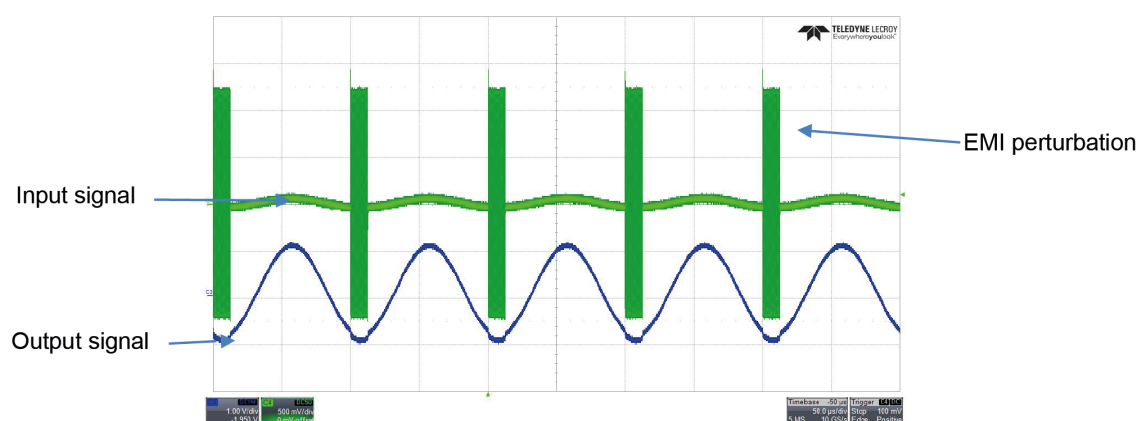
Therefore, the bode diagram of this system can be plotted as depicted in [Figure 9. Bode diagram of the open loop transfer function](#).

Figure 10. Common mode EMI test with a bipolar op amp configured in differential mode

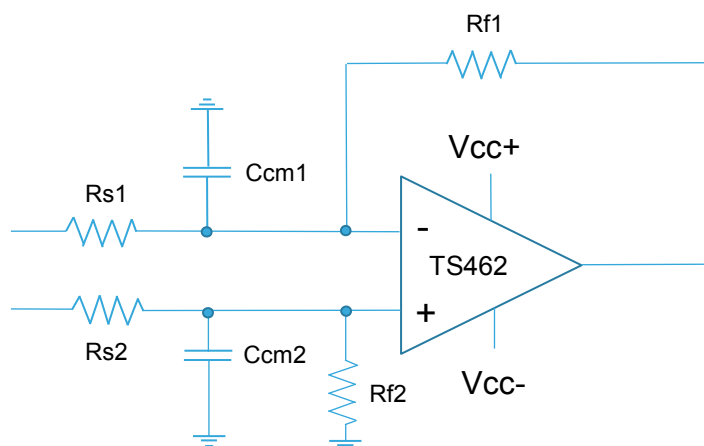


The results shown by the scope screenshot in Figure 11. Common mode EMI effect on bipolar op amp in differential mode without any protection exhibit a distorted output signal.

Figure 11. Common mode EMI effect on bipolar op amp in differential mode without any protection



Firstly, it is important to filter the common mode by adding a capacitor Ccm1 and Ccm2 as described by Figure 12. Common mode capacitance.

Figure 12. Common mode capacitance


It is recommended to place the same low-path filter on each input of the op amp, in order to equilibrate the two inputs.

Unlike an instrumentation amplifier, the circuit is not symmetric. The op amp is generally not able to properly feed back the information at a frequency over the stress. As a result, a common mode capacitor does not fully reject the RF signal by the same ratio on each side. In addition, their matching also acts in the same way. So, they do not kill the differential EMI stress.

Moreover, as seen previously, using high value capacitances can cause instability of the op amp.

So, it would be better to use a lower value of capacitances. There is a tradeoff.

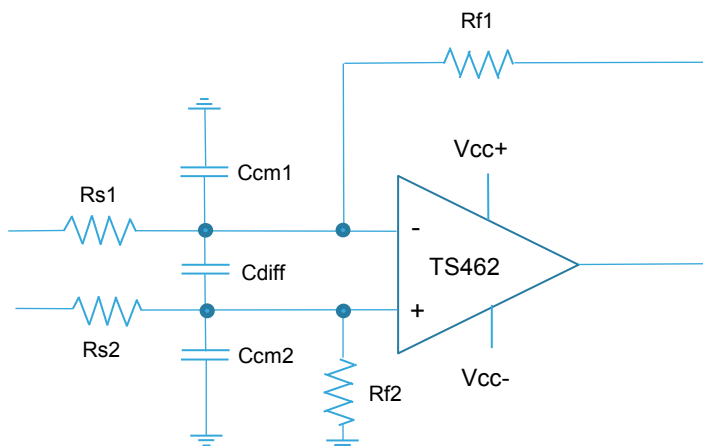
For better EMC performance, it is important to use capacitance with a low ESR.

Another point that can be considered is the equipotential of the ground plane. Effectively, if the impedance of the ground of the Ccm1 and Ccm2 is slightly different, the common mode filtering is not totally equal as well. Resulting, as seen previously, in an AC error in differential mode.

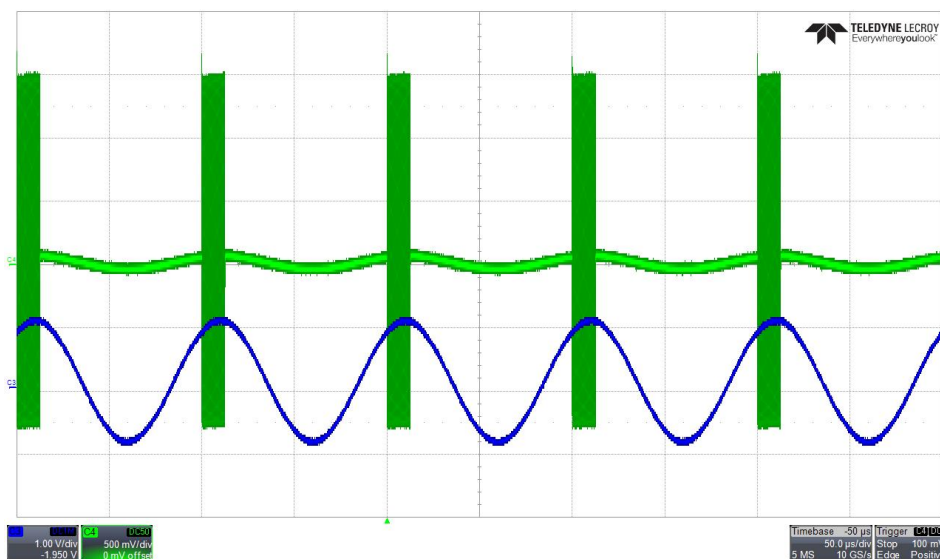
The solution to compensate these points is to add a differential capacitor Cdiff between the two inputs of the op amp. The impedance of Cdiff should be largely higher than the impedance of the Ccm capacitances in order to have a good impact on the filtering. Therefore, the differential mode capacitance is chosen five to 10 times higher than the common mode capacitance.

The capacitances should certainly be placed as close as possible to the input pins.

The schematic below describes how to correctly protect the input pins of a differential op amp.

Figure 13. Common mode and differential capacitance


With such an input filter the TS462 op amp is now immune against EMI as described by the following scope screenshot, see Figure 14. EMI effect on bipolar op amp in differential mode with RC filter.

Figure 14. EMI effect on bipolar op amp in differential mode with RC filter


3.4

Application example

EMI radiation can impact a device through an input or output pin.

The PCB layout is of course essential for the robustness of a system, and we outline in the section “Printed circuit board layout” some simple but important rules to improve the robustness against EMI.

Let us take the example of an op amp used as a current source described by Figure 15. Op amp used as current source. The op amp (LM2904) is used in follower configuration and the NPN transistor (2N222) is used to provide the necessary current into the load. So, in typical conditions the output V_{out} must be equal to the input voltage, in this case 2 V.

Figure 15. Op amp used as current source

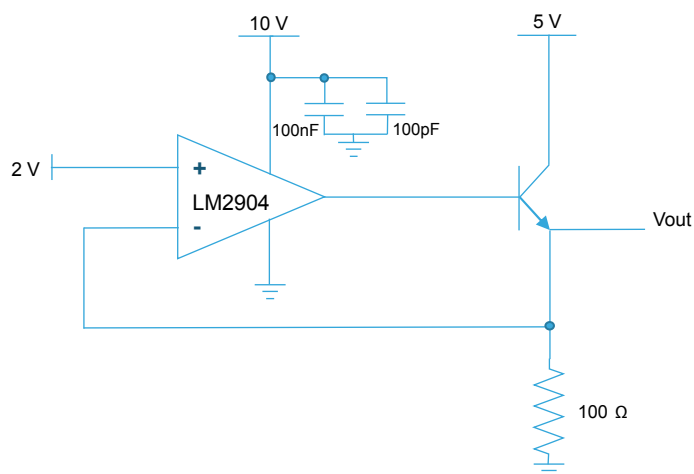
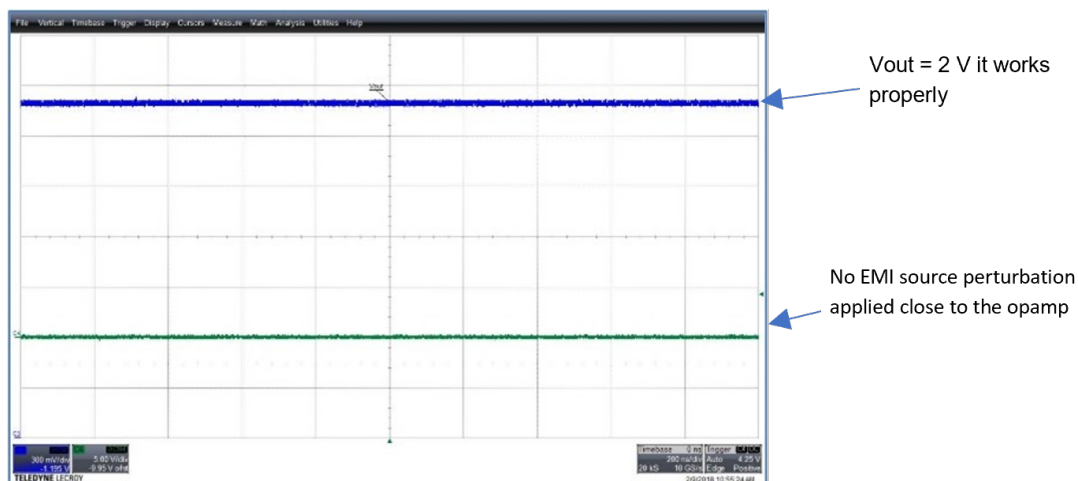


Figure 16. System without any source of EMI

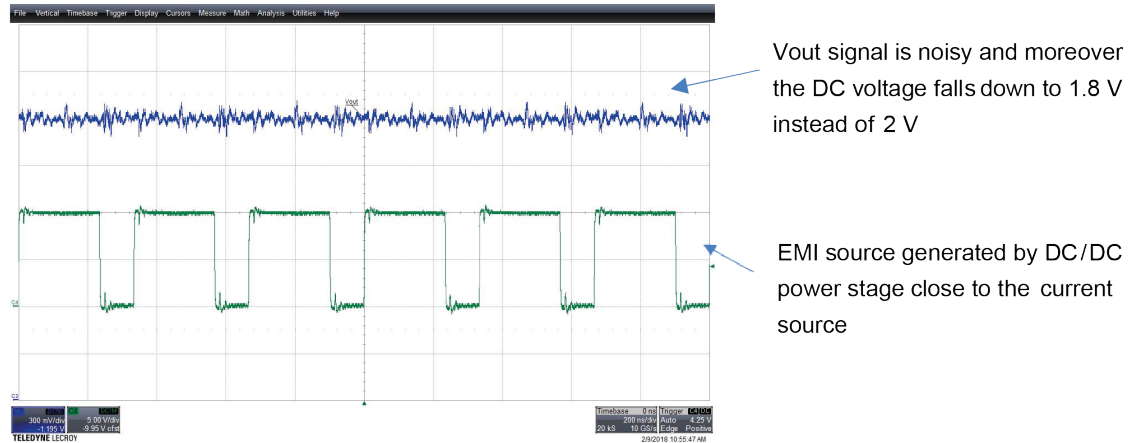


The system is working well as 2 V is measured on the output and, it is stable.

In this example, no particular care has been taken regarding the PCB layout. In the whole application system, the current source is placed very close to a potential source of EMI, a DC/DC power stage generating a square signal of 10 V of amplitude and with very sharp edge of 5 ns.

Figure 17. Output voltage of current source victim of EMI describes the voltage at Vout when the DC/DC power stage is working.

Figure 17. Output voltage of current source victim of EMI



When a source of EMI is placed close to the op amp, we can see that the output becomes distorted. Firstly, the DC value is now wrong (1.8 V instead of 2 V), and the output signal is really noisy.

EMI can enter in the victim device via any pins, and as seen in the previous section, one of the important things is to protect the input thanks to common mode and differential capacitance. The main goal of the capacitances is to present a low impedance at the frequency of the stress. So, the first reflex can be to add a small capacitive value of 100 pF on the input as described by Figure 18. Input filtering.

Figure 18. Input filtering

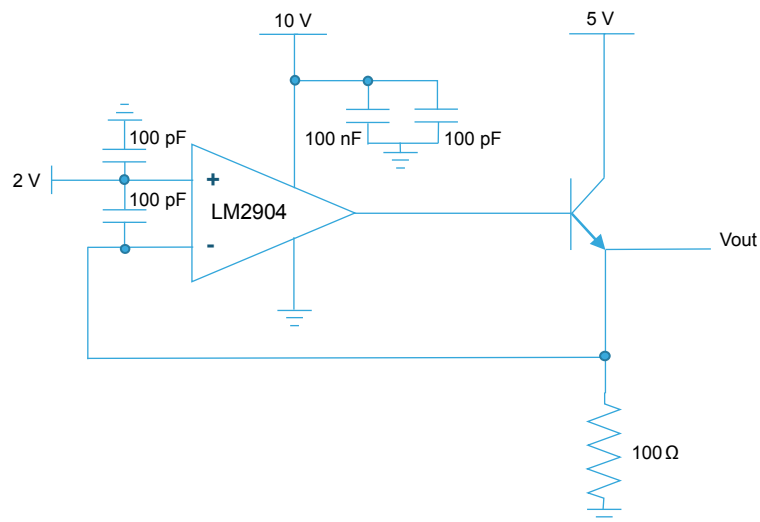
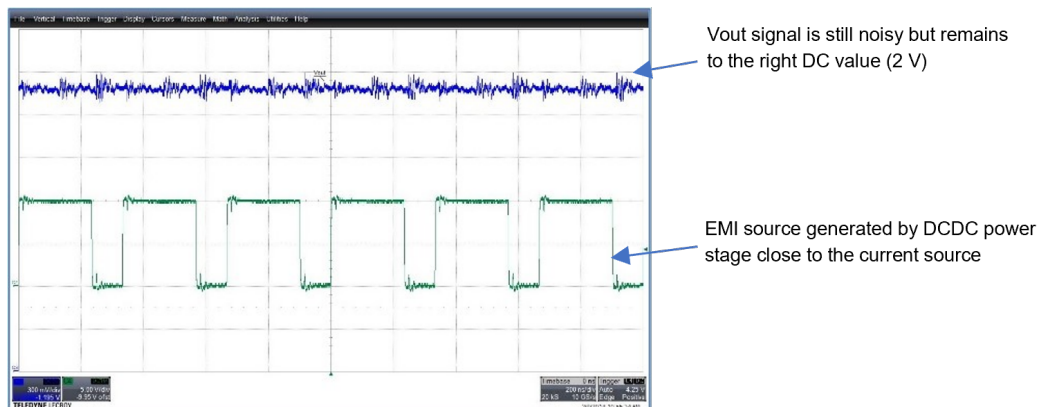


Figure 19. Probe scope result of input filtering



The scope probe depicted in [Figure 19. Probe scope result of input filtering](#) shows the improvement and the effect of such capacitance. Effectively, the output voltage is still noisy, but the average DC value remains good at 2 V. In order to improve the Vout signal, another capacitance can be added to filter more efficiently the output signal, as described in [Figure 20. Output filtering](#).

Figure 20. Output filtering

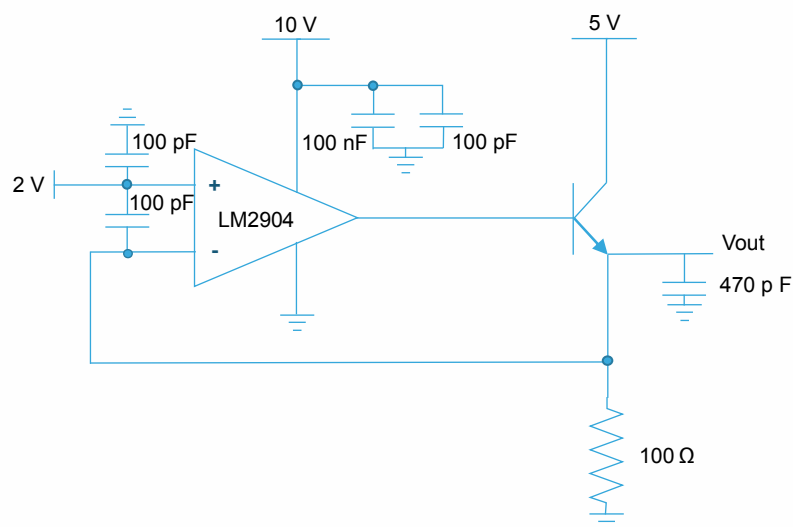
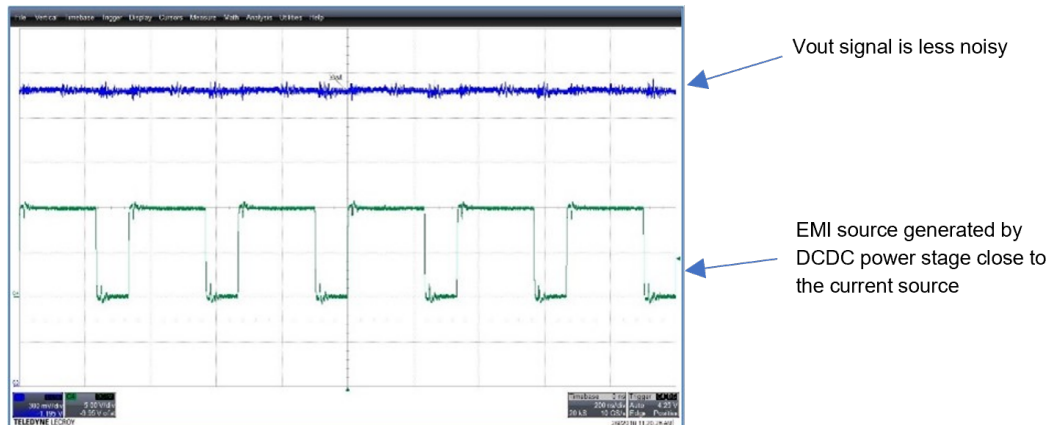


Figure 21. Probe scope result of output filtering

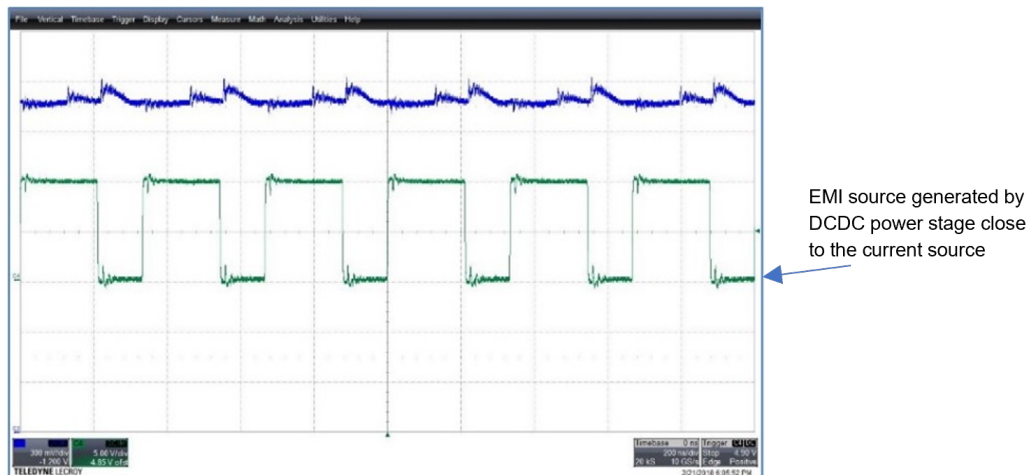


In the case of an EMI issue, a long wire can be a source of the problem. Let us consider the same application but with a long track between the output of the op amp and the base of the transistor. This long wire acts as a trap for the EMI disturbance and then spreads it into devices. Unfortunately, as with many components, the transistor presents some parasitic capacitance impacting the applications with higher frequencies. Effectively, due to the p-n junction, the bipolar transistors present a capacitance between its base and emitter (as well as between base and collector!), and so in high frequency it becomes a path, and the noise can also be present on Vout.

Moreover, the EMI disturbance can enter via the output of the op amp and cause some dysfunctionality.

Figure 22. EMI disturbance with long tracks shows an EMI source applied close to the long track between the op amp output and the base of the transistor. The result is a Vout completely distorted.

Figure 22. EMI disturbance with long tracks



To prevent this issue, it is better to design the traces as short as possible. We can see in Figure 25. Output voltage of current source victim of EMI with a good PCB layout that good layout solves a lot of these issues. But it can also be possible to filter the output of the op amp with a capacitor soldered close to the output of the op amp.

Nevertheless, care must be taken to keep the system stable and functional.

Adding capacitance directly on the output of an op amp is not always a good idea, as it creates a new pole and depending on the value of this capacitance it can cause the op amp to oscillate.

The best solution to isolate the output of the op amp from the capacitance is to add a resistance between them. However, adding a high resistance value can cause a saturation of the op amp, which gives a wrong value. In order to choose this serial resistance correctly, it is important to follow Eq. (7):

$$2V + V_{be} + i_b \cdot R_s < V_{out_max_opamp} \quad (7)$$

Where i_b is the base current of the NPN transistor.

R_s , the serial resistance placed between the op amp output and the NPN base.

$V_{out_max_opamp}$ is the V_{OH} voltage of the op amp.

In this typical application case, 20 mA is drawn into the load ($2\text{ V} / 100\ \Omega$), so it can be considered that the collector current $I_C = 20\text{ mA}$.

The 2N222 transistor used in this condition presents a gain β of 200, so the base current can be easily deduced, $i_b = 100\ \mu\text{A}$ ($I_C = \beta \cdot i_b$). $V_{be} = 0.7\text{ V}$.

The LM2904 op amp used is not high rail and overtemperature the V_{out_max} cannot exceed $V_{CC} - 2\text{ V}$. So, in this case let us consider that $V_{out_max_opamp} = 8\text{ V}$ ($10\text{ V} - 2\text{ V}$).

So, R_s max. must be lower than $53\text{ k}\Omega$.

Regarding the stability point of view, it is largely enough.

In Figure 23. V_{out} with a filter on the op amp output the 22 pF allows to have a low impedance on the output of the op amp at the EMI frequency. Additional R1 and R2 can be added.

Figure 23. V_{out} with a filter on the op amp output

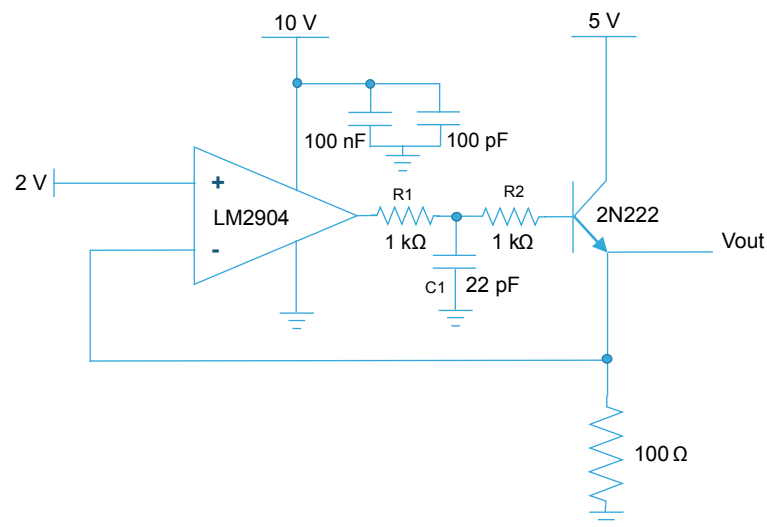
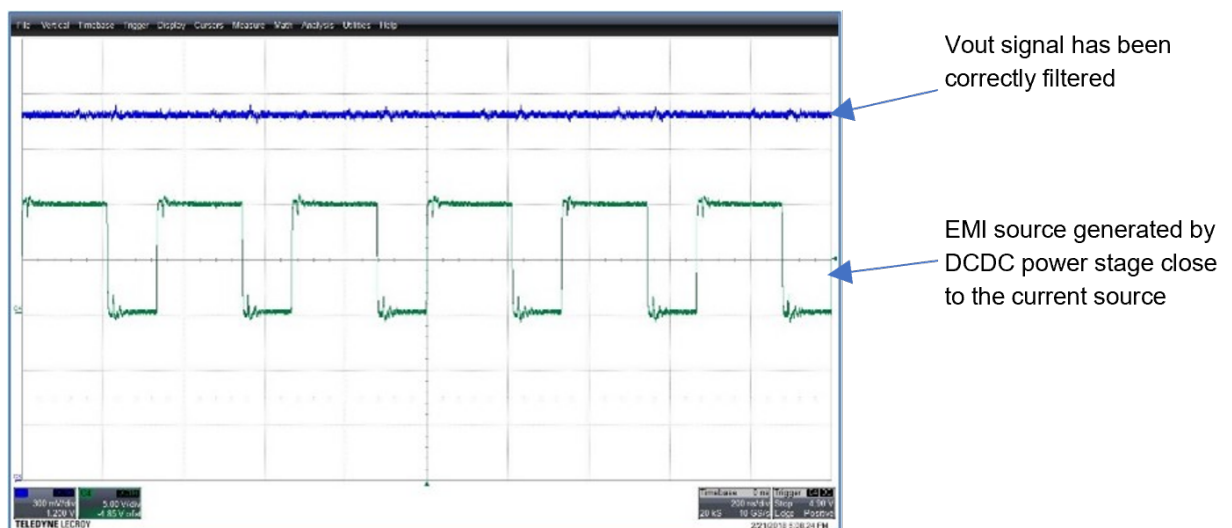


Figure 24. Result on V_{out} of RC filter

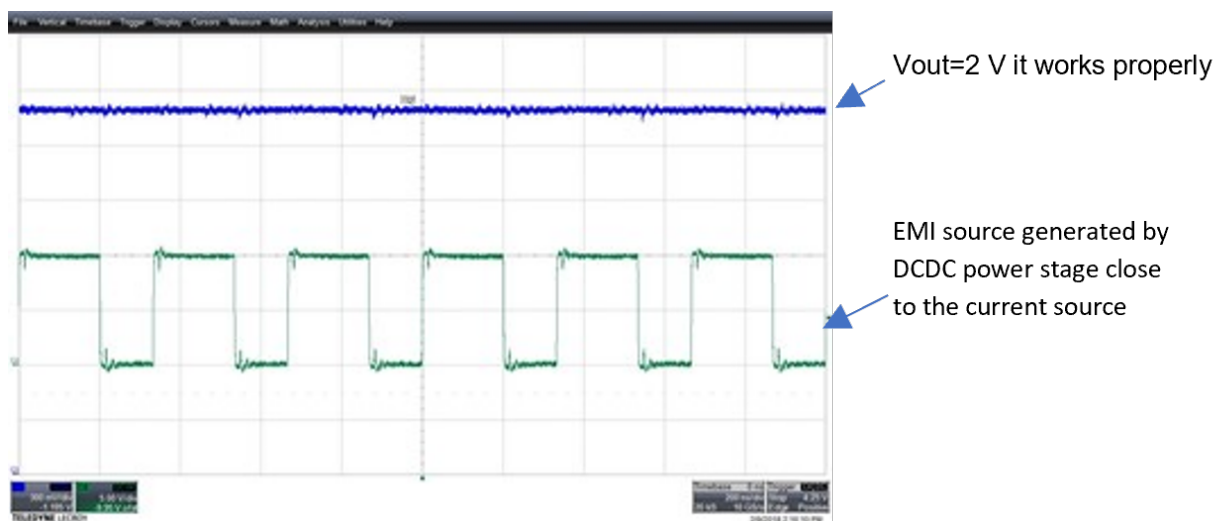


3.5 Special care taken at PCB level

In the following section the same test has been realized, but special care has been taken during the design of the board layout. Effectively, a dual layer board made with FR-4 material has been used, and the ground plane has been designed on both sides of the board. Moreover, the tracks have been designed as short as possible. Only the decoupling power supply capacitance has been used and placed extremely close to the op amp.

In the figure below we can see that the PCB layout plays an important role in the robustness of EMI, as we can effectively see that with no additional capacitors on input and output. The output is not disturbed by any high frequency.

Figure 25. Output voltage of current source victim of EMI with a good PCB layout



4 Printed circuit board layout

PCB layout is generally an accomplishment of an ingenious schematic, but sometimes due to production constraints, not enough attention is paid to that step. A good layout can represent 80% of the robustness of an application with regard to EMI disturbance. The PCB should be thought of as a component itself in the realization of a design.

In this section, some well-known rules are recalled in order to avoid issues linked to a parasitic environment.

The performances of an IC in an application are dependent on a number of factors, these include: mechanical design, printed circuit board design and layout, components, connectors, and cables. Good performance at IC level does not guarantee good performance at system level.

PCB traces

EMI propagation from cables to IC (and vice versa) cannot be avoided.

In addition, EMI can couple directly with PCB traces, flat cables, and IC package lead frame; the higher the interference frequency the shorter the length of the wiring at which parasitic coupling is effective.

Effectively, the PCB trace can certainly be seen as a resistive path, but also as an inductive component. Its impedance can be simply described by the following equation:

$$Z = R + jL\omega \quad (8)$$

So, at low frequency, the traces act as a resistance but with increasing frequency, impedance increases and acts as an antenna, which catches and then conducts any RF or EMI noise. The inductance of the PCB trace is linked to its length. This is why it is important to keep the traces as short as possible in order to limit the antenna effect at high frequencies.

Another important point regarding the antenna, is what we generally call loop antenna, especially a risk when no ground plane is used but only track even for the ground. So, a loop can be created by the ground traces and the signal traces. The loop antenna is, unfortunately, extremely efficient in catching undesired high-frequency signals, therefore, in order to reduce this effect, a ground plane on the PCB is highly recommended.

It strongly reduces the area of the loops.

Here is a suggestion to route a dual op amp.

Figure 26. Dual schematic example

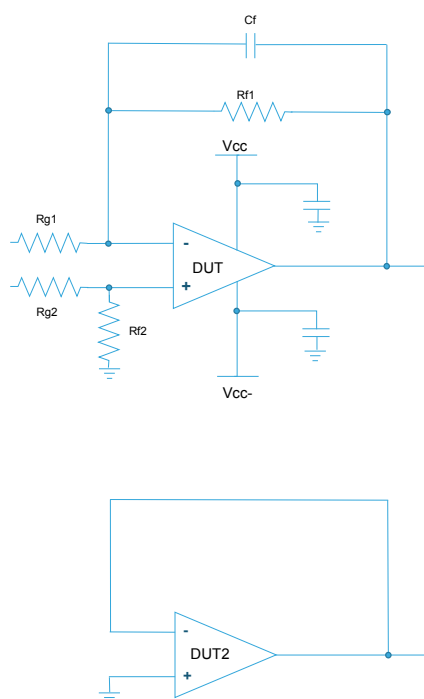
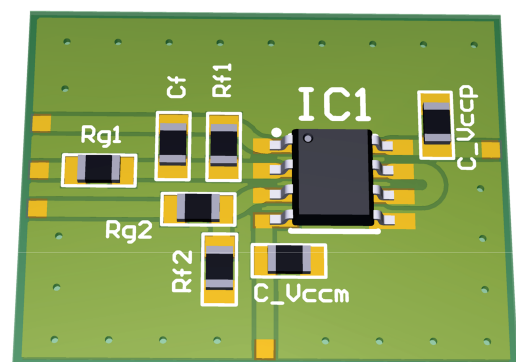


Figure 27. Dual layout example



Grounding

Ground is an essential part of a good PCB realization. The first and simplest rule to respect is to separate the ground of the digital and analog parts. The currents must find a return path and ground is dedicated for that. So, separate ground does not mean having two different grounds, but they must be common.

In the case of a multilayer board and separate ground between digital and analog, it is also important not to superpose an analog ground plane and a digital ground plane. Because the two planes can create a capacitance and the noise generated by the digital can in this case pollute the analog ground.

What is true for the ground is true for the signal. It is better to avoid having digital signal close to the analog portion. Generally, digital is much noisier than analog due to the fast transition that can happen, which can generate some EMI noise. So, as for the ground, it is better to avoid overlapping the digital signal and analog signal in the case of multilayer boards.

Multilayer

The most cost effective solution is obviously the single layer, but unfortunately it is also the worst solution for EMI robustness. The preference is a double side PCB with one side used as a ground plane. It gives a major advantage to reduce the impedance of the ground connection and distributes the capacitance, reducing the impact of EMI. The ground plane can also be seen as a shield, which protects the other side against the radiated noise. If there is enough space on both sides of the board, two ground planes can be used, one on each layer. To minimize parasitic impedance over the entire surface, a multivias technique that connects the bottom and top layer ground planes together in many locations is often used.

The multilayer technique (at least four layers) is the most efficient in terms of EMI robustness. Ground plane and power plane can be traced in the middle layer in order to keep a good capacitance distribution between the planes.

5 EMI-hardened op amp

For several years STMicroelectronics has hardened all new generation op amps against EMI. To quantify this robustness the EMIRR (Electromagnetic Interference Rejection Ratio) parameter has been added in the datasheet. As explained in the section “What is the impact of EMI on an op amp?” RF interfering signal can be converted into a DC signal due to p-n junction or diode, which rectifies the EMI signal and generates a DC signal causing an unexpected error on the output of the op amp.

The EMIRR definition is given by the following formula:

$$EMIRR = 20 \cdot \log\left(\frac{V_{RF}}{|\Delta V_{io}|}\right) \quad (9)$$

Where V_{RF} is the amplitude of the applied unmodulated R_F signal. The chosen standard level for V_{RF} is -10 dBm (100 mVp).

ΔV_{io} represents the input voltage shift. It is the difference between the op amp's input offset voltage (V_{io}) without any EMI signal injected and the op amp's V_{io} when an RF signal is applied.

The EMIRR is expressed in dB, and the higher the EMIRR value, the better the op amp EMI's robustness.

EMIRR measurement

Each pin of the op amp can be tested for EMIRR.

In the following example only the input pin is tested as it is generally the most sensitive part of the circuit.

To test the positive input pin, we use the simplest configuration for an op amp: the follower mode, as described by [Figure 28. Configuration for EMIRR test non-inverting input](#).

The RF signal is applied on the non-inverting pin and the V_{io} is directly measured on the output pin.

To test the inverting input, a gain configuration of -1 can be used as described by [Figure 29. Configuration for EMIRR test on inverting input](#). The V_{io} variation is also measured on the V_{out} pin but in this case the input offset voltage has to be divided by two.

Figure 28. Configuration for EMIRR test non-inverting input

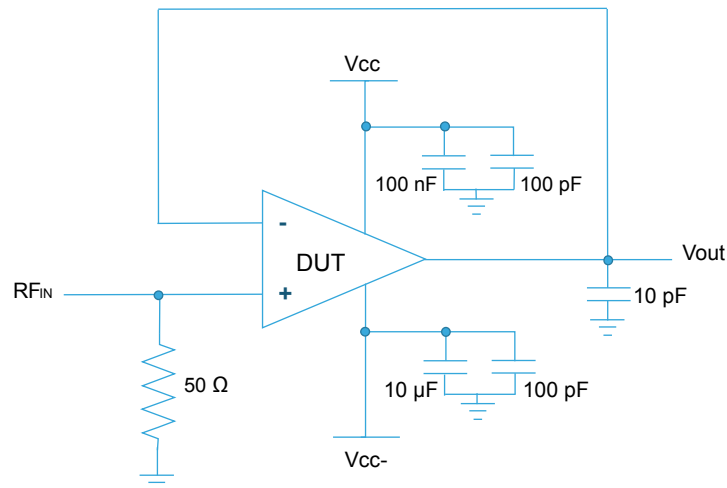
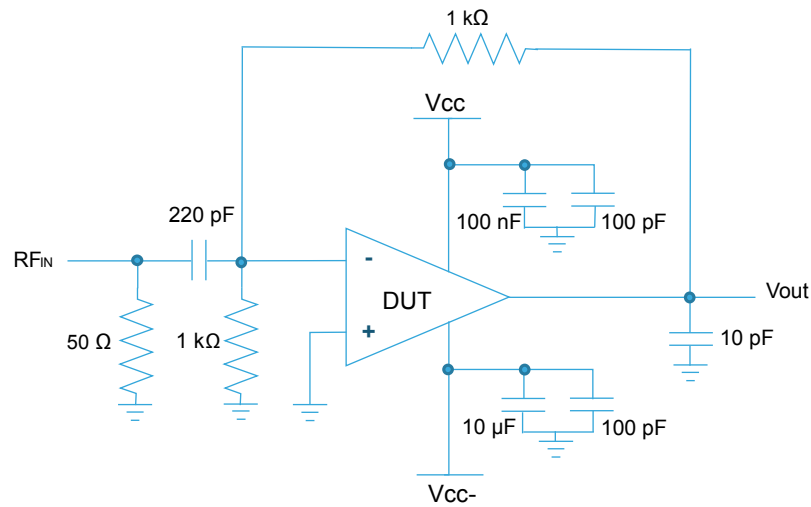


Figure 29. Configuration for EMIRR test on inverting input


The following graph shows the results of EMIRR robustness on the two op amps having the same schematics except for input EMI hardening.

The **TSV621**, a single op amp, is not EMIRR hardened, while its twin, the **TSV622** a dual op amp, has been specially designed with EMI protection.

Figure 30. EMIRR result on PIN+ describes the robustness of the non-inverting input pin against RF signal, and **Figure 31. EMIRR result on PIN-** describes the robustness of the inverting input pin when an EMI signal is applied.

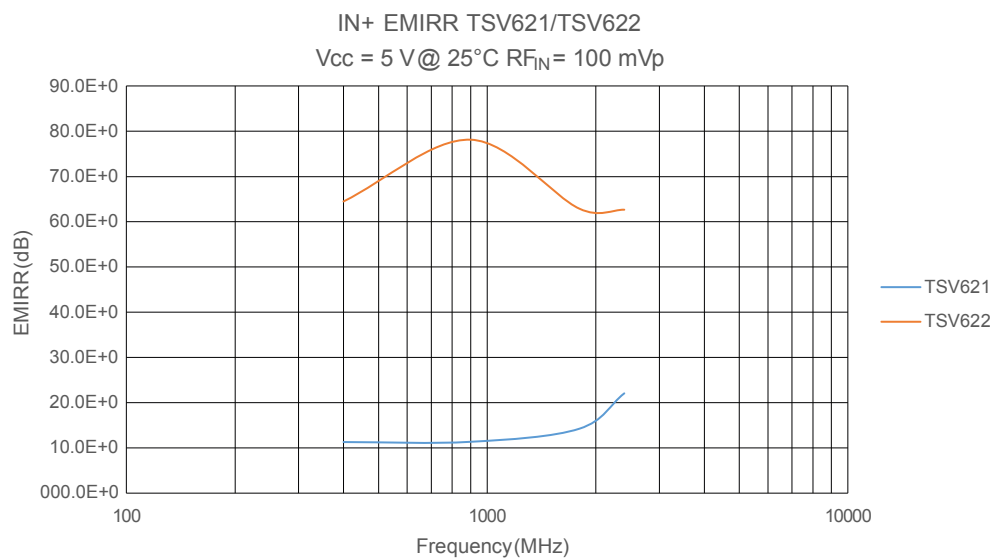
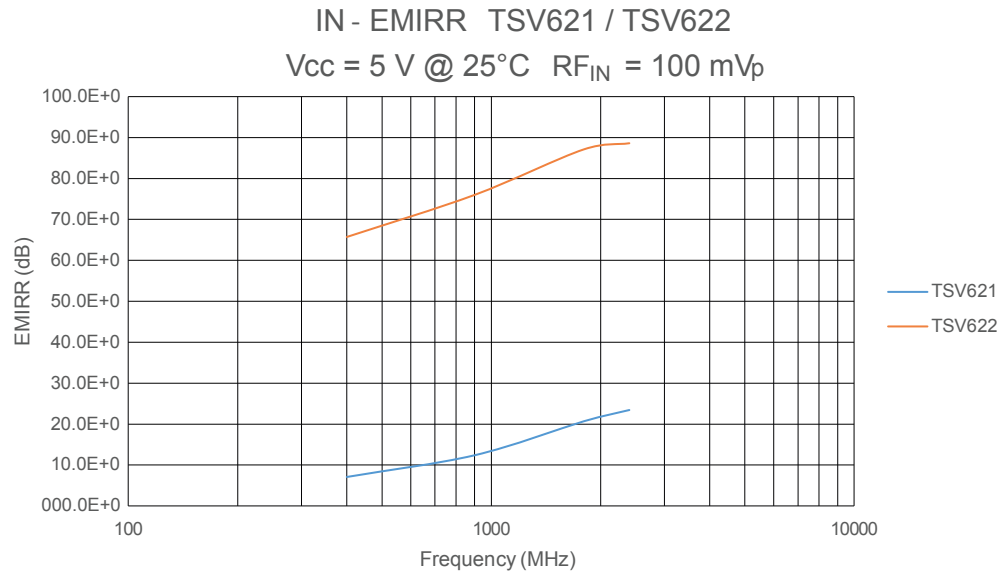
Figure 30. EMIRR result on PIN+


Figure 31. EMIRR result on PIN-



We can see that the **TSV622** (EMI-hardened op amp) is roughly 55 dB better than the **TSV621**, which is not EMI proof. It simply means that for the same EMI stress, the error signal is around 560 times higher on **TSV621** than with **TSV622** when the op amps are used in the same condition.

5.1 Passive component: one of your best friends for EMI immunity

As seen in the previous section, the RC filter is a very simple and cost effective solution to immunize a system against EMI. But it may also add some drawbacks. For example, a resistance generates a white noise with a spectral density of:

$$e_n = \sqrt{4kTR} \quad V/\sqrt{Hz} \quad (10)$$

Where k is Boltzmann's constant $k = 1.38 \times 10^{-23} \times JK^{-1}$.

And T the temperature expressed in Kelvin.

We can see that the greater the resistance, the higher the noise.

For reference, a 1 kΩ resistor is a noise source of roughly 4 nV/√Hz.

A high-Z circuit is generally more sensitive to picking up noise. This is because a small current induced on a high-Z circuit results in a higher noise voltage, so it is generally recommended to use low resistance values (there is a tradeoff with power consumption).

Because of input bias current, having high value resistors on the inputs creates a voltage drift and can add a non-negligible DC error on the output. Especially if a bipolar op amp is used as they tend to exhibit input bias current of several hundred of nV.

In order to limit this drawback, a common choke can be used instead of the resistance. It creates an LC filter of second order. But inductors might be more cost effective than resistances and capacitances.

5.2 Capacitors

Choosing a capacitor may become difficult due to the wide variety of such components. Here is a small list of the most commonly used capacitors.

- Ceramic capacitor:** The ceramic capacitor is a type of capacitor that is used in many applications from audio to RF. Values range from a few pF to several μF . Ceramic capacitors have many advantages such as size, and price. They present a low inductance and are particularly suitable for higher frequency decoupling applications; they can be used up to 1 GHz. Nevertheless, the characteristics of ceramic capacitors vary a lot depending on their dielectric.
 Regarding NP0, also called C0G, their capacitance only varies slightly due to change of temperature. The value range can be [0.5 pF to 0.1 μF].
 X5R or X7R (for higher temperature range) has a capacitance variation $\pm 15\%$ over their temperature range.
- Aluminum electrolytic capacitor:** The main advantage of aluminum electrolytic capacitors is the huge capacitance storage that they can provide (up to several mF). This type of capacitor is polarized. The main drawback of aluminum electrolytic capacitors is that they have high leakage rates, which is not convenient in applications for high-frequency AC coupling. They also have a wide tolerance range, usually $\pm 20\%$, which is not suitable for applications where precise values are needed, such as filtering circuits. But they are widely used for decoupling on applications working with frequencies lower than 100 kHz.
- Tantalum capacitor:** Like electrolytic capacitors, tantalum capacitors are also polarized and offer a very high capacitance level for their volume. But their main advantage compared to aluminum electrolytic capacitors is that they are smaller and more stable. The main drawback for this type of capacitor is its tolerance to high current spike. It can generally be used up to 1 MHz.

Bypass capacitor

EMI can also find a path from the power supply of the op amp, and so it is essential to use a bypass capacitor in order to present a low impedance, helping to reduce noise.

It is also necessary to choose the right capacitance in order to ensure the best filtering. As seen previously, material is important depending on the range of frequency needed to filter but it is also important to keep in mind that a capacitance does not act only as a pure capacitance.

At first level, a capacitor can be represented by a capacitance in series with a resistance and an inductance as described by Figure 32. Model of capacitance.

Figure 32. Model of capacitance



Figure 33. Capacitor impedance vs. frequency depicts the impedance of different capacitances vs. frequency from Murata. Three capacitances impedance made with the same material but with three different values are reported.

Figure 33. Capacitor impedance vs. frequency


After the self-resonant frequency, the capacitance starts to act as an inductance.

So, for the upper frequencies the capacitors do not exhibit low impedance and no longer play their role.

It is generally advised to use some hundreds of nF as decoupling capacitor, but do not assume that only one value can act with all frequency. It can be interesting to add in parallel a smaller capacitance value to attenuate higher frequency noise. But pay attention to the anti-resonance peak resulting from a self-behavior in parallel with capacitive behavior. A magic combination could be the association of 22 nF and 22 pF!

The higher the noise frequency, the lower the bypass capacitor should be (to exhibit the lowest impedance at the noise frequency).

These capacitors must be placed as close as to the op amp for a better efficiency as depicted in [Section 4](#).

6 Conclusion

When an op amp is placed in a high-frequency noisy environment, the first thing to understand is the EMI source and the frequency domain involved. Any kind of signal with a very sharp edge is susceptible to generating an EMC issue, as the edge can be defined as a large frequency spectrum.

It is extremely important to think of the PCB as a component itself of the schematic and the combination of a good PCB layout with added filtering, thanks to passive components, is a very efficient way to fight against EMI perturbation.

Capacitor selection must certainly be done carefully depending on its value and material in order to ensure the best efficiency against EMI.

It is also important to consider every node and trace as a potential antenna, in order to minimize them as much as possible.

In some cases, shielding can also be used to protect a sensitive device.

Unfortunately, there is no single EMI fix for all problems, so do not be afraid to experiment!

Revision history

Table 1. Document revision history

Date	Version	Changes
22-Jun-2022	1	Initial release.
17-Oct-2022	2	Minor text changes.

Contents

1	EMI origin	2
2	Differential and common mode interference	3
3	What is the impact of EMI on an op amp?	4
3.1	Common mode perturbation for a non-inverter schematic	4
3.2	Common mode perturbation for an inverter circuit	7
3.3	Common mode and differential mode perturbation for a differential schematic	8
3.4	Application example	11
3.5	Special care taken at PCB level	17
4	Printed circuit board layout	18
5	EMI-hardened op amp	20
5.1	Passive component: one of your best friends for EMI immunity	22
5.2	Capacitors	23
6	Conclusion	25
	Revision history	26

List of tables

Table 1.	Document revision history	26
----------	-------------------------------------	----

List of figures

Figure 1.	Differential mode.	3
Figure 2.	Common mode.	3
Figure 3.	EMI test with a bipolar op amp	4
Figure 4.	EMI effect on bipolar op amp without any protection	5
Figure 5.	EMI test with a bipolar op amp and RC filter	5
Figure 6.	EMI effect on bipolar op amp with RC filter	6
Figure 7.	EMI effect with the TSV632 EMI-hardened op amp and without RC filter	6
Figure 8.	Filtering of an inverter schematic.	7
Figure 9.	Bode diagram of the open loop transfer function	8
Figure 10.	Common mode EMI test with a bipolar op amp configured in differential mode	9
Figure 11.	Common mode EMI effect on bipolar op amp in differential mode without any protection	9
Figure 12.	Common mode capacitance	10
Figure 13.	Common mode and differential capacitance	11
Figure 14.	EMI effect on bipolar op amp in differential mode with RC filter	11
Figure 15.	Op amp used as current source	12
Figure 16.	System without any source of EMI.	12
Figure 17.	Output voltage of current source victim of EMI	13
Figure 18.	Input filtering	13
Figure 19.	Probe scope result of input filtering	14
Figure 20.	Output filtering	14
Figure 21.	Probe scope result of output filtering	15
Figure 22.	EMI disturbance with long tracks	15
Figure 23.	Vout with a filter on the op amp output	16
Figure 24.	Result on Vout of RC filter	16
Figure 25.	Output voltage of current source victim of EMI with a good PCB layout	17
Figure 26.	Dual schematic example	18
Figure 27.	Dual layout example	18
Figure 28.	Configuration for EMIRR test non-inverting input.	20
Figure 29.	Configuration for EMIRR test on inverting input.	21
Figure 30.	EMIRR result on PIN+	21
Figure 31.	EMIRR result on PIN-	22
Figure 32.	Model of capacitance	23
Figure 33.	Capacitor impedance vs. frequency.	24

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved