

## EFFICIENCY AND FET SELECTION

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Revised: March 19, 1999

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### Overview

The Tripath Class-T amplifier provides a number of advantages over a linear design of comparable output power. The overall efficiency of Class-T is a major plus. Another of the advantages of a Class-T design is in output device selection. Most linear designs require the use of comparatively expensive, complimentary matched pairs of N- and P-channel bipolar devices. A 200 Watt per channel linear design typically requires two of these devices per rail per channel (for a total of eight devices in a two channel amplifier). Class-T designs, on the other hand, utilize standard switch-mode N-channel FETs in the output stage, and a 300 Watt per channel stereo design is easily implemented with only four of these very cost-effective devices. This article will provide additional information about the output stage of the Class-T amplifier so that the designer can estimate final efficiency, calculate heatsink requirements, and select the appropriate FET for the application.

### FET Selection Criteria

The primary selection criteria for the output device in a Class-T design are:

- Drain-Source Voltage ( $V_{DS}$ )
- Maximum Power Dissipation ( $P_D$ )
- Drain-Source Resistance ( $R_{DS(on)}$ )
- Total Gate Charge ( $Q_g$ )

Once the target power output and operating voltages are known, the designer can use the above four parameters to select the output device independent of any other criteria. In practice, the designer should first choose a group of devices that meet the  $V_{ds}$  and  $P_D$  requirements, and then choose a device from that group that best meets the design goals. If low-power efficiency is a priority, then select a device with minimum  $Q_g$ . If peak load efficiency is more important, then the designer should select for lowest  $R_{DS(on)}$ .

## Drain Source Voltage

The choice of  $V_{DS}$  is driven entirely by the chosen operating voltages of the amplifier design. The device must be able to operate at the rail voltage, plus margin for ringing, thermal conditions, and bridged operation. Tripath recommends that  $V_{DS}$  be 50% greater than the combined rail voltage swing. Thus for a design using +/- 33.75 Volt rails (a typical 50W design), the minimum value for  $V_{DS}$  should be 100 Volts. If the layout is sufficient to minimize ringing under all conditions, then there is no need to choose a device of higher rating. Arbitrarily choosing a device of higher rating will lead to a less than ideal value for  $R_{DS(on)}$ . (Making a device with a high voltage capability requires that the epi layers be thicker, which means that they will be more resistive.)

## Drain Source On Resistance

The efficiency of a Tripath amplifier at full load is determined largely by the resistive losses in the output device(s). For this reason, if highest possible efficiency is the goal, the designer should select from among appropriate devices the one with the lowest value of  $R_{DS(on)}$ .

- Efficiency is inversely proportional to  $R_{DS(on)}$ .

This relationship is most important in higher-power designs, as small differences in  $R_{DS(on)}$  will lead to large differences in heat loss.

The value of  $R_{DS(on)}$  increases with die temperature. If the die temperature rises from 25° C (the commonly quoted value) to 125° C,  $R_{DS(on)}$  will typically double.

## Total Gate Charge

The gate of a MOSFET is electrically isolated from the body of the device. As voltage is applied to the gate (and the rest of the device), capacitance is created and charge accumulates under the gate. As this charge accumulates, material under the gate (which is normally p-channel in an n-channel device) is converted to n-channel material and current then flows through the device. This charge must be removed as the device transitions from an “on” to an “off” state, and must be restored as the device transitions from “off” to “on”. The energy lost in turning the device on and off is called the gate-charge switching loss and is proportional to the switching frequency, transition time, gate voltage and current. This lost energy translates directly to reduced efficiency. Gate charge is essentially

independent of temperature and, at idle, nearly all of the power losses in the Tripath amplifier are these switching losses.

- Gate charge losses are proportional to gate charge, frequency, and voltage.

## Diode Losses

The body diode of a MOSFET and the external Schottky diodes in the Tripath design are also sources of stored charge. Diode losses occur during switching when this charge dissipates through the  $R_{DS(on)}$  of that channel's active FET (on the opposite rail). Diode losses increase with frequency and output current. Also, since the charge dissipates through  $R_{DS(on)}$ , losses increase with temperature (though the amount of charge does not).

- Diode losses are a proportional to heat, frequency, and load current.

## Maximum Power Dissipation

The maximum power dissipation rating of a device ( $P_d$ ) is simply a measure of the ability of the device to withstand the heat generated by it's own internal losses. These internal losses are dominated by two components:  $I^2R$  losses due to  $R_{DS(on)}$ , and a group of switching losses, dominated by gate charge and diode losses. Total internal power losses must be kept below  $P_d$  and adequate heatsinking provisions must be made to keep the die temperature below the manufacturer's recommended maximum value.

- Maximum power dissipation in a Tripath design occurs at full load, and is the sum of switching losses and  $I^2R$  losses.

## Efficiency and Loss Equations and Calculations

In the Tripath amplifier, 95% of the losses at full load are resistive and switching losses. The proportion of the losses changes over the output range, but their sum (plus 5%) will define the total heat load of the output stage, and thus the heatsink requirements. Note that the peak heat load for a Tripath amplifier is reached at the maximum output level, unlike Class-AB and other linear designs. The equations for calculating the resistive and switching losses are:

- Resistive losses =  $I^2 R_{DS(on)}$
- Switching losses (including diode loss) =  $f \times .5T_f \times V \times I$

For an IRF640 FET in a typical Tripath application (200W/channel) with  $T_j=140^{\circ}\text{C}$ :

$$R_{DS(on)} = .28 \text{ Ohms}$$

$$T_f = 35\text{ns} \text{ (typical, with } R_g=9.1\Omega)$$

$$V = 40\text{V}$$

$$I = 6\text{A (RMS)}$$

$$f = 200 \text{ kHz (represents full load operation)}$$

$$\text{Resistive Losses} = I^2 R_{DS(on)} = 36 \times .28 = 10.08\text{W}$$

$$\text{Switching Losses} = f \times .5T_f \times V \times I = 200\text{K} \times .5 \times 35\text{ns} \times 40 \times 5 = 1.18\text{W}$$

$$\text{Total Losses} = 11.26 \text{ W per device, or } 45.1 \text{ W total in a } 400\text{W amplifier}$$

$$\text{Efficiency} = 400 / (400 + 45.1) = 89.9\%$$

## Paralleling MOSFETS for High Power (>1KW) Designs

Many designers of higher-power amplifiers have, at one time or another, had to resort to paralleling output devices in order to guarantee safe and reliable operation. This is a common requirement in linear designs due to the fact that, in these designs, the output devices must dissipate as much as 50% of the peak load. In a Tripath amplifier, however, the output devices are only required to dissipate 10-15% of the peak load. This means that the use of paralleled output devices is rarely necessary. Therefore, a pair of standard 125W devices (per channel) in TO-220 (or similar) packages with proper heatsinking can safely be used in a 300W/channel amplifier design. Using available standard n-channel devices, it is only when the power requirements get up above 1kW that paralleled devices become necessary. For efficiency calculations, paralleling identical devices has the effect of halving  $R_{DS(on)}$ , but doubling the switching losses. As a consequence, idling efficiency is greatly reduced, but full power efficiency is improved. For example, using the above values:

$$\text{Resistive Losses} = I^2 R_{DS(on)} = 36 \times .14 = 5.04\text{W}$$

$$\text{Switching Losses} = f \times .5T_f \times V \times I = 200\text{K} \times .5 \times 70\text{ns} \times 40 \times 5 = 2.36\text{W}$$

$$\text{Total Losses} = 7.4 \text{ W per device, or } 29.6 \text{ W total in a } 400\text{W amplifier}$$

$$\text{Efficiency} = 400 / (400 + 29.6) = 93.1\%$$

Should paralleled devices be needed to meet the design goals, the designer should be aware that the Tripath TA0102A/TA0103A products are rated to drive a total gate charge of 100nC per rail per channel. If large high-power devices are paralleled, this specification can be exceeded, leading to unstable operation of the amplifier. Should gate charge be a limiting factor in the design, the designer may wish to investigate the “NB” series of power MOSFETs from ST Microelectronics. These parts have low gate charge as a function of  $P_D$ .