1
GENERAL DESCRIPTION

The 4400 Audio Test Set consists of basically three sections: A generator or a transmitter developing a source signal, a meter or measuring facility and a receiver or analyser to evaluate the returned signal. In addition to the basic facilities of a conventional test set the instrument incorporates several additional features to provide a more complete and rapid performance evaluation of the device or medium under test.

Efficient integration of facilities, sophisticated control circuits and good human engineering enhance the use of the 4400 and reduce the chances of measurement error.

The instrument uses inovative circuits, state of the art semiconductors such as CMOS logic and Bi-fet linear devices and high quality components throughout. It requires a minimum of calibration and provides easy access to all circuitry. All integrated circuits are on plug in sockets and most parts are standard "off the shelf" types to facilitate service.

In addition to front panel controls two multicontact connectors are provided on the rear panel for external equipment, remote programming and connection of accessory products to expand the basic facilities of the instrument.

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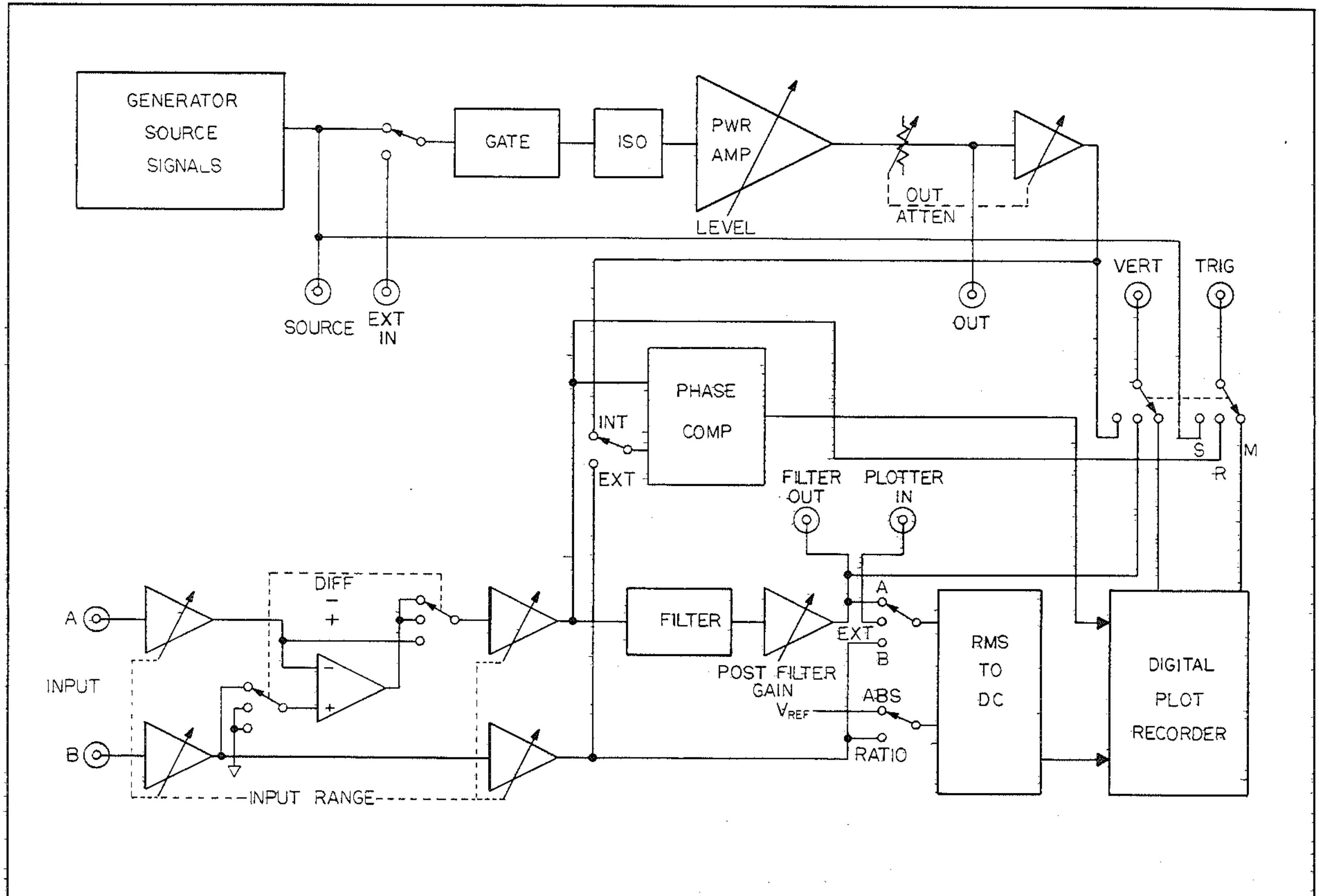


4400A BLOCK DIAGRAM

CAUTION

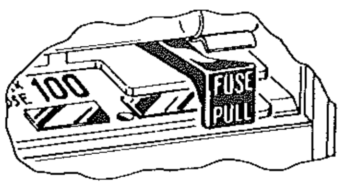
This instrument can be set to operate from one of four nominal power line voltages. Unless otherwise specified, instruments shipped to North America destinations are set to operate from 120V AC, those to other destinations are set for 240V AC. Before connecting this instrument to a source of AC power ensure that both the voltage selection card and the fuse are correct.

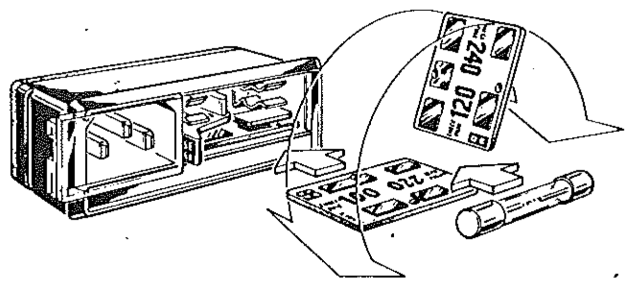
VOLTAGE AND FUSE SELECTION					
Input Voltage (48 to 440 Hz)	Max	105	126	231	252
	Min	90	108	198	216
Voltage Selection		100	120	220	240
Fuse Selection		500 mA		250 mA	

HOW TO SELECT OPERATING VOLTAGE

1. Open cover door and rotate fuse-pull to left.
2. Select operating voltage by orienting PC Board to position desired voltage on top left side. Push board firmly into module slot.
3. Rotate fuse-pull back into normal position and re-insert fuse into holders, using caution to select correct fuse value.

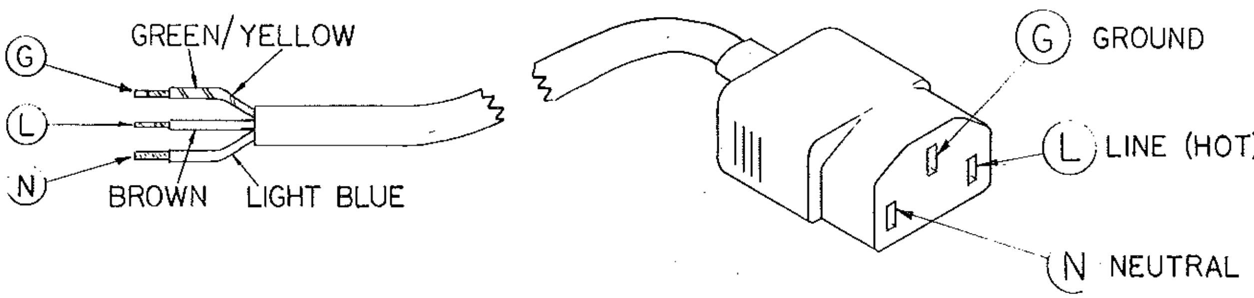
Operating voltage is shown in VS&F Connector window.



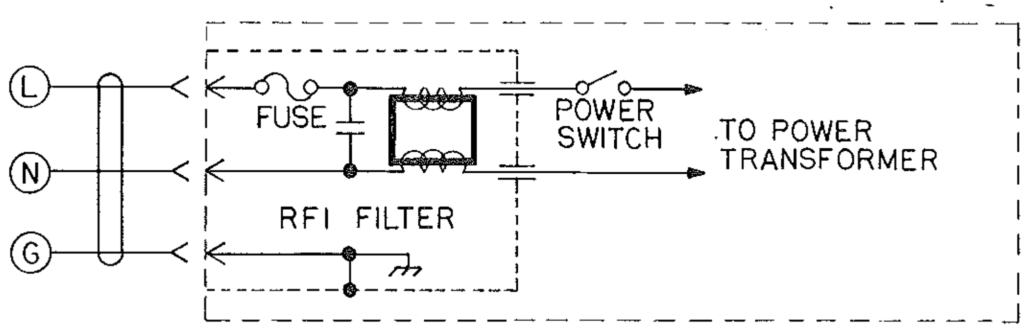


POWER CORD PREPARATION

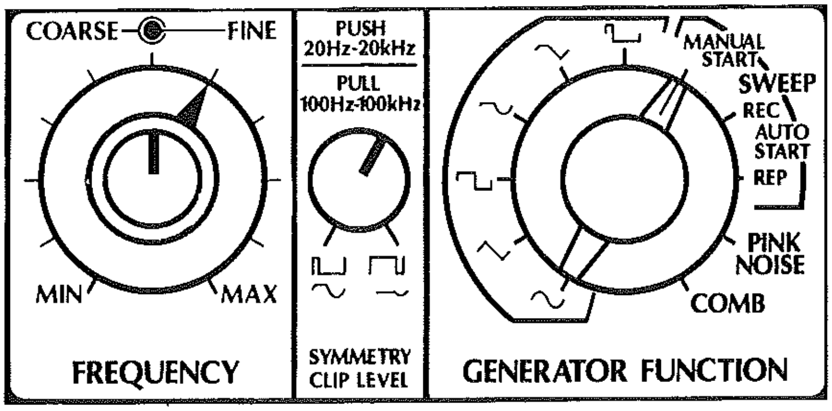
Instruments shipped to destinations outside North America are supplied with a power cord with conductors employing I.E.C. color code and ready to accept a male plug (not supplied) to mate with the customers receptacle. Refer to the accompanying sketch to determine connection procedure. (Instruments shipped to North American destinations are supplied with a power cord terminating in a molded female receptacle at one end and a molded standard twin blade plus ground male plug at the other end. These cords, of course, require no preparation.)

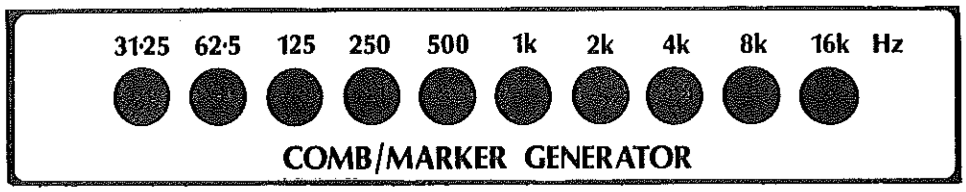


IEC POWER CORD



INSTRUMENT





2.1 GENERATOR SECTION

The generator or transmitter section provides the basic source signals for all measurements. It consists of several source signals, a gating circuit and an output power amplifier.

2.1.1 GENERATOR FUNCTION CONTROL

The GENERATOR FUNCTION Control chooses the signal to be generated. The first six positions of this control choose the function generator and set one of 6 possible wave forms: sine, triangle, square, asymmetrically clipped sine, asymmetrically clipped triangle and pulse. The frequency of these waveforms is set by the concentric FREQUENCY controls over a range of approximately 1000 to 1. The push/pull control in the center selects the broad range: In: 20 Hz to 20kHz or Out: 100 Hz to 100kHz. Within this range the COARSE and FINE FREQUENCY controls set a specific frequency. The FINE control varies the frequency set by the COARSE control by approximately ±12%. (It should be noted that the FINE control continues to operate in the SWEEP mode although the COARSE control operates only in the first 6 positions of the GENERATOR FUNCTION control).

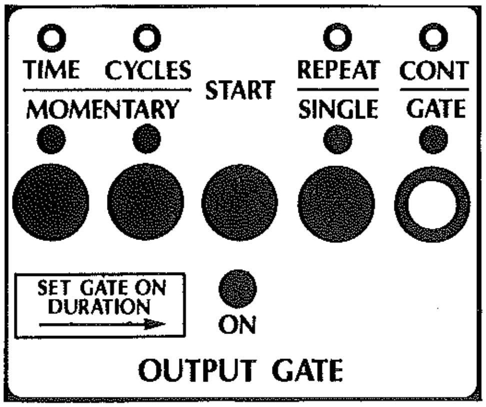
The CLIP LEVEL control sets the clipping point of the asymmetrical wave forms. It is generally set to approximately 75%. A mid frequency asymmetrical clipped triangle is particularly useful as a "quick check" signal. This wave form will provide an immediate indication of polarity or 180° phase reversal, low frequency roll off by the tilt of the clip line, high frequency roll off by the shape of the triangle, crossover distortion and several other gross malfunctions.

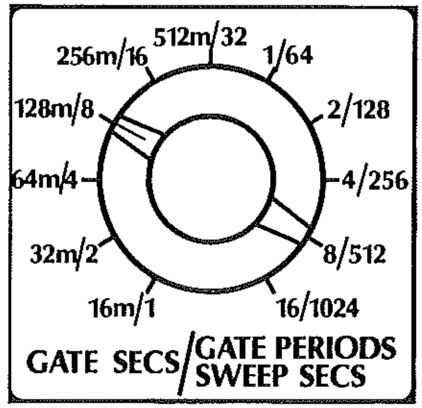
Positions 7,8 and 9 of the GENERATOR FUNCTION control choose a sweep mode. In this mode the sine wave is swept up or down logarithmically over the selected range (20 Hz to 20kHz or 100 Hz to 100kHz). Speed of sweep and other parameters are set by the SWEEP section. As this mode closely relates to the receiver section it will be described in a separate section of this manual.

Position 10 is PINK NOISE. This is a psuedo random pink noise signal of particular value in acoustic testing. It is derived from white noise which is digitally generated and passed through a seven section 3 dB per octave low pass filter. The white noise generator uses a 26 stage shift register and 128kHz clock which provides a 524 second sequence length and spectral lines separated by 0.002 Hz.

Position 11 is a unique signal. It consists of any combination of ten fixed frequency sine waves at the ANSI octave frequencies. The sine waves are selected by the 10 COMB/ MARKER GENERATOR pushbuttons. Selected one at a time they form accurate and stable reference signals. Selected in combination they become a comb signal useful for spectrum analysis markers and other applications.

The signals are digitally generated by counting down the master crystal clock. The 10 resulting square waves have 3rd-harmonic components eliminated by digital cancellation and the results are filtered by 10 5-pole Butterworth low pass filters to produce 10 sine waves. They can then be selected in combination and summed. As the original reference is a crystal clock the signals are accurate and stable in both frequency and amplitude. The 5-pole low pass filters and 3rd harmonic cancellation yield a distortion in the order of 1% T.H.D. or better.





2.1.2 OUTPUT GATE

This section provides a means of turning on the selected source signal for a predetermined time with either a SINGLE or REPETITIVE burst. The predetermined time may be keyed to either a length of time, a number of cycles of the waveform or a manually determined time.

The pushbutton on the right marked CONT/ GATE (continuous/gate) bypasses the gate control and selects continuous operation. With this pushbutton OUT, the gate logic controls the output signal. The START pushbutton initiates the gate period and the ON led shows when the signal is ON in any mode.

With the SINGLE mode selected three triggers are possible: TIME, CYCLES or MOMENTARY.

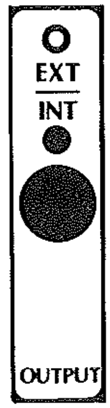
In the TIME mode the signal is on for a specific time from 16 milliseconds to 16 seconds as selected by the 11 position rotary switch. The ON period starts on the next positive going zero crossing transition of the signal, continues for the selected time and switches off at the next positive going zero crossing transition. Thus an integral quantity of cycles is generated and the actual time is the time selected, plus up to one cycle period. The ON period continues for the selected interval regardless how long the START button is activated.

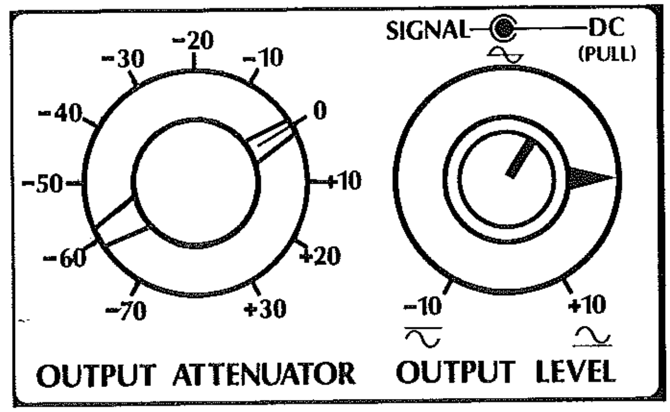
In the CYCLE mode the gate is on for a selected quantity of cycles of the source signal. The quantity of cycles is selected by the 11 position rotary switch from 1 to 1024 cycles in a binary sequence.

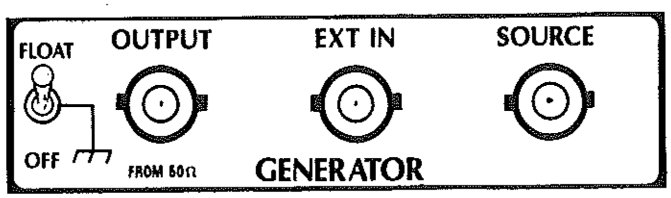
If both the TIME and CYCLES buttons are out the gate in is the momentary mode. In this mode the gate is ON when the START button is pushed and OFF when the button is released. The ZERO CROSS feature is functional in this mode as well.

In the REPEAT (repetitive) mode, two triggers are possible: TIME or CYCLES. Operation is essentially the same as the SINGLE mode described above but is a continuous stream of on and off tone bursts. The ON and OFF times are always identical and are the same as would be if the SINGLE mode had been selected. For example if CYCLES and 4 is selected the output will be 4 cycles on followed by an equivalent period of silence followed by 4 cycles on and so on.

The gate operation may be remoted by grounding terminal 8 of J1 on the rear panel (the connector farthest from the AC power connector.) This action is equivalent to pushing the START push button.





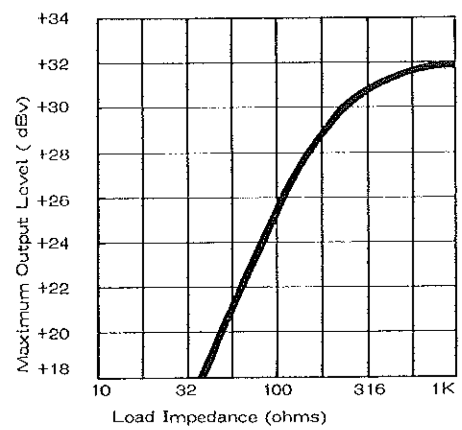


2.1.3 OUTPUT AMPLIFIER

The output power amplifier provides a low impedance, high-power drive to a load. It may be set to provide either a floating output or ground referenced output. The floating output may be efficiently used to reduce the problems caused by ground loops in measurement set ups. The output float is achieved without the use of a transformer to preserve the quality of output waveform generated by the generator section. Although actively achieved,it exhibits the floating characteristics of a true transformer output. That is,either side may be connected to instrument ground with no change in output.

The output amplifier is capable of producing in excess of 8 watts into a load. The voltage output swing is ±50V peak while the current is limited to approximately ±200ma peak. This represents an output level of over +33dBm. The output impedance (that is the source impedance of the amplifier) is 50Ω. This value remains constant in the floating or grounded mode and at any attenuator setting. The output load impedance will normally be 600Ω but may be anywhere from ∞ to 50Ω. With a 50Ω load the maximum output capability is reduced to approximately +20dBv. It will however drive load impedances as low as 300Ω to full output before current limiting. The output is short circuit protected by virtue of the output current limiting. The amplifier is not thermally protected, however, and certain forms of abuse could damage it. Adequate ventilation must be provided and extended short circuits or high level drives to low load impedances should be avoided.

The output level is variable over a range in excess of 100 dB using the OUTPUT ATTENUATOR and OUTPUT LEVEL controls. The attenuator varies the output level in 10dB steps while the variable level control provides a nominal 14dB range to provide a total output range of approximately +33dBm to -80dBm. A concentric knob within the LEVEL control may insert a DC offset in the output. This is activated



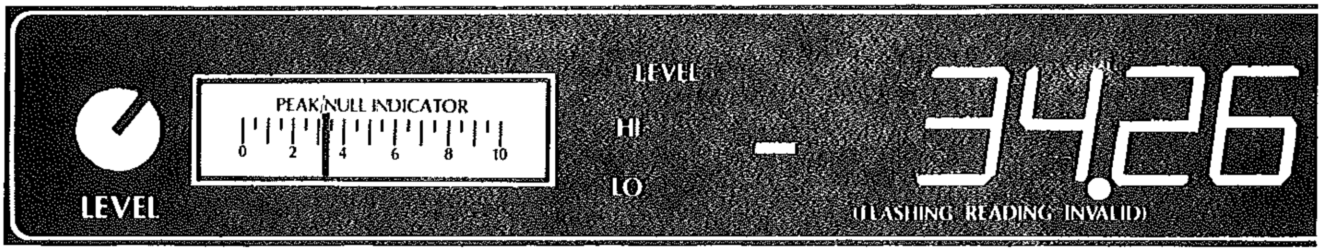
Maximum Power Amplifier output level in dBv for various load impedances. (0 dBv = 0.775 VAC rms)

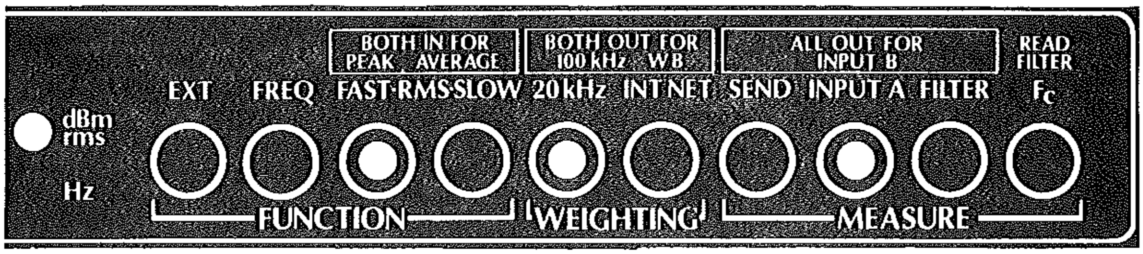
by pulling the knob and turning clockwise for positive offset and counter-clockwise for negative offset.

The miniature toggle switch adjacent to the OUTPUT connector selects FLOATING, GROUNDED or OFF modes. In the OFF mode the connector is grounded and connected to a 50Ω source resistor.

SOURCE OUT AND EXT IN

The SOURCE OUT connector is the direct output of the selected source signal prior to gating and the output amplifier. It may be used as a generator sync out signal or as the output for further processing. The EXT IN connector is the input to the gating circuits and the power amplifier (and its associated attenuator). It is activated by pushing EXT. Signals connected to this input can benefit from the gate function and the drive capability of the power amplifier. The nominal maximum input level is approximately +12 dBv (3v rms). External processing may be inserted between SOURCE OUT and EXT IN. For example a filter will produce band limited pink noise if this source is selected.





2.2 MEASUREMENT SECTION

The measurement or meter section provides a digital readout of amplitude and frequency of either the send (generator) signal or the receive signal. The frequency readout is in Hertz from 10Hz to over 100kHz while the amplitude readout is in dBm from over +30.00dBm to lower than -90.00dBm.

The amplitude measurements are in dBm and either true rms, average or peak. The measurement bandwidth may be chosen by front panel pushbuttons.

An auto range level setting circuit permits automatic amplitude measurements over a wide range and facilitates frequency measurements of low level signals.

2.2.1 INPUT SELECTION

The readout may measure two parameters: frequency and amplitude, of four circuits: the output or what the generator is sending, the input or what the receiver is receiving, the output of the filter or wave analyser or the center frequency of the filter itself.

When measuring SEND amplitude it is measuring the absolute level in dBm delivered to the output connector. To prevent disturbing the output floating configuration the meter measures using an isolated preamp whose gain is the inverse of the output attenuation. Thus it will be sensitive to output load variations and indicate the true signal delivered to the load.

2.2.2 FUNCTION SELECTION

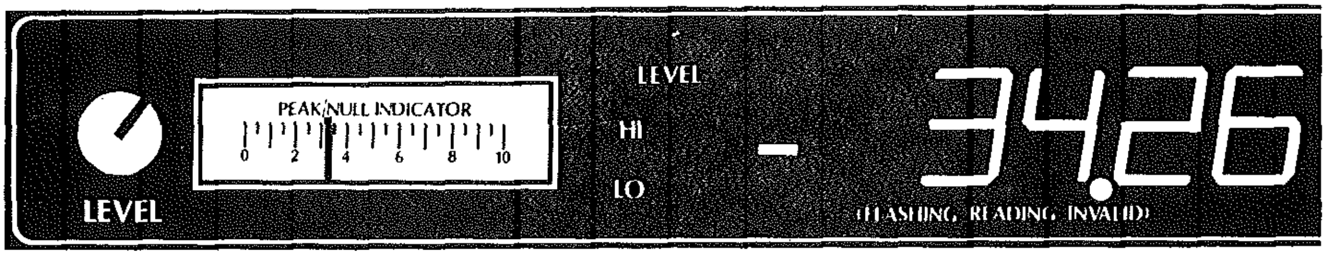
Four pushbuttons set the function of the measurement section. The first button EXT, selects an external accessory connected to J3 on the rear panel. In this mode the digital readout is completely connected to the external device.

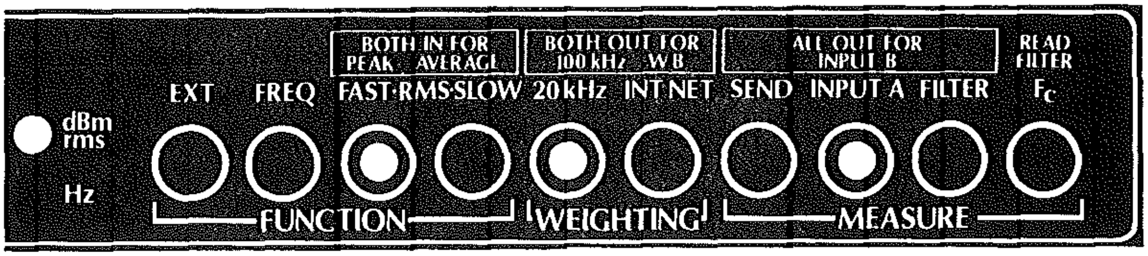
The second button FREQ causes the readout to display the frequency of the selected signal in Hz. The measurement time is one second and the display is updated at the completion of each measurement. Auto ranging level circuits allow a measurement over a 60dB range. Beyond this range the HI or LO leds will light and the display will flash indicating an invalid reading.

The next two pushbuttons select the amplitude measuring mode. The third button selects FAST RMS, the fourth button SLOW RMS and if both buttons are pushed the detector is PEAK or AVERAGE as determined by an internal connection. (see section 4 for details on how to make this connection.) The instrument is normally calibrated so each of the three detectors will show the RMS value of a sine wave. With other wave forms the three readings will obviously be different.

The unweighted bandwidth of the measuring instrument is 20Hz to 100kHz. Certain measurements require readings to be made in a more restricted bandwidth. With both weighting buttons OUT the full 100kHz bandwidth is selected. Pushing 20kHz inserts a 3 pole 20kHz Butterworth low pass filter in the measuring path. This provides measurements in the audio band. If INT NET (internal weighting network) is pushed a user option weighting network is selected. An internal accessory socket accepts plug-in weighting networks. Details are provided in section four for construction of 1,2, or 3 high pass or low pass filters, band pass and band rejects filters, band pass and band reject filters and A,B and C weighting networks. A high performance operational amplifier is dedicated to this function and most filters may be constructed using only resistors and capacitors.

If both weighting buttons are pushed the resultant curve will be a composite of the two. As buffers are used no interaction will be caused by using both filters simultaneously.





The weighting networks are normally used to make particular amplitude measurements. However, they may also be used when making frequency measurements to reduce the errors caused by trying to measure the frequency of noisy signals.

The readout is a 5-1/2 digit (5 full digits and ±1 digit) LED display. The large 0.6 inch filter enhanced display facilitates viewing even at great distances. LED's on the right of the display show the measurement units and LED's on the left show high or low levels. When these are lit the signal level presented to the measurement section is outside the amplitude capabilities of the circuit. At the same time the readout will flash to show an invalid reading. The over and under trip points are approximately 3dB away from the actual limits as an added protection. For example when reading 0dBm to -60dBm the display will flash above -3dBm and below -57dBm. Readings will, in fact, be valid over the full 0 to -60 range however.

Note that the resolution of the dBm measurement is much above the stated absolute accuracy. This is common in digitally measuring instruments. While the meter will not measure over its entire range to 0.01 dB absolute accuracy, over a small range say, 10dB, will maintain an accurate 0.01 dB relative accuracy. Thus it is possible to compare two signals of approximately the same amplitude and determine their dB difference to 0.01 dB accuracy.

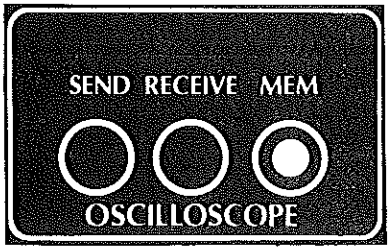
The meter has a measurement range of over 150dB. This enormous range is handled by breaking it up into several 30dB ranges and either autoranging or manual ranging to place the input signal within a particular 30dB window. The range switching is at approximately -3, -33, -63 and -93dBm. Internal trim adjustments permit the ranges to be adjusted for maximum absolute accuracy, however, this accuracy is not claimed to be 0.01dB. Thus the above statement regarding 0.01dB relative accuracy is true within a particular range, for example -10dB to -15dB. But from say -30 to -35dB a range change will take place and the 0.01dB relative accuracy will not be maintained.

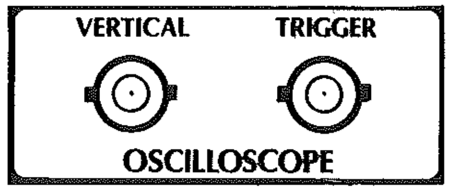
The nominal amplitude range of the instrument is +30dBm to -90dBm. However the output amplifier will actually provide up to +33dBm. To accommodate this level the meter has an over-range circuit at the high end to extend the measurement capability above +30dBm. Thus it will measure the full output level of the generator.

Similarily at the low end the inclusion of the band pass filter in the receive section permits measurements below -90dBm. An additional 30dB range at the low end extends the capability of the instrument well below -100 dBm

To the left of the digital readout is a small analog meter and sensitivity control. This meter may be used to see trend indications or find peaks and nulls; it is useful any time relative level change is more important than absolute level. The scale is arbitrary and the variable control permits setting the meter to a mid-scale reading. The meter is measuring a DC voltage representative of the true RMS amplitude of the signal and is located after the autoranging circuitry. Thus as the input signal is increased the meter will read higher and higher until it falls to a low level and begins climbing again.

The meter may measure at several selected points in the instrument. SEND measures the actual signal delivered to the load at the OUTPUT connector. INPUT A measures the signal connected to INPUT A in the DUAL CHANNEL mode and the signals at both INPUT A and INPUT B in the DIFFERENTIAL MODE. FILTER measures the signal at the output of the receiver filter and with all three buttons OUT the signal at INPUT B (in either the DUAL CHANNEL or DIFFERENTIAL mode) is measured. Finally if FILTER and FREQ are both selected and READ FILTER F_c is pushed the receiver filter will be put into oscillation at its natural (center) frequency and that frequency will be displayed.





2.2.3 OSCILLOSCOPE

Three pushbuttons are provided as a convenience to select the signal viewed on an external oscilloscope. Two connectors are provided for vertical or Y signal deflection and trigger.

The three pushbuttons each route a particular set of signals to the two connectors to establish oscilloscope sync and viewing of the selected signal.

If SEND is pushed the vertical connector contains an amplified version of the actual signal presented to the load while the TRIGGER connector contains the SOURCE output. In this manner the oscilloscope will remain syncronized regardless of what happens to the output. For example, if the OUTPUT is a gated tone burst the SOURCE is a steady version on the same signal. The oscilloscope will trigger on the continuous waveform and not be falsely triggered by the gating action.

As stated the VERTICAL output is an amplified version of the actual OUTPUT. In this way it will show the true OUTPUT signal as presented to the external load. The amplification presents a good oscilloscope drive signal even with very low outputs. Also the constant level TRIGGER signal will prevent the oscilloscope from loosing sync as the signal is lowered. Finally, the isolation amplifier presents an instrument ground referenced oscilloscope signal without disturbing the OUTPUT floating characteristics.

If RECEIVE is pushed the VERTICAL output contains the FILTER OUT signal while the TRIGGER contains the INPUT A signal. The FILTER OUT signal is, of course, a wide band signal similar to INPUT A in receiver functions which do not include the filter (positions 6 through 11). Also INPUT A is only the signal connected to INPUT A in the DUAL CHANNEL mode. In the DIFFERENTIAL mode this signal is the differential input provided by both INPUT A and INPUT B.

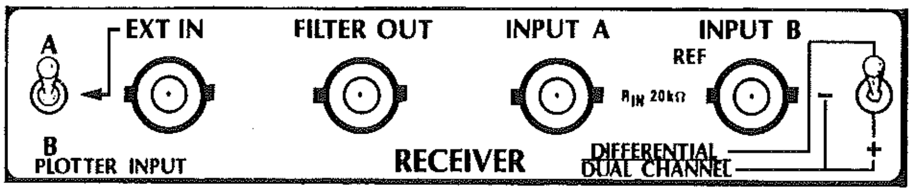
As in the SEND mode the choice of different pick off points for VERTICAL and TRIGGER signals prevents the oscilloscope from loosing sync, for example, as the filter is passed through a null in the reject mode.

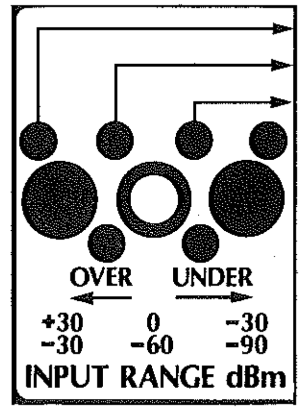
If both the SEND and RECEIVE buttons are pushed the VERTICAL output will be FILTER OUT while the TRIGGER will be generator SOURCE out.

Finally the MEM mode selects the outputs of the digital memory or plot recorder as selected by the DISPLAY control group. In this mode the oscilloscope should be set to a 200 μs per division sweep. The vertical deflection should be set to place the approximate 5 volt pattern over 6 or 8 divisions of the screen.

Memory data is read out as a series of eight sub frames to form a single frame. The eight sub frames are each plot with its associated reference lines repeated twice. The trigger pulse is arranged so that four of the these sub frames overlay to form the composite frame. If the oscilloscope used is dual trace it should be switched to single trace. If left in the dual trace mode it will probably only display two of the required four sub frames. Thus depending on which trigger pulse it uses, it will display A only or B only but not both.

If all three buttons are out,the VERTICAL and TRIGGER connectors will contain signals determined by user selected conditional strapping on an internal 14-pin header. This header contains additional signals such as memory clock signals, SWEEP commands and INPUT B signals. See section 4 for variations.





2.3 RECEIVER SECTION

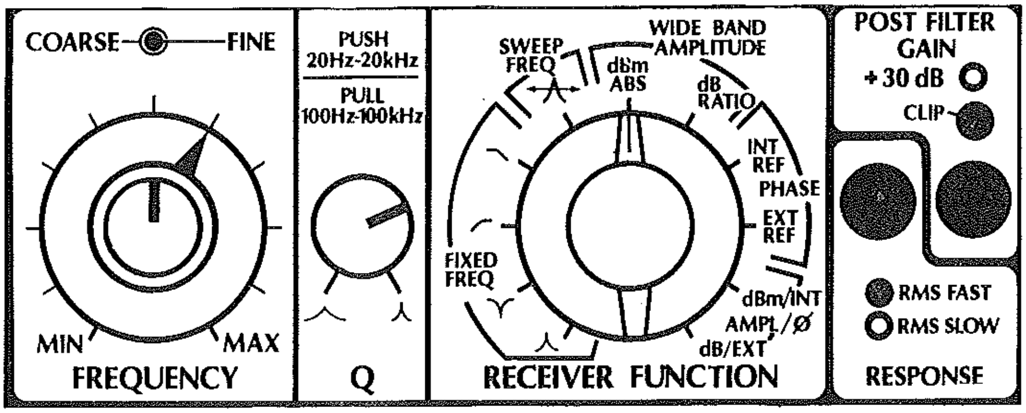
This section is perhaps the most unique in the instrument and contains some of the most powerful features. It begins with a wide band instrumentation type front end or preamp followed by a choice of filter, wide band processor or phase comparator and finally terminating in the digital plot recorder. It permits a detailed analysis of the generator signal as returned by the device or medium under test. Amplitude measurements in restricted bandwidths (wave analysis) may be made and XY plots in the form of amplitude or phase versus time or frequency can be generated.

A word about a basic philosophy carried throughout the instrument is in order. The audio industry is basically a logarithmic world. Intensity or amplitude is measured in dB or dBm, a log based unit, as opposed to volts, a linear based unit. That is, each time a signal level is doubled it is increased by a fixed amount (6 in the case of dB). Similarily in the frequency domain a log frequency scale or linear octave scale is used. This format is derived from our subjective perception of sound. We consider a sliding tone going from say 100Hz to 200Ha to change by the same amount as from 10000Hz to 20000Hz. In both cases the signal increases by one octave yet at the higher frequency the change is 100 times the number of cycles as the lower frequency. Because of this subjective perception most audio measurements are made with log units. Amplitudes are measured in dB or dBm and frequency scales are log with linear octave spacing. This also means that noise must be pink noise and not white and filters must be constant percentage bandwidth as opposed to constant bandwidth. All functions of this test set are based on these facts in order that information be presented in the most meaningful format.

2.3.1 FRONT END

Two inputs are provided: INPUT A and INPUT B. (these designations are purely for reference and in no way are they related to MEMORY A or MEMORY B.) The two inputs may be configured as independent input channels i.e. a DUAL CHANNEL preamp or as a DIFFERENTIAL (single channel) preamp. The miniature toggle switch selects the configuration. In the upper position the inputs form the differential inputs of an instrumentation type preamplifier. INPUT A is the non inverting (positive) input while INPUT B is the inverting (negative) input. The output of the differential preamplifier feeds the filter input. In the lower position the two inputs are separate and independent, although with the same gain. They separately feed the two inputs of the phase comparator and the inputs of the two RMS converters in the dB ratio circuit. In the mid position an inversion stage is inserted into the A input. Otherwise the configuration is the same as the lower position. i.e. DUAL CHANNEL. The +/- option provided by the mid and lower toggle positions facilitates phase measurements as it can correct an external phase inversion between two input signals.

Three pushbuttons determine the gain of the front end section. They are set according to the signal level to be processed. High level signals will fall in the +30dBm to -30dBm range, medium level signals from 0 to -60dBm and low level signals (microphones, tranducers etc.) in the -30dBm to -90dBm range. If an incorrect choice is made the OVER or UNDER led will light and an arrow will point to a lower or higher button. A different selection should be made. The OVER led indicates the front end is clipping or near clipping (the led comes on 3dB below clipping). The UNDER led show the signal is too close to the noise floor of the preamp.



When the input range is selected one of four led's above the pushbutton group will light to show which of four display ranges has been selected. There are three preamp gains and two gains after the filter, the combination of which can select one of four possible measurement ranges.

Measurements made in the measurement section by selecting INPUT A or INPUT B are made after the input preamp and prior to any further processing. The digital display in the measurement section is absolute and takes into consideration the gain of the front end.

2.3.2 RECEIVER FUNCTION

The receiver function switch sets the basic operational mode of the receiver. The first mode is used for wave analysis or plots in a restricted bandwidth. The filter may be switched to a band pass, band reject, high pass or low pass mode. The center frequency of the filter is set by the concentric FREQUENCY controls and the filter Q or percentage band width is set by the Q control. The frequency range is similar to that of the generator with two nominal ranges of 20Hz to 20kHz and 100Hz to 100kHz. The Q range is approximately 70% to 2%.

To read the amplitude of the signal at the output of the filter the FILTER button is pushed in the measurement section. With this button pushed and the FREQ button selected the frequency of the signal present at the output of the filter is measured. Finally with these same two buttons pushed and the READ FILTER F_C button held, the center frequency of the filter is displayed. This frequency is found by putting the filter into oscillation with amplitude stabilization and disconnecting the input signal. The AGC circuit ensures that the filter will oscillate at its center frequency. This frequency is, of course, not necessarily the same frequency as the input signal.

The "center" frequency of the high pass and low pass filter is the -3dB point in low Q settings or the peaking frequency in high Q settings. The filter shapes for various configurations and Q settings are shown in the illustrations.

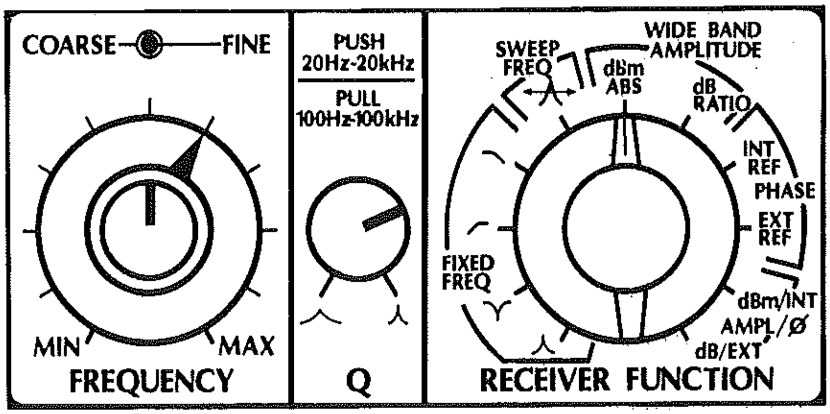
The output of the filter is available at FILTER OUT for further processing or external measurements.

Position 5 is a log sweep of the band pass or band reject filter over the range 20Hz to 20kHz or 100Hz to 100kHz. This is the spectrum analysis mode and is used with the digital plot recorder. The Q control has the same effect as in the manual mode.

A 30dB gain stage may be switched into the output of the filter to measure low level signals in the presence of high level signals. For example, say an input signal contained both 1kHz and 10kHz and the 10kHz was 60dB below the 1kHz. The INPUT RANGE (front end) would be set so the higher level signal, 1kHz, would not overload the preamp. If the band pass filter were set to 10kHz the 1kHz would be virtually non existant but the 10kHz signal would be a low level. Pushing the +30dB POST FILTER GAIN button would permit measurement of this low level signal.

The addition of this gain after the filter permits very low level measurements to be made. In a narrow bandwidth levels considerably below -100dBm may be made. The measurement section takes into account the additional 30dB of gain switched in.

The 30dB gain stage may be used in the spectrum analysis mode (position 5). However very slow sweeps must be made to permit the filter to settle after switching to a new value. Speeds of 2 minutes or longer are necessary.



In the sweep mode the filter is actually incremented through 256 logarithmic steps by switching precision resistors in the frequency determining section. This provides a significant advantage over, for example a voltage controlled filter. The frequency determination is very accurate, better than 2% at any step. The range can be 3 decades (10 octaves) without the limitations that would be present at one end or the other in an analog technique. Finally the frequency determination is extremely stable with time and temperature. There are no trim adjustments and drift is virtually nil.

The penalty for all these advantages is switching transients. The filter is frequency programmed by an 8 bit digital code for its 256 values. Each time a new value is entered a switching transient will be generated.These are greatest at the MSB (most significant bit) transitions, i.e. at one quarter, one half and three quarters of the sweep. No visible switching transients would imply they be over 90dB below clipping or about ten parts per million. With the very high Q x Frequency products of the filter (over one million) this is virtually impossible.

The proper technique is simply to wait for the transient to die down before taking the measurement and storing the value in the digital plot recorder. A slow sweep speed will accomplish this. With very slow speeds (4,8 or 16 minutes) it is possible to plot down to -120dBm.

RECEIVER FUNCTION SWITCH POSITIONS
6 through 11

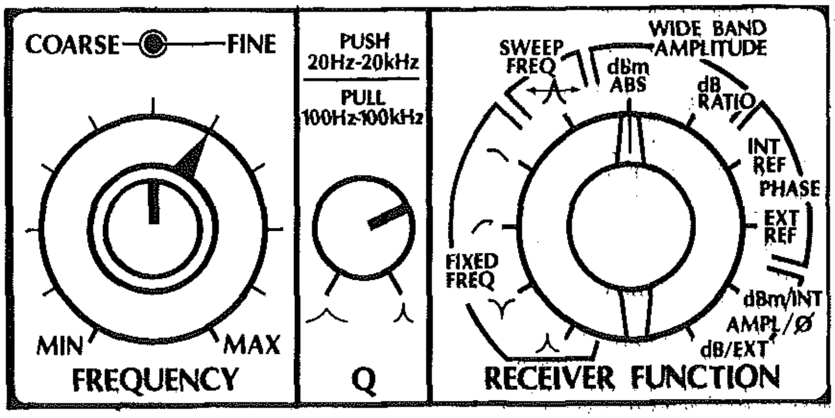
These positions remove the filter from the input and provide WIDE BAND or PHASE plotting capability. Positions 6 and 7 plot wide band amplitude vs time. If the generator is switched to SWEEP the time axis becomes frequency so the resulting plot is amplitude vs frequency (assuming the device under test does not change during the sweep time).

Position 6 is the ABSOLUTE dBm mode. That is the plots will be the absolute amplitude using an internal precision reference. Position 7 is dB ratio and is the amplitude difference between two inputs. In this mode the input preamp must be set to the DUAL CHANNEL mode. The plot will be the amplitude of INPUT A as referenced to INPUT B. The range is ±30dB. (see window selection). The two signals must be both within the input range selected and differ by no more than 30dB.

Positions 8 and 9 are phase vs time (or vs frequency if a sweep signal is selected in the generator). Position 8 plots the phase difference between signal at INPUT A or INPUT B and the generator OUTPUT. That is the reference is the SEND signal. Position 9 is the phase difference between two signals at INPUT A and INPUT B respectively. INPUT B is the reference input. Again the DUAL CHANNEL mode must be selected.

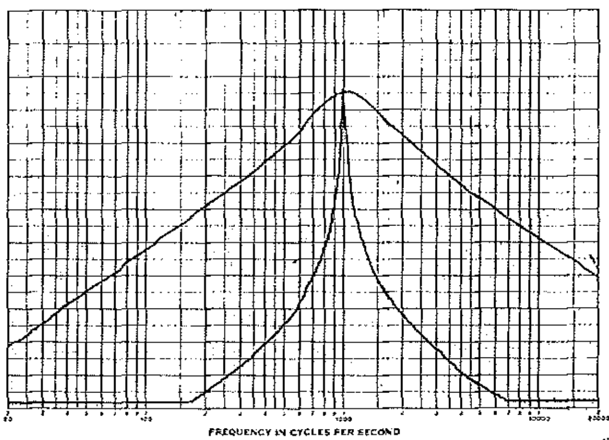
If the two signals are in phase or almost in phase select - DUAL CHANNEL. If they differ by close to 180° use + DUAL CHANNEL. This selection will put the plot near the center of the window. In DUAL CHANNEL the total window is ±180° while in +DUAL CHANNEL the total window is 0 to +360°. As the plot nears the upper or lower limits of the window its phase difference becomes ambiguous and the plot will show this ambiguity as chatter. Selecting a different configuration with the toggle switch will place a 180° offset in the plot to shift it to the center of the window.

Positions 10 and 11 are dual plotting modes, Position 10 is Positions 6 and 8 combined while POSITION 11 is POSITIONS 7 and 9 combined. They are exactly equivalent to doing two separate plots into two memory positions at two different times but combine both plots in a single sweep. These positions override the MEM ENTER selection and place the two plots in A and B or C and D.

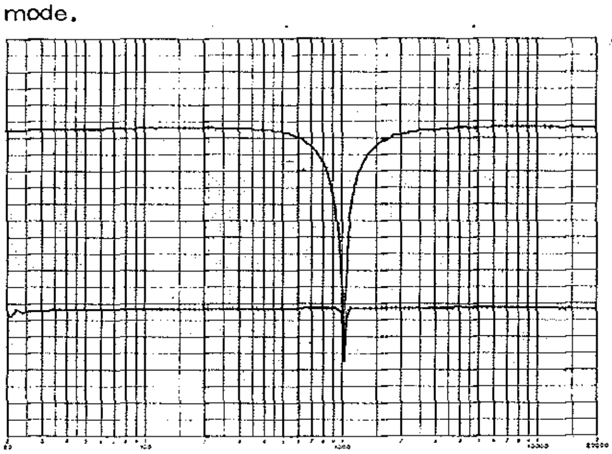


2.3.3 FILTER SHAPES

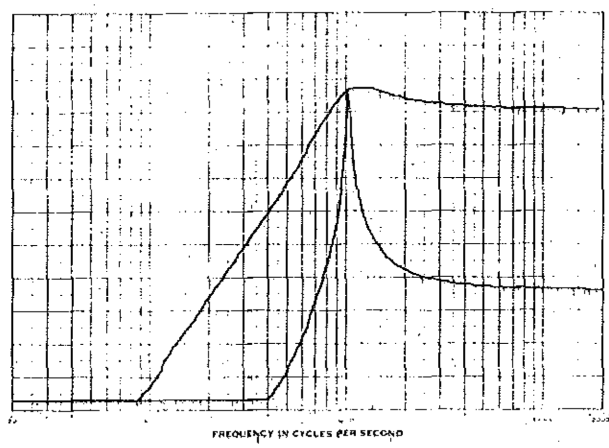
The 4400A receiver section includes a state variable filter with provision for either manual tuning or sweep tuning. The filter may be configured as either a BAND PASS, BAND REJECT, HIGH PASS or LOW PASS format. In addition the Q or percentage bandwidth may be adjusted over a wide range. Each of these parameters is mutually independent.



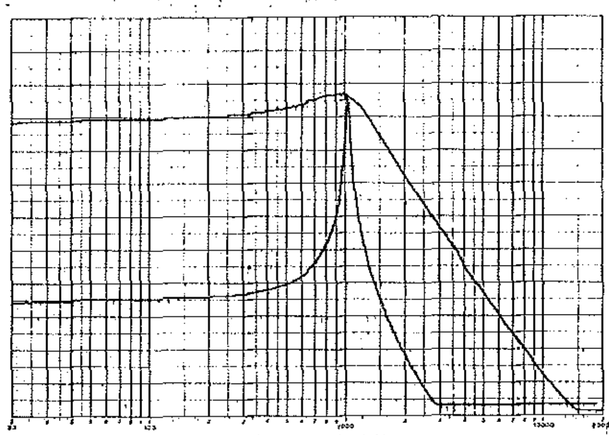
BAND PASS configuration. The asymptote of the filter skirts is 6dB per octave. At maximum Q (approx. 3%) the skirt is approximately 35dB down at 2F and 1/2F. The filter parameters are identical in either the MANUAL TUNE mode or the SWEPT TUNE (digitally programmed mode.



BAND REJECT configuration. Maximum notch depth is with the Q control at minimum (fully CCW). The depth at center frequency is approximately 55 dB max. while the attenuation at 2F and 1/2F is less than 2dB.

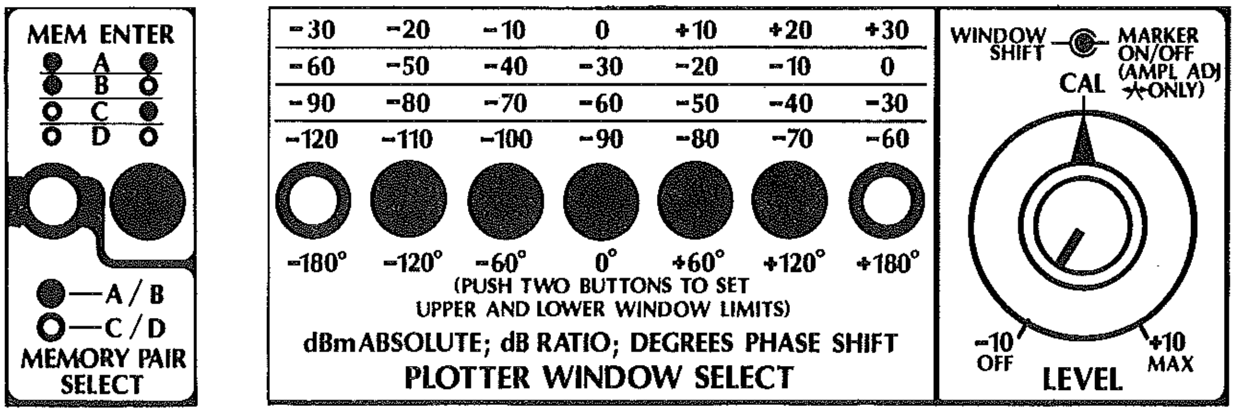


HIGH PASS configuration. Increasing Q produces a "corner peaking" effect. The asymptote of the roll off is 12 dB per octave.



LOW PASS configuration. Similar to HIGH PASS again with 12dB per octave roll off.

The filter is configured so any Q setting gives a constant center frequency gain. This avoids clipping problems as the bandwidth is reduced. With the BAND PASS filter centered on a steady sine wave the amplitude at the output of the filter should remain within 2dB as the Q control is varied over its range. However if the sine wave is replaced with PINK NOISE the filter output will decrease as the bandwidth is reduced (or Q increased) as a lower bandwidth passes less energy.



2.3.4 DIGITAL PLOT RECORDER

MEMORY SELECT, WINDOW SELECT and LEVEL

This control grouping establishes the mode of operation of the write or enter portion of the digital plot recorder. The recorder contains four digital memories divided into two pairs. The memories are designated A and B for the first pair and C and D for the second. One pair may be selected at a time and either position of that pair addressed. The MEMORY PAIR SELECT pushbutton selects the pair. Out, it selects pair A and B; in, it selects pair C and D. The MEM ENTER button selects which position of the selected pair will be addressed. Thus if both buttons are out the plot will be "written" into memory position A. With both buttons in position D would be selected and so on.

Writing a plot into a memory position automatically erases the previous plot.

In absolute amplitude response plots the vertical range is determined by the seven PLOTTER WINDOW SELECT pushbuttons and the WINDOW SHIFT LEVEL control. The total vertical range may be any 10,20,30,40, 50 or 60dB window within the INPUT RANGE chosen in the front end. This window is selected by pushing any two of the seven pushbuttons in the group. For example if the 0dBm to -60dBm range had been chosen on the INPUT RANGE group the second led would light pointing to the 0 to -60 scale. Then by pushing the 0 and -50 buttons for example a 50dB window would be chosen. If the -20 and -30 buttons were pushed a 10dB window would be selected. The seven buttons permit a permutation of 21 possibilities of windows within the 60dB scale selected.

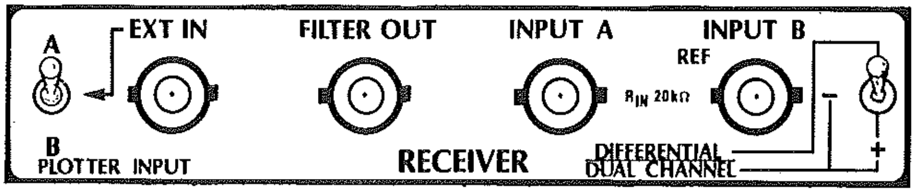
When the WINDOW SHIFT LEVEL control is in the CAL center detent position the plot is as selected above. By moving this control clockwise or counterclockwise this scale may be shifted up or down approximately 10dB. This is useful where it is desired to lay a trace on a particular reference line or oscilloscope graticule.

Bear in mind that all of these controls affect the trace write mode. That is they must be set before the plot is made.

In ratio amplitude response plots the vertical range is as defined by the top scale: -30 to +30 The total window is ±30dB and 21 possibilities from 10 to 60 dB total range may be selected. Remember the scale is dB ratio. The two signals may, for example, be -52dBm and -43dBm absolute but their difference (or ratio) is 9 dB. The two signals must be within the input range selected and differ by no more than 30dB. For example if 0 to -60 is selected on the INPUT RANGE switch and one signal is -20dBm the other signal can be between 0 and -50dBm.

In phase response plots the vertical range is ±180° (or 0, +360° as described earlier). Again 21 possibilities between 60° and 360° total window may be selected. The amplitude of the two input signals must be within the INPUT RANGE selected and a suitable phase difference window may be selected.

Before continuing a word about frequency response plots. There are basically two methods to generate an XY plot of amplitude vs frequency of a device or medium. You may use a swept sine wave and a wide band receive or a wide band source, such as pink noise, and sweep tune the receive. The swept sine wave gives, by far, the fastest results, the most accurate and the cleanest display. It can be used to analyse an amplifier, a filter, an equalizer, a tape recorder or any electronic medium.



However, normally it cannot be used with acoustic mediums or tranducers due to room reflections, standing waves and other disturbances which would cause large errors in the results. In this case the pink noise/tuned receive method must be used.

The swept wave method is selected by setting the GENERATOR FUNCTION switch to SWEEP and the RECEIVER FUNCTION switch to WIDE BAND. The swept filter method is selected by setting the GENERATOR FUNCTION switch to PINK NOISE and the RECEIVER FUNCTION switch to SWEEP FREQ and the band pass mode. The digital plot recorder controls operate in an identical way for either method.

A further mode is possible by using a swept sine wave and swept tuned receive. The filter has not specifically been optimised to track the generator as this would involve a completely different approach to the sacrifice of some of the parameters that have been optimised. However, at low Q settings it will track with reasonable accuracy. The plotted results will be the same as swept sine wave/wide band receive except they can be made in the presence of noise in the device under test. The wide band receive cannot differentiate between the swept sine wave and the noise floor of the test medium. Using the filter with minimum Q an additional 10 or more dB margin may be gained with less than 2dB error due to mistracking of the filter and generator.

DIGITAL PLOT RECORDER INPUT

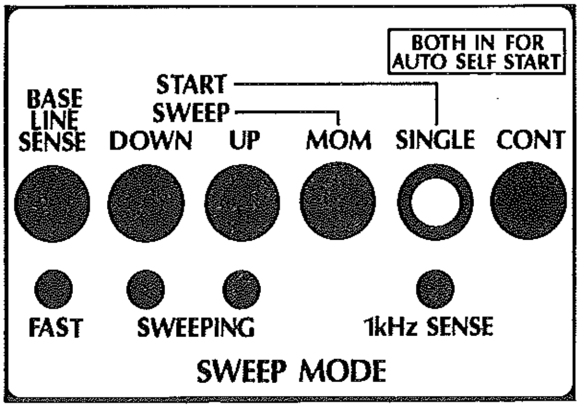
The miniature toggle switch designated PLOTTER INPUT selects the input to the amplitude plotting section. With the switch up it selects FILTER OUT. The filter, in turn, is fed from INPUT A in the DUAL CHANNEL mode or INPUT A and INPUT B in the DIFFERENTIAL mode. When the filter is not selected by the RECEIVER FUNCTION SWITCH (Positions 6 through 11) the FILTER OUT connector (and thus PLOTTER input when A is selected) is the output of the INPUT A preamp. That is, the filter acts as a unity gain, wide band buffer.

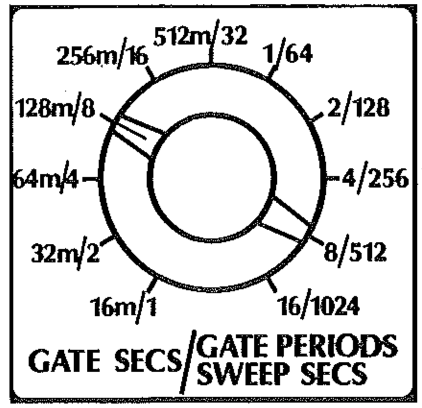
With the switch in the mid position the plotter is fed by the signal connected to EXT IN. The nominal input level at this point is +13dBm to -47dBm corresponding to the 60dB plotting window.

Finally, with the switch in the lower position the plotter is connected to the INPUT B preamp.

This facility permits the front end of the receiver, and specifically the filter, to be used for other functions and still retain the plotting capability. For example, it may be desired to connect the filter between SOURCE and EXT IN in the GENERATOR using PINK NOISE in order to achieve swept, band limited PINK NOISE but use the WIDE BAND mode of the plotter by using INPUT B or EXT IN.

The detectors used to produce the single line amplitude plots are a true RMS to DC converters. They have selectable response times, RMS FAST or RMS SLOW, by pushing the RESPONSE button. The fast mode will more generally be used, while the slow mode is useful for pink noise analysis.





2.3.4.1 SWEEP CONTROLS

The sweep controls are common to the generator sine wave sweep, the receiver filter sweep and the digital plot recorder. They consist of a mode selection, sweep initiate control and sweep speed control.

There are three sweep modes: MOM or momentary, SINGLE and CONT or continuous. The SINGLE mode is a single up or down sweep after pushing the UP or DOWN button. CONT is a repetitive version of SINGLE with a short pause between sweeps. MOM is a manual sweep where the sweep is under direct control of the UP and DOWN buttons. Sweeping takes place only when the buttons are held and sweep direction may be reversed mid-sweep.

While the instrument is sweeping, a vertical line or cursor moves across the plot to show the memory enter position. Also, the led below the UP or DOWN button flashes at the sweep rate to show direction and speed. The cursor is particularly useful in the momentary mode for example to examine a filter response. The cursor can be "walked" to the peak of a filter, the frequency and amplitude read then "walked" to a new point and readings taken. The slope in dB per octave can be measured along with other parameters. Both UP and DOWN pushbuttons can be used to zero in on a particular spot.

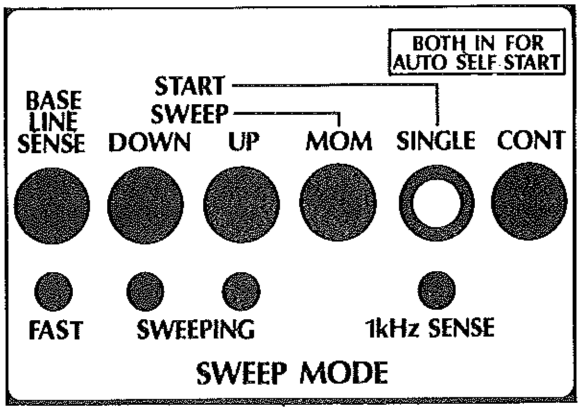
In the MOM mode when the sweep has reached an end point it stops. It can only be moved by sweeping in the opposite direction. In the SINGLE or CONT modes when the sweep reaches an end point it resets to the opposite end and may continue in the same direction.

The 11 position rotary switch selects the time for a complete sweep. It is variable from 1 to 1024 seconds in a binary sequence.

The sweep speed must be carefully chosen. It is desirable to use the maximum speed before the results are inaccurate. Several factors determine the maximum permissible sweep speed. They are basically the Q of the swept filter (if used) and the Q of the device being measured. The higher the Q, the steeper the slopes in the plot and the slower the sweep speed must be.

If too high a speed is used two things will happen. First, sharp peaks will be rounded. This will be particularly noticable on very sharp spikes of peak or notch filters. Second, an apparent frequency displacement or shift in the direction of sweep will be noticed. These errors obey a basic law of physics relating sweep speed to device Q and cannot be overcome in any other way except a slower speed. This speed can be determined very easily by doing a plot at a particular speed into one memory then doing the same plot in the opposite direction into the other memory. When the horizontal displacement is nil or very low the speed is acceptable. Another method is to examine the shape of sharp peaks. As the speed is reduced the peaks will sharpen. When no further sharpness is evident by switching to lower speeds, the correct speed has been chosen.

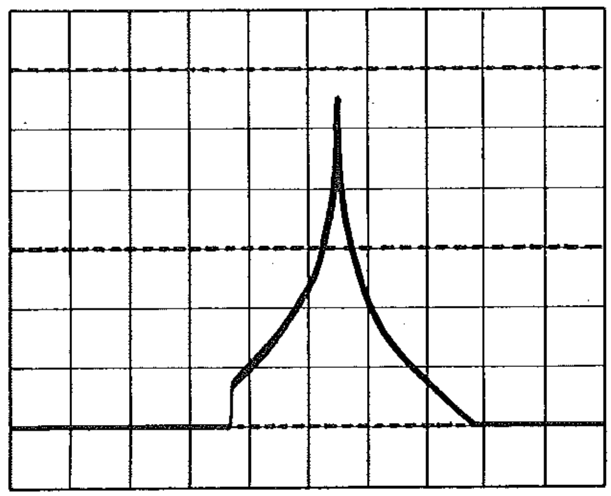
It will be found that devices with reasonable flat responses, such as amplifiers, tape recorders etc. can be swept from 20Hz to 20kHz in 1, 2, or 4 seconds with accurate results. Sharp filter and equalizers will require 8, 16 second or slower sweeps. Acoustic plots using pink noise and SLOW RMS detection will generally require a slow sweep.



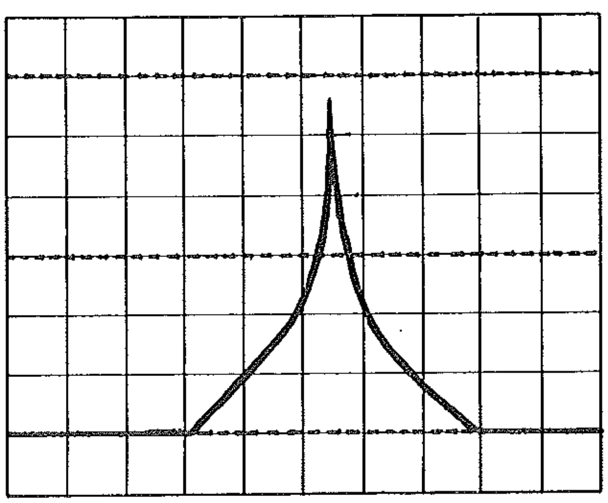
2.3.4.2 BASE LINE SENSE

Certain plots can be made in less time than normally required. In particular, plots of band pass filters. Such curves have a bell shaped response with a sharp peak at the center frequency and large attenuation a few octaves above and below the center frequency.

To achieve these plots rapidly, a feature called BASE LINE SENSE may be used. With this button in the sweep is speeded up whenever there is no information, that is when the cursor is on the base line of the plot. The "fast" sweep speed may be chosen internally to be 2,4 8,16 or 32 times the selected speed.

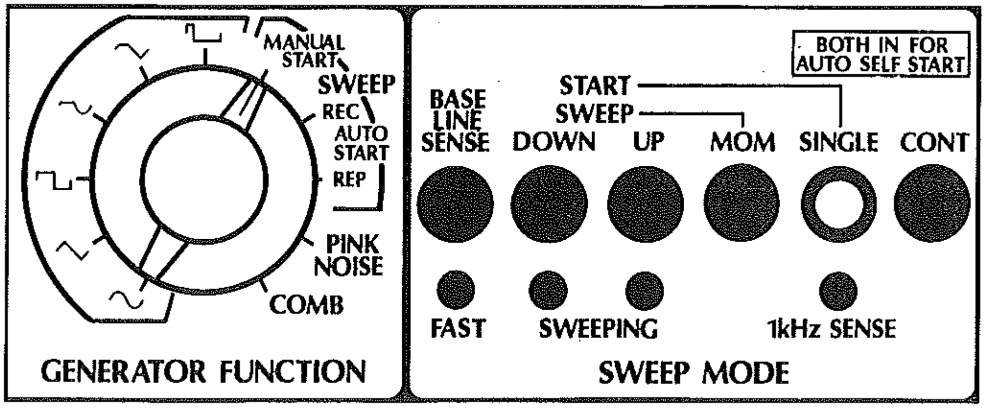


Sweep with BASE LINE SENSE. With SWEEP SPEED knob set to 16 secs, slow speed during data plot is at 16 seconds rate, fast speed during base line plotting is at 2 second rate. Total time to generate the plot would be approximately 9 to 10 seconds.



Normal Sweep. With SWEEP SPEED knob set to 16 secs total time to generate this band pass filter plot would be 16 seconds.

The instrument is normally shipped with the 8x speed selected. If, for example, a 32 second sweep is chosen to achieve a good sharp plot at the peaks, the speed will be at the 4 second sweep rate when on the base line and will immediately switch to a 32 second speed to plot the filter and then return to the rapid speed at the base line. Because of the fast approach speed the leading edge of the filter plot may show a small error in the form of an overshoot but the important peak and the trailing slope will be as accurate as a full 32 second plot although it will have taken far less time. When in the fast mode the FAST led below the BASE LINE SENSE button lights up.



2.2.4.3 AUTO START

Certain response plots must be made where the generator and receiver are separated in space or time. For example, response plots of a transmission line or a tape recorder. The instantaneous swept sine wave frequency must coincide with the digital plot recorder X axis address. This is automatic when both happen simultaneously but some means of synchronization must be used otherwise. The 4400 uses a 1kHz cue tone before a sweep to accomplish this.

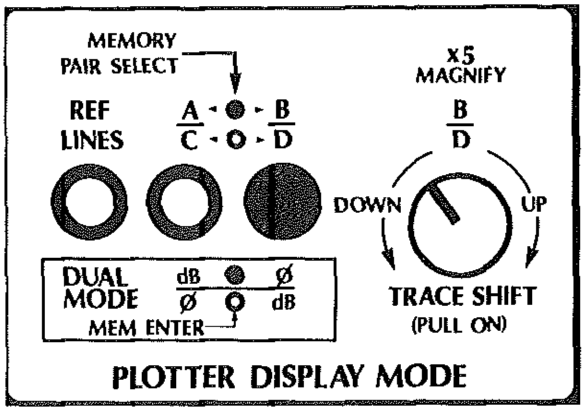
Two AUTO START modes are provided REC or record and REP or reproduce. REC is identical to the normal MANUAL START mode except at when the generator is not sweeping the output is 1kHz rather than the normal 20Hz (or 20kHz). This permits a 1kHz cue tone to be recorded between sweeps. As soon as the UP button (or DOWN button) is pushed the output falls to 20Hz and sweeps up to 20kHz (or the reverse for DOWN). At the conclusion of a sweep the output returns to 1kHz until the next sweep is initiated.

The REP mode is similar to the MANUAL SWEEP mode except sweep start is initiated by detecting the drop out of 1kHz. During tape playback and with a 1kHz signal on the INPUT connectors the 1kHz SENSE led will light. As soon as the sweep starts the signal changes to 20Hz or 20kHz and the 1kHz led goes out. If the UP or DOWN pushbutton is held in before the sweep starts, the digital plot recorder will start as soon as the 1kHz stops and thus load the memory in syncronism with the previously generated sweep. Obviously the SWEEP SECS (speed) must be in the same position for both send and receive and both must be either UP or DOWN.

If, for example, several response plots are required of a tape recorder while various bias settings are tried or some other parameter is varied, several sweeps will be recorded with a short pause between sweeps containing the 1kHz cue tone. Before each sweep the parameter is varied. On playback the UP button would be held in during the 1kHz portion and could be released as soon as the sweep starts. If the memory enter controls are changed before each sweep up to four separate plots could be made.

The sweep can be programmed to automatically start by pushing both the SINGLE and CONT buttons in. Doing this eliminates the requirement of holding the UP or DOWN button while the 1kHz disappears. This is useful, for example, during playback optimization of a tape recorder. If a tape has several sweeps recorded on it with short pauses between sweeps the plot will be updated each time a new sweep is played back. Adjustments can be made during the pause and the results will be displayed with a new sweep as an old one is erased. With the initial sweep on the second trace a direct comparison of the improvement can be made on a continuous basis.

The AUTO START mode operates in any receiver function, that is, both amplitude and phase plots.



2.3.4.4 DISPLAY CONTROLS

This control grouping determines the memory display format. They operate in conjunction with the MEMORY SELECT pushbutton (pair select).

REF LINES (reference lines) turns on 3 horizontal dotted lines at maximum, medium and minimum amplitude as set by the DISPLAY RANGE pushbuttons. If an amplitude window from, for example, -20dBm to -40dBm was chosen to make the plot the top line would indicate -20, the center -30 and the lower -40dBm.

The second two pushbuttons select either or both traces from the memory pair selected. Note that when the MEMORY SELECT pushbutton is out, the buttons select memory position A and/or B; in, they select C and/or D.

The TRACE SHIFT control can provide three separate functions. The choice of one of these is made by operating miniature rocker switches inside the instrument. Details of these setups are given in section 4.

The three functions are:

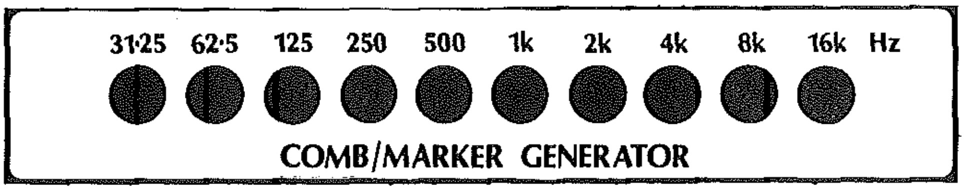
TRACE and REFERENCE LINES SHIFT
TRACE ONLY SHIFT
TRACE MAGNIFY AND SHIFT

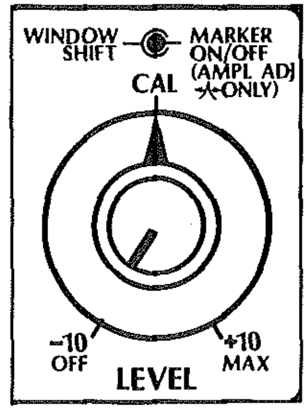
The first of the above allows plot B or D to be shifted vertically up or down with respect to A or C. This is useful where it is desired to view two plots of unrelated data where superimposition would cause confusion. In this mode the reference lines associated with the shifted trace move with the trace to retain an accurate vertical scale reference.

TRACE ONLY SHIFT is identical to above except the reference lines remain fixed. This is useful to reposition one trace over the other for direct comparison.

TRACE MAGNIFY AND SHIFT magnifies the vertical scale of the B or D trace by precisely 5. This is equivalent to dividing the previously selected window by 5. For example, if a 10dB window had been used for memory enter it would now be 2dB, a 60° phase window would be 12° and so on. Note that this function is only DISPLAY magnify and does not affect the selected WINDOW. The WINDOW selection is a memory enter function and affects the scale factor of data to be stored in the DIGITAL PLOT RECORDER. The X5 function temporarily changes the display of the memory output. The memory quantization will become more visible - what was displayed as 256 steps will now be 51 steps. Had a 10dB window been used to record the plot each step would be 10 divided by 256 or 0.04 dB.

The designations below the push buttons indicate which trace is amplitude and which is phase when a dual plot is generated. Remember that when in the dual mode the MEM ENTER push button (right button of the two) is controlled by internal logic. If this button were in during the plot (normally selecting B or D) PHASE will be recorded in A (or C) and amplitude in B (or D). If the button was out the reverse would be true. This flexibility permits the user to himself select the assignment of parameters between the traces. The graphics define the choice.



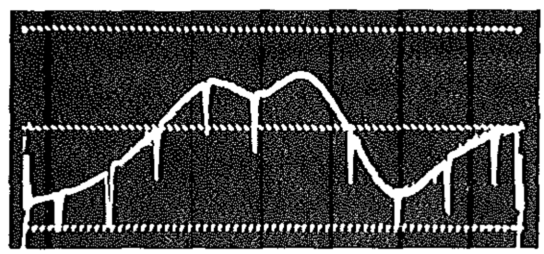


2.3.4.6 MARKERS

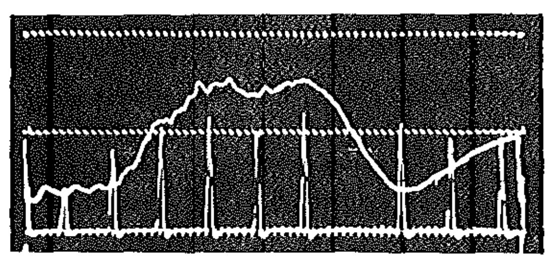
Two types of frequency markers may be added to response plots to obtain accurate frequency references. The markers are added during a sweep and are entered into the memory. Markers are turned on by rotating the small MARKER knob past the click stop off position. Up to ten markers may be added to a plot as selected by the COMB/MARKER GENERATOR pushbutton bank. Any combination from one to ten markers at octave intervals from 31.25 Hz to 16kHz may be selected.

In the SWEPT SINE WAVE/WIDE BAND RECEIVE mode the marker generator is a digital circuit which compares the signal on the INPUT connector (a sine wave sweep) with a set of accurate, crystal controlled reference signals. When the swept input signal frequency is the same as a reference signal a marker in the form of a negative going spike is added to this trace. If, for example, the 1K, 2K and 8K buttons were pushed in, three spikes would mark these frequencies on the plot. By interpolation and extrapolation other frequencies could be determined. These marker spikes in combination with the reference lines facilitate accurately reading information about a response directly from the trace. (An up sweep must be used).

In the swept filter mode the markers are actually a comb signal mixed with the input. The digital principle cannot be used, of course, since the input is not sweeping. The MARKER knob adjusts the amplitude of the comb signal and the COMB/MARKER GENERATOR push-buttons select the frequencies to be displayed. In some cases it may be desirable to put markers only, with no signal, on one trace and signal, with no markers, on the other trace. In this way the filter Q and display window can be optimized for best display. The markers will show as positive going spikes if a 10dB window and high Q setting is used. By using the trace shift control the marker peaks can be positioned over the signal plot on the other trace.



Swept sine wave response plot of an equalizer with all but the 1kHz markers switched on.



Swept filter response plot of the same equalizer using a pink noise source on trace A. Trace B is a plot of the comb signal less the 2kHz frequency. This plot was made using a 10dB window and adjusting the MARKER level control so the peaks appeared in the lower area.

Remember that the digital markers (negative spikes) operate only with up swept sine waves and the RECEIVE FUNCTION switch in positions 1,2,3,4,6;7,8,9,10 or 11. The COMB markers (positive peaks of adjustable amplitude) only operate with position 5 of the RECEIVE FUNCTION switch.

3.0 SPECIFIC APPLICATIONS

3.1.0 Acoustic Applications

3.1.1 Frequency Response.

Frequency response of acoustic transducers, such as microphones, speakers etc, require excitation with a wide band signal to avoid the problems that would be caused by sinusoidal signals. The latter waveforms introduce errors due to room modes and other effects not directly related to frequency response.

A wide band signal better approximates the natural use of the system (music or voice) with a controlled, known signal. A convenient wide band signal is pink noise. Such a signal has equal energy in each octave or percentage octave.

To generate frequency response plots three elements are required: A generating or transmitting transducer (usually a speaker), a receiving transducer (usually a microphone) and a medium connecting the two (a room or aneochic chamber). One or more of these is often an unknown. For example, to test a studio monitor system the speaker and room are unknown while a "flat" reference microphone is used.

The response is made by exciting the generating transducer with pink noise, receiving the noise signal with the receiving transducer and selectively tuning this signal with a narrow band pass filter and plotting the amplitude at the output of the filter versus its center frequency. The receiver configuration for such a measurement is commonly refered to as a spectrum analyser.

Pink noise, or more specifically Pseudo Random Pink Noise, by its very nature has random variations in its amplitude. These variations are most pronounced at the low end of the spectrum. To achieve meaningful results these amplitude variations must be time averaged over some period of time. As the time increases the amplitude will approach a fixed value.

The time averaging is achieved on the 4400 by using the SLOW RMS mode. This inserts a long time constant in the RMS detector. The sweep speed must be consistent with the time averaging. That is the RMS detector must be given time to settle before the filter tunes to a new frequency band.

Slow sweep speeds (32 seconds or longer) and SLOW RMS detection should yield an acceptable frequency response plot of the system under test.

The filter bandwidth used affects resolution of the resultant plot. Most acoustic measurements can be made with the control 1/2 or 2/3 open. This gives a filter bandwidth close to 1/3 octave. With the control fully clockwise the bandwidth is approximately 2%.

The shape of the filter must be specified with more detail than just bandwidth. The bandwidth (or percentage bandwidth or Q) describes the width of the filter, relative to the center frequency, where the slope is 3dB below the attenuation at the center frequency. Thus it only specifies the very tip of the peak. The slope of the skirts beyond this 3dB point are also important, however.

Various standard organizations agree on a rigid and rigorous definition of a full octave, 1/2 octave or 1/3 octave filter. The shape of the filter is defined by giving an actual plot of the limits on an XY attenuation vs frequency graph. Two or more classes are defined for each size of filter. The difference in the classes is chiefly one of skirt roll off characteristics.

It is virtually impossible or at least impractical to construct a filter with a rectangular shape, that is zero attenuation within the band and infinite attenuation outside the band. Practical filters have a bell shaped curve; minimum attenuation in the pass band and progressively greater attenuation outside the pass band. To meet the characteristics of acoustic filter sets defined by standard organizations requires a multiple pole filter. In a band pass filter these are realized by cascading several band pass filters in series with slightly staggered center frequencies. This gives good flatness (low ripple) at the top of the filter and steep filter skirt slopes.

The 4400 uses a single pole pair filter. A multiple pole filter with the characteristics of the actual filter used in the 4400 would be a few orders of magnitude more complex than the filter used. For example, three or more sections using six or more variable elements would have to track in the sweep mode over a 1000 to 1 range with better than 0.5% error. This is beyond the scope of the instrument.

In normal situations, however, the simplified filter used, due to high Q capabilities, gives excellent results. The skirt roll off characteristics have a very minimal effect on the readings or plots. The bandwidth of the filter is variable from approximately 70% to 3%. Using these figures alone the corresponding bandwidth would be approximately one-octave to one-thirtieth-octave. The foregoing discussion will clarify that this is not completely valid.

3.1.2 Reverb Time

Reverb time or RT-60 is the time it takes for an acoustic excitation in a room to fall 60 dB in amplitude. It is measured by exciting a room with a signal (usually pink noise), abruptly removing this signal and measuring the time it takes for the amplitude to fall from the original by 60dB.

Reverb time can be measured wide band, that is, without any spectral weighting or in a restricted bandwidth such as octave or third-octave.

The 4400 may be easily used to directly determine reverb time. The Generator should be set to PINK NOISE and this signal fed to the room using a power amplifier and flat speaker. A microphone should be connected via a simple low to high impedance transformer to the receiver input. Initially select WIDE BAND on the RECEIVER FUNCTION switch and a 60dB plotting window. Adjust amplitudes so with the room excited with a reasonably loud signal the plotter just paints a line on the top of the plot. Quickly cut the signal and observe the decay. Select a plotting speed slightly longer than the observed decay.

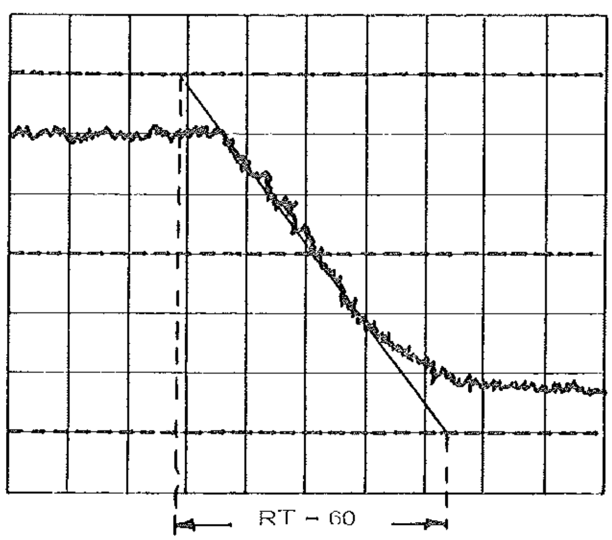


Fig. 3.1.2 Illustration of amplitude decay on removal of pink noise excitation. A 60dB window has been selected (6 divisions on the CRT) The total decay achieved is just over 40dB. By extrapolation the slop is extended to the full 60dB range and the time measured based on the sweep time.

In many cases it will be difficult or impossible to achieve a complete 60dB decay. 30 or 40dB may be the maximum for several acoustic and electrical reasons. However, the slope of the decay can be extrapolated to show the equivalent of a 60 dB decay. Under most situations the slope will be reasonably constant. Certain acoustic conditions may produce odd shaped or multiple slopes. These could be caused by anomolies in the room and should be investigated.

If the RECEIVE FUNCTION switch is put in the FIXED FREQ band pass mode the reverb time in a restricted bandwidth can be determined. By making several tests with different settings of the FREQUENCY control the RT at various parts of the spectrum can be determined.

3.1.3 TONE BURSTS

Tone bursts are very useful to evaluate the transient capabilities of a transducer. They can be easily generated on the 4400.

The GENERATOR FUNCTION is set to sine wave, the GATE to REPEAT and CYCLES mode and a suitable quantity of cycles selected. This signal is fed to the speaker under test and a microphone connected to the RECEIVER input will monitor the results. The Oscilloscope should be connected to the VERTICAL and TRIGGER connectors and both the SEND and RECEIVE buttons selected in the OSCILLOSCOPE group. This will put the transmitted steady state tone on the TRIGGER connector and the received burst on the VERTICAL connector. In this way the oscilloscope can trigger on the send signal and allow observation of the leading edge of the received signal.

3.2.0 TAPE RECORDER APPLICATIONS

3.2.1 Frequency response

There are various ways to generate frequency response plots of a tape recorder. Plots can be generated of just the reproduce portion or the total record-reproduce chain.

3.2.1.1 Reproduce response

Response can be checked in two ways. First by using a calibrated, standard test tape and second by magnetically coupling into the reproduce head.

In the first method a standard test tape is played and the plotter is set to WIDE BAND with a 10 or 20 dB window selected. If a slow sweep speed is used the amplitude at each reproduced frequency will be plotted with one trace. The whole test tape will draw a sky line picture of the machine response. Relative amplitudes can be seen at a glance without having to write down each reading. An oscilloscope photo gives a permanent record.

The second method uses the normal sine wave/ wide band plotting capabilities of the 4400. If the generator output were connected directly to the reproduce preamp input the reactive components of the reproduce head would not be included. Also, the extreme low level required by the preamp would introduce noise and other errors.

A convenient method is to couple magnetically directly into the reproduce head. A small coil connected to the 4400 output and oriented to couple into the gap of the head will give excellent results. The plotted curve will, of course, be the playback curve of the amplifier (NAB or other equalization).

3.2.1.2 Record/Reproduce Response

Frequency response can be determined in a variety of ways. If an accurate response over the full 20Hz to 20kHz range is required the AUTO START mode should be used.

First one or more sweeps are recorded on the tape with the GENERATOR FUNCTION switch in AUTO START REC. This will record a 1kHz cue tone when the 4400 is not sweeping.

Several sweeps could be recorded leaving a pause between sweeps (filled with 1kHz). Changes could be made as required before each sweep.

On playback the AUTO START REP mode would be used. The receiver would be set up in the normal mode for swept sine wave response plots. As a confirmation of accuracy some markers (Eg. 63Hz, 1kHz, 8kHz) should be switched on. The tape is played back including some of the 1kHz tone. This should cause the 1kHz SENSE led in the SWEEP control group to light. If it does not light the level is probably too low. Push and hold in the UP sweep button. During the 1kHz tone nothing will happen. As soon as the 1kHz tone disappears the sweep starts and, if the UP button is still being held, the memory will start to enter and plot a response trace. If there are several sweeps on the tape up to four of them can be loaded into the four available memory positions by selecting suitable MEMORY ENTER functions between sweeps.

Note that in AUTO START REP sweep start can only be initiated by a combination of interuption of 1kHz and the UP button being held.(see page 2-15)

There are times when an accurate full range plot is not as important as fast continuous information. In this case the MANUAL START mode should be used and CONTINUOUS sweep selected. Due to the time delay between record and playback (head spacing) the response plot will be shifted to the right. This will cut off the high frequency part of the range. This can be minimized by using fast tape speeds and/or slow sweep speeds. Alternatively, the 100Hz to 100kHz range can be used. This will give a plot from 100Hz to say 50kHz. Using markers, various sweep speeds and both sweep ranges the full 20Hz to 20kHz range can be covered in the CONTINUOUS mode.

This mode is particularly useful during adjustments. For example, to optimize bias or head alignment the effect of change will be rapidly seen. Seeing the whole spectrum in a plot avoids the potential errors of looking at only one or a few discrete frequencies.

3.2.2 PRINT THROUGH

Print through can be readily evaluated using the 4400. The procedure is as follows.

Record a series of short tone bursts on the tape with the burst repetition rate synchronized to reel revolutions. For example, select a 1kHz sine wave, 32 or 64 cycle gate mode and push the GATE START BUTTON once at each reel revolution.(Use MOMENTARY and SINGLE)

The tape is played back with the RECEIVER FUNCTION switch in WIDE BAND, a 60dB window selected and a slow sweep speed selected. The tone bursts should register as "full scale" steps in the plot. The print through will be lower steps displaced from the larger ones but at the same rate and in phase. Other random steps are noise, erasure etc. and not print through. The distance between the tops of the two steps in dB is the print through.

4.0 MODIFICATIONS AND CUSTOM NETWORKS

This section describes certain custom modifications that may be performed inside the 4400A and the construction details for weighting networks used on the meter amplitude measuring circuit.

4.1 Internal Modifications

The 4400A Sudio Test Set can be modified to meet particular requirements or suit personal preferences. Standard modifications include:

1. Pause duration during CONTINUOUS sweep.
2. AVERAGE or PEAK detection characteristics on amplitude meter.
3. Invalid display mode.
4. Oscilloscope outputs.
5. FAST speed during BASE LINE SENSE.
6. Marker height selection.
7. Filter input configuration.
8. Rear panel plotter output.
9. Display shift and magnify mode.

Before any modifications are made the reader should read the HANDLING PROCEDURES warnings in section 6 and be familiar with good practice in soldering, etc. Amber will not uphold warrenty claims on damages due to poor handling.

4.1.1 Pause Duration During Continuous Sweep

When in the CONTINUOUS sweep mode a short pause is generated between sweeps to allow the oscillator time to settle to 20Hz after switching from 20kHz. This pause can be 1,2 or 4 seconds in duration. The selection is done on the generator board by connecting two pads with a jumper wire.

PAUSE DURATION	CONNECT PADS
1 second	A and D
2 seconds	A and C
4 seconds	A and B

4.1.2 Average/Peak Detector

The meter board has three types of AC to DC converters used for amplitude measurements. An RMS to DC converter is normally used. A PEAK or AVERAGE responding detector may also be selected. The determination of PEAK or AVERAGE is made on the meter board by joining two pads located between U311 and U313. The pad on the left is connected to either PK for PEAK or AVG for AVERAGE. Of course, the calibration described in section 6 should be followed.

4.1.3 Invalid Display Mode

When the signal amplitude being measured is outside the measurement range of the meter circuit the digital display will normally flash and the HI or LO leds will indicate if the signal is above or below the capability of the meter. The status of the display during this condition can be set to flash at one of 3 rates, remain on or completely blank by connecting two pads near U31 on the meter board.

DISPLAY MODE	CONNECT PADS
No Change (ON)	A and V
Total Blank	A and W
Flash 5 Hz	A and X
Flash 2 Hz	A and Y
Flash 1 Hz	A and Z

4.1.4 Oscilloscope Outputs

The three OSCILLOSCOPE SELECT push buttons are configured so that when all three are out other signals can be routed to VERTICAL and TRIGGER output connectors. The choice is made on J10 located near the push button group. By connecting suitable pins of a 14 PIN header that can plug into J10 several signals can be selected. Pins 1 through 7 have the signals while pins 8 through 14 have the VERTICAL and TRIGGER connectors when all three buttons are released.

J10 PIN ASSIGNMENTS	
PIN NUMBER	SIGNAL
1	Plotter DC Input
2	$\overline{\text{SWEEP}}$
3	Rimac Clock
4	Preamp B Out
5	Filter Out
6	Preamp A Out
7	Trigger 250 Hz
8	Vertical BNC
9	Trigger BNC
10	Vertical BNC
11	Trigger BNC
12	Vertical BNC
13	Trigger BNC
14	Vertical BNC

4.1.5 Base Line Sense Speed

When the BASE LINE SENSE button is pushed the sweep will switch to a faster speed when the plot is on the base line, that is when data is outside the window selected. This faster speed is normally eight times the normal speed. The instrument can, however, be modified to change the fast multiple to 2,4,8, 16 or 32.

The FAST speed is set by a loop joining two points on the RECEIVER BOARD (lowest board). There are 10 solder holes located between U23 and U24. A loop is connected between any of the four terminals labeled F and one of A,B,C, D or E. C is the normal 8x connection. The following table shows the connections for various speeds.

Fast Speed	Connections to be Joined
2x	F and A
4x	F and B
8x	F and C
16x	F and D
32x	F and E

when changing loops use caution to prevent damage to the circuit board.

4.1.6 Marker Height Selection

The swept sine wave marker cause a sharp negative spike to be added to the trace. The height of this spike may be varied with loops on the RECEIVER BOARD.

Marker height is set by a loop between G and either A,B,C,D, or E. These terminals are located between U23 and U24. (some of the terminals are shared with base line sense.) The instrument is normally set with G and B connected. Other connections will give variations to the height of the spike.

Marker Size	Connect Pads
1/2 Full Scale	G and A
1/4 Full Scale	G and B
1/8 Full Scale	G and C
1/16 Full Scale	G and D
1/32 Full Scale	G and E

4.1.7 Filter Input Configuration

Some applications in acoustic testing require band limited pink noise as the source. In this case the filter of the receiver is moved to the generator path by connecting it between SOURCE and EXT IN. The preamp is set to the DUAL CHANNEL mode and the PLOTTER INPUT select switch is set to INPUT B. INPUT A and FILTER OUT are the input and output respectively of the filter. These are connected to SOURCE and EXT IN on the generator. INPUT B is now the wide band input to the plotter.

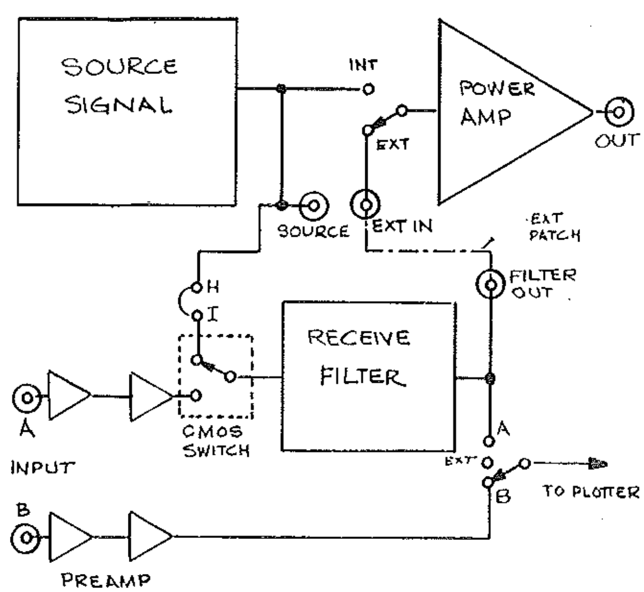
Although this signal routing is correct the levels are not ideal and the INPUT A and INPUT B levels must be the same.

There is a way to internally connect the SOURCE signal directly to the FILTER input. This frees the preamp for its normal function and allows the INPUT RANGE push button group to be set to whatever is convenient to the INPUT B signal. It also establishes the signal level through the filter to an optimum level.

An internal CMOS switch can be set to transfer the direct filter input from its normal preamp A output to SOURCE out. FILTER OUT is connected to EXT IN and one of the filter modes is selected on the RECEIVER FUNCTION switch. The plotter input is set to INPUT B.

To permit this path install a jumper between pads H and I on the receiver board. This connects the SOURCE signal to the switch. To transfer the filter input to SOURCE put a DC level of +7V to +10V on pad L. This will operate the CMOS switch. It may be desirable to install a miniature toggle switch to activate this CMOS switch.

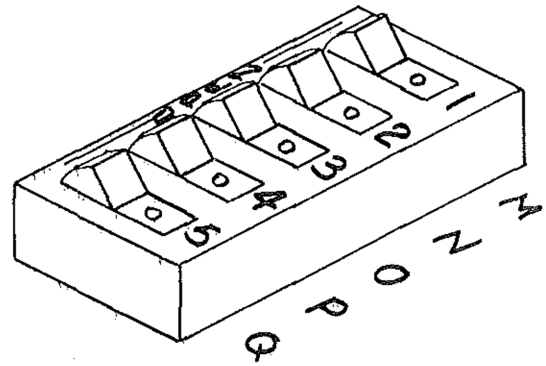
The SOURCE signal is routed via the HI jumper to reduce crosstalk. Even with the CMOS switch in the normal (INPUT A) mode some of the SOURCE signal would leak into the filter input. With the path between H and I broken the source of crosstalk is removed.



Simplified functional showing signal path for insertion of Receive Filter in Generator Send Signal.

4.1.8 Rear Panel Plotter Output

Pin 23 on J1 located on the rear panel may receive one of two signals: the DC level going into the A to D converter at the input to the plotter or the DC output coming out of the D to A converter at the output of the plotter. In the former case a DC voltage of 0 to +10V DC represents a 60dB input amplitude. 0 is the lowest signal amplitude while +10V is the highest. The DC voltage is linear in dB i.e. +5V is 30dB down, +8.3V is 10dB down, etc. In the case of memory data output mid scale (center reference line is 0V, the top reference line is approximately +3.5V and the lower reference line is -3.5 V.



SWITCHES SHOWN ON

The input OR the output DC may be selected by operating one of two positions on a 5 position miniature rocker switch.

Function Desired	Set Switch On
Plotter DC Input	1-M
Plotter Data Output	2-N

4.1.9 Display Shift and Magnify

The TRACE SHIFT rotary control in the DISPLAY group can actually produce any of three possible effects. Operation is initiated by pulling the knob and shifting by rotating the knob. (see page 2-16)

The choice of which of the three modes of operation will be available is determined by three of the five position of the rocker switch on the receiver board.

Function Desired	Set Switches On
DATA and Reference lines of PLOT B/D to shift when SHIFT control operated.	4-P, 5-Q
DATA only of PLOT B/D to shift when SHIFT control operated.	3-O, 4-P, 5-Q
DATA only of PLOT B/D to both shift and magnify x5 when SHIFT control operated	3-O

Amplitude Measurement Weighting Network.

Amplitude measurements are often made using some form of weighting. This may be to conform to some standard practice using a standard weighting curve, for example noise measurements using an "A" weighting curve or to measure a particular signal in the presence of another signal or noise.

The amplitude measuring circuit of the 4400 can accept several weighting networks to provide weighted amplitude measurements. An accessory 16 pin dual in line socket is provided on the meter board to accept standard 16 pin headers with resistors and capacitors. A dedicated high quality operational amplifier is used in conjunction with these passive components to form precision filter networks which may be inserted in the measurement path by pushing the WGHT push button on the instrument.

Specific applications will dictate the use of particular types of filters. For example, to reject hum components a high pass filter with a cut off frequency of around 400 Hz may be required. Or to measure ambient noise in a noisy environment the standard "A" curve may be required.

Several types of standard filters are described here along with details of how to determine component values to provide specific parameters. In addition to the networks presented here several others may be derived using classic filter design technique and implemented in a similar fashion. The configuration of the accessory socket, dedicated op amp and terminations provide near ideal filter conditions: low source impedance, extremely high op amp input impedance and wide op amp bandwidth.

For best results resistors should be 1/4 watt metal film with ±1% tolerance, capacitors should be ceramic plastic film or mica with ±10% or better tolerance.

3rd Order Butterworth HIGH PASS and LOW PASS filter networks.

Three pole filters may be realized by using three resistors and three capacitors as shown in the instructions. The component location determines the filter character while it values the -3dB point.

Capacitor values should lie between 200 pf and 0.5 μf while resistor values should be between 1KΩ and 400KΩ. Values for several frequencies are shown. Component values for other frequencies can be found by interpolation or extrapolation or using the 1Hz values and the following procedure:

LOW PASS

Divide the capacitor values shown by the desired -3 dB frequency (fc). If the resulting capacitor values are too small multiply each by a constant and devide the 10KΩ resistor value by the same constant. If the capacitor values are too large divide each by a constant and multiply the 10KΩ resistor value by the same constant.

HIGH PASS

Divide the resistor values shown by the desired -3dB frequency (fc). If the resulting resistor values are too small multiply each by a constant and divide the 0.01 uf capacitor value by the same constant. If the resistor values are too large divide each by a constant and multiply the 10KΩ resistor value by the same constant.

Example:

Suppose we want a 60Hz high pass filter:

$C_1 = C_2 = C_3 = 0.01\ \mu f$

$R_1 = 11.43\ M\Omega \div 60 = 190.5 K\Omega$

$R_2 = 78.63 M\Omega \div 60 = 1.310\ M\Omega$

$R = 4.49\ M\Omega \div 60 = 74.83\ K\Omega$

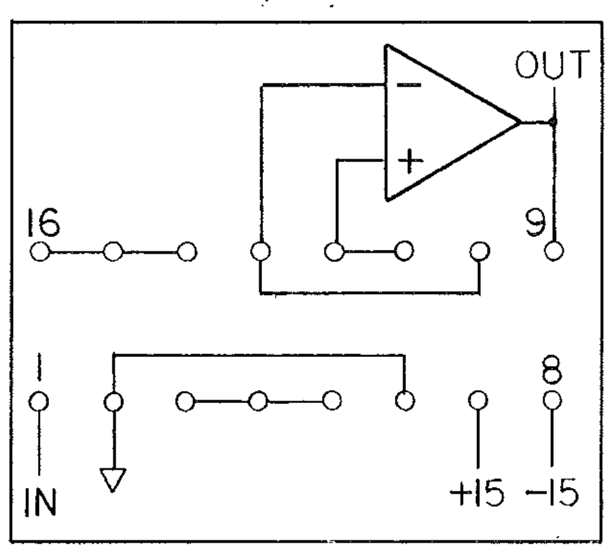
R_2 is over 1MΩ and should be scaled to about 20% of this value. Choosing a standard value capacitor of 0.047 μf or 4.7 times the previous value we divide all resistors by 4.7 to arrive at the final values:

$C_1 = C_2 = C_3 = 0.047\ \mu f$

$R_1 = 190.5 K\Omega \div 4.7 = 40.5\ K\Omega$

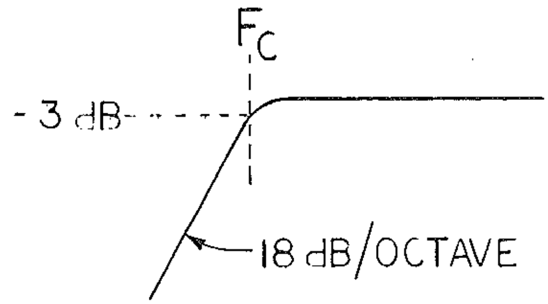
$R_2 = 1.310\ M\Omega \div 4.7 = 279\ K\Omega$

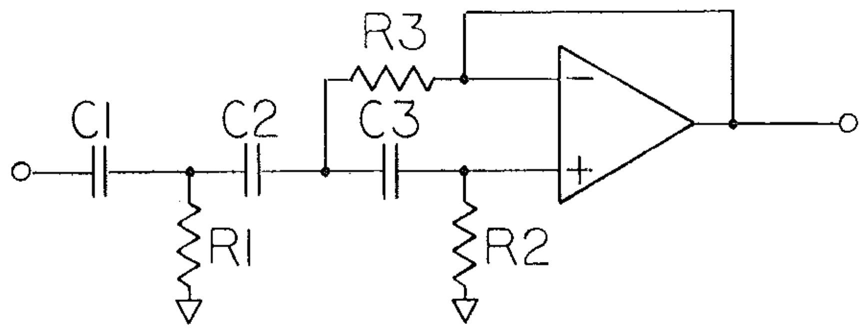
$R = 74.83\ K\Omega \div 4.7 = 15.9\ K\Omega$

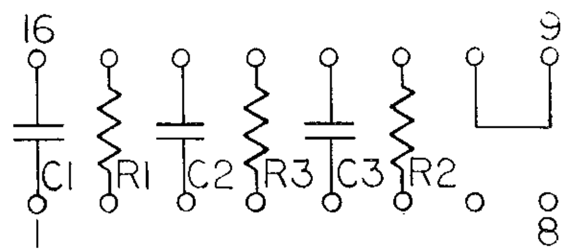


Accessory Socket Wiring

3 POLE HIGH PASS FILTER (BUTTERWORTH)

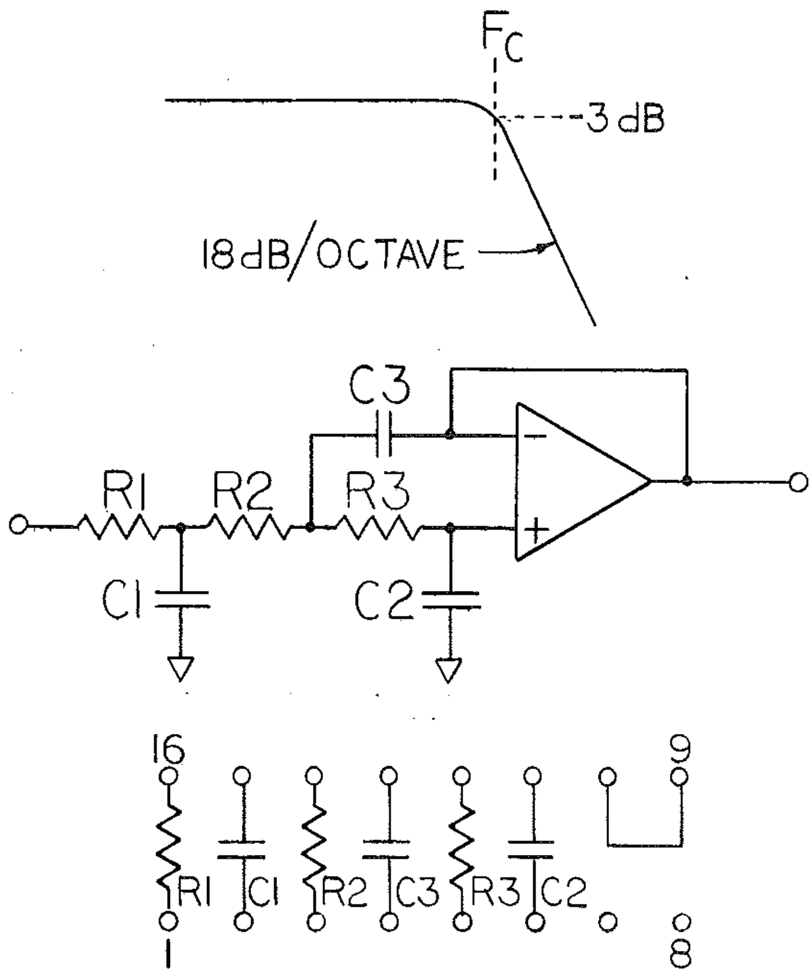






COMPONENT VALUES FOR HIGH PASS FILTER				
Fc	R_1	R_2	R_3	$C_1 = C_2 = C_3$
20 Hz	26.1 KΩ	178 KΩ	10.2 KΩ	0.22 uf
30 Hz	17.4 KΩ	118 KΩ	6.81 KΩ	0.22 uf
50 Hz	48.7 KΩ	332 KΩ	19.1 KΩ	0.047 uf
100 Hz	24.3 KΩ	169 KΩ	9.53 KΩ	0.047 uf
400 Hz	28.7 KΩ	196 KΩ	11.3 KΩ	0.01 uf
1kHz	22.6 KΩ	158 KΩ	8.87 KΩ	0.005 uf
10kHz	24.3 K	169 KΩ	9.53 KΩ	470 pf
1 Hz	11.43 MΩ	78.63 MΩ	4.49 MΩ	0.01 uf

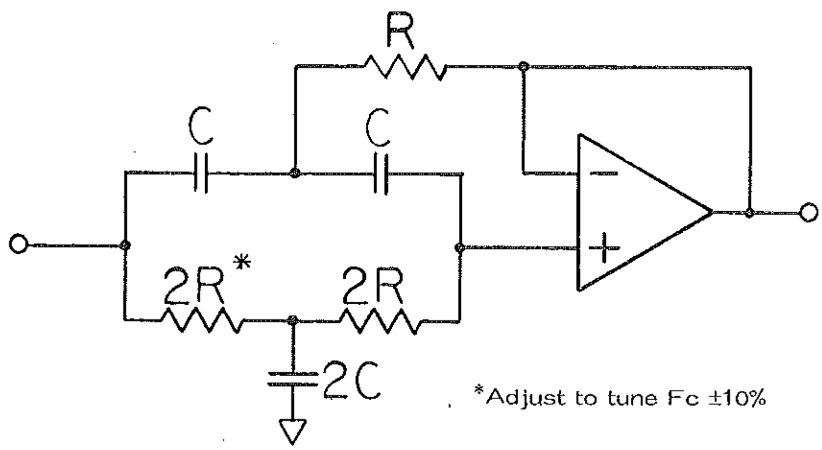
3 POLE LOW PASS FILTER (BUTTERWORTH)



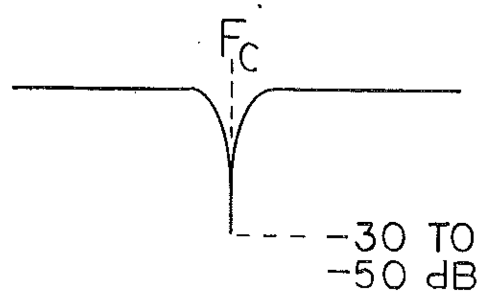
COMPONENT VALUES FOR LOW PASS FILTER

Fc	C_1	C_2	C_3	$R_1 = R_2 = R_3$
100 Hz	0.047 uf	0.0068 uf	0.12 uf	47.5 KΩ
1kHz	0.022 uf	3300 pf	0.056 uf	10.0 KΩ
10kHz	2200 pf	330 pf	5600 pf	10.0 KΩ
20kHz	2200 pf	330 pf	5600 pf	4.99 KΩ
30kHz	2200 pf	330 pf	5600 pf	3.32 KΩ
50kHz	2200 pf	330 pf	5600 pf	2.00 KΩ
100kHz	2200 pf	330 pf	5600 pf	1.00 KΩ
1 Hz	22.15 uf	3.221 uf	56.44 uf	10 KΩ

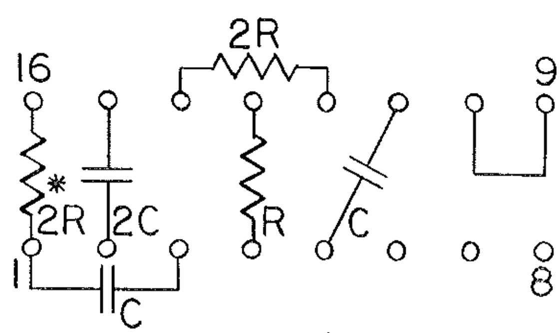
2 POLE "TWIN TEE" BAND REJECT FILTER



*Adjust to tune Fc ±10%



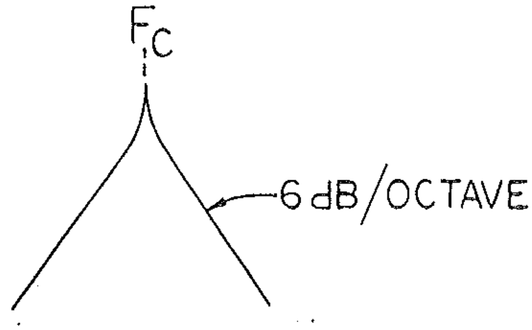
$$Fc = \frac{1}{4\pi RC}$$

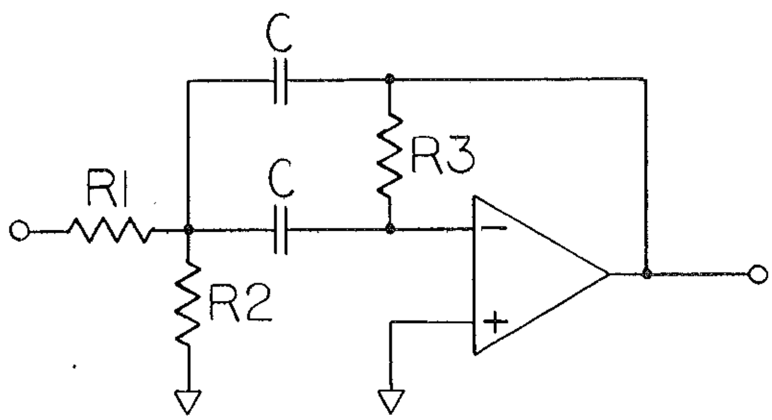


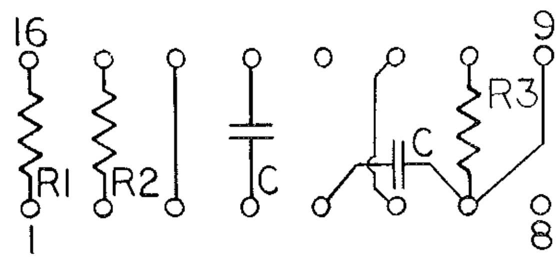
COMPONENT VALUES FOR BAND REJECT FILTER

Fc	R	2R	C	2C
60 Hz	26.7 KΩ	53.6 KΩ	0.05 uf	0.1 uf
120 Hz	13.3 KΩ	26.7 KΩ	0.05 uf	0.1 uf
400 Hz	20.0 KΩ	39.2 KΩ	0.01 uf	0.02 uf
1kHz	15.8 KΩ	31.6 KΩ	0.005 uf	0.01 uf
10kHz	2.43 KΩ	4.87 KΩ	3300 pf	6800 pf

SINGLE POLE PAIR BANDPASS FILTER







For Gain at Fc = −1 $\quad R_3 = 2R_1$

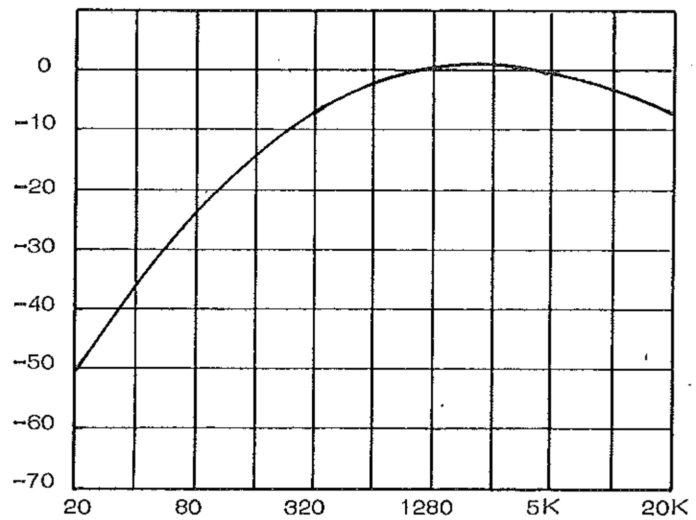
$$\text{Filter } Q = \frac{F_c R_3 C}{2}$$

$$F_c = \frac{1}{\pi}\sqrt{\frac{R_1 + R_2}{2R_1^2 C^2 R_2}}$$

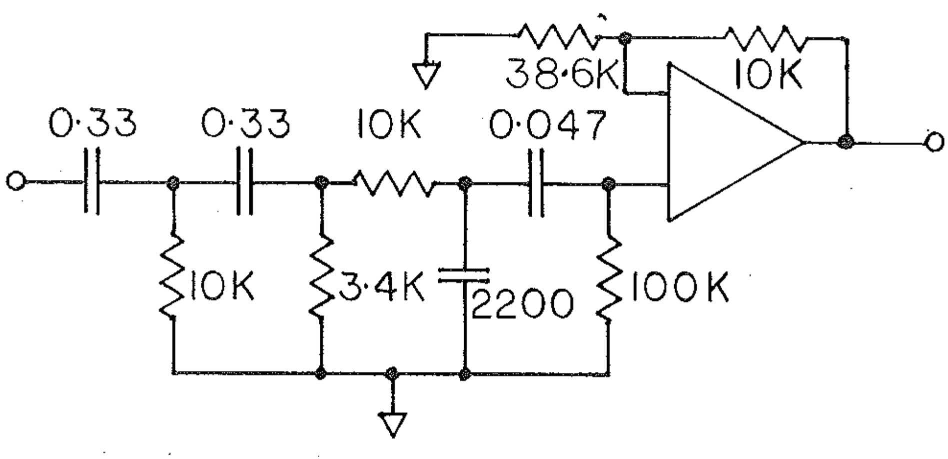
Example: For Q = 10
Fc = 1kHz

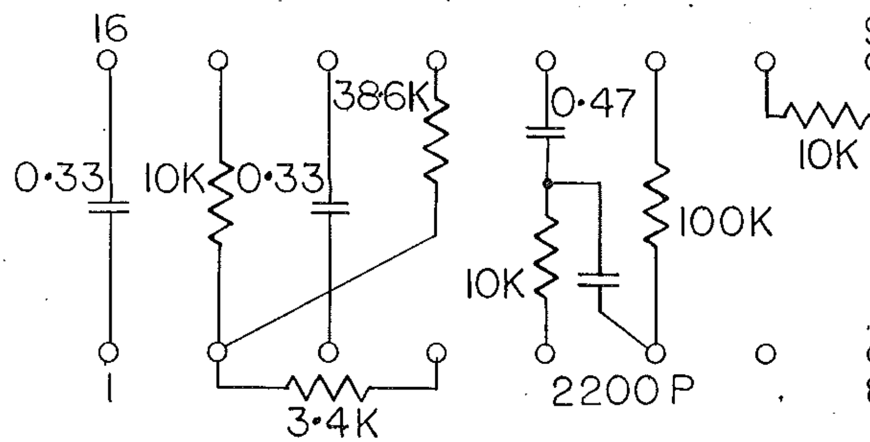
C = 0.1 µf
R_1 = 10KΩ
R_2 = 530Ω
R_3 = 200KΩ

"A" WEIGHTING NETWORK

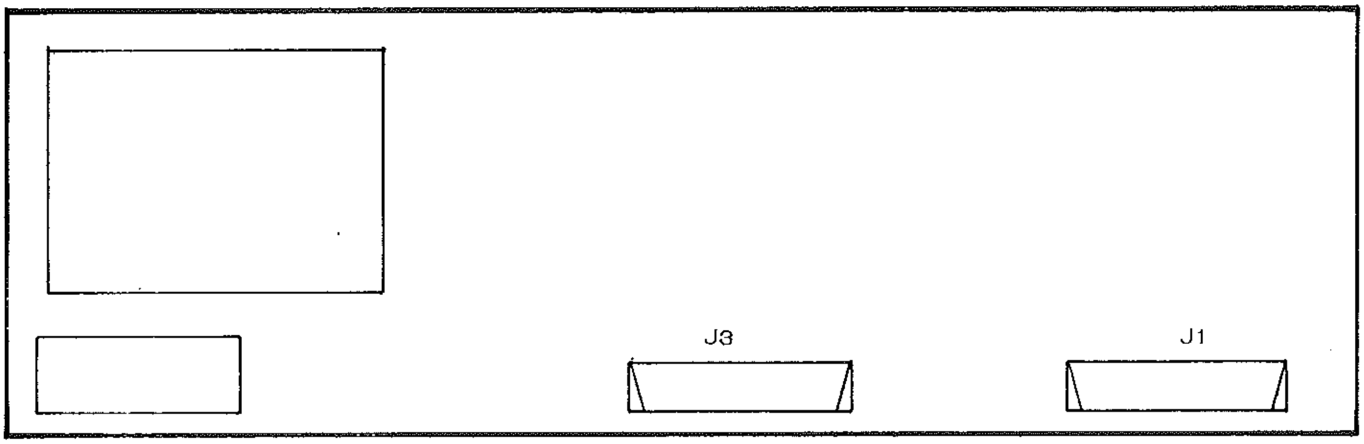


"A" Weighting Network Frequency Response

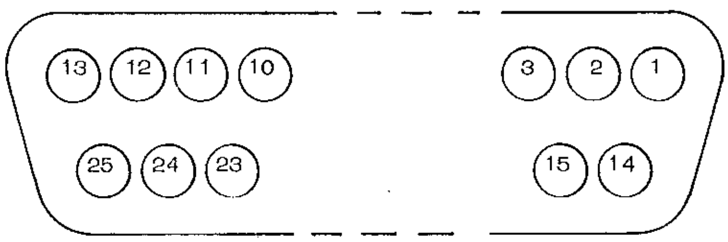




4400A REAR PANEL CONNECTOR DESIGNATIONS



REAR PANEL VIEWED FROM REAR



25-PIN FEMALE CONNECTOR VIEWED FROM MATING SIDE. (AS SEEN ON REAR PANEL OF 4400A)

Two 25-Pin D-Type connectors are provided on the rear panel to interface to various Amber accessories. Various logic outputs and command inputs are available as well as unregulated power. The tables show the functions of these connectors.

The first column of numbers refers to the actual numbers on the connectors. (Either on the rear panel or a mating connector). The second column of numbers refers to the equilivent number of the flat cable internal to the 4400A. These numbers appear on all schematics in this manual and other documentation.

As the D-Type connector and the flat cable system evolved from different segments of the industry their numbering sequence does not correspond.

Note that these rear panel connectors are intended for use with Amber accessories only. They should not be considered general purpose control inputs and output as they are neither buffered nor protected. Incorrect voltage or current levels could permantly damage internal circuitry on the 4400A and such damage will not be covered under warranty. The tables shown here are a guide only and should not be considered as definitive use instructions.

J1 PIN ASSIGNMENTS — ACCESSORY CONNECTOR

J1 Designations	Flat Cable Designations	Function	Voltage Level/ Operation
1	25	SWEEP	SWEEP = -7V STOP = +7V
2	23	Plotter DC or Memory Data Out	DC = 0 to +10V; DATA = ±4V
3	21	XY Mode ON/SET	PULL TO +5V to Set; +5V = XY Mode
4	19	SWEEP Up Start	Pull To -7V To Start; +7V Normal
5	17	1.024 MHz Master Clock	0 to +10V Clock
6	15	RIMAC Bit 8 MSB	Low = -7V; High = +7V
7	13	RIMAC Bit 6	Low = -7V; High = +7V
8	11	RIMAC Bit 4	Low = -7V; High = +7V
9	9	RIMAC Bit 2	Low = -7V; High = +7V
10	7	+10V Regulated	+10V for reference
11	5	GROUND	
12	3	-18V Unregulated	Current Drain 40MA
13	1	-9V Unregulated	Current Drain 40MA
14	24	*Plotter Logic In/Out	Low = 0V; High = +5V
15	22	*MEMORY Enter Select	Low = 0V = B/D ; High = +5V = A/C
16	20	62.5Hz Clock Low freq Sync	Low = 0V; High = +5V
17	18	*Variable RIMAC Clock	Low = -7V; High = +7V
18	16	RIMAC Bit 7	Low = -7V; High = +7V
19	14	RIMAC Bit 5	Low = -7V; High = +7V
20	12	RIMAC Bit 3	Low = -7V; High = +7V
21	10	RIMAC Bit 1 LSB	Low = -7V; High = +7V
22	8	External GATE	High = Nor = +7; Pull to -7V for On
23	6	GROUND	
24	4	+18V Unregulated	Current Drain 40MA
25	2	+9V Unregulated	Current Drain 40MA
	26	Not Used	

* High impedance line (10KΩ); May be forced to new value.

J3 PIN ASSIGNMENTS — DIGITAL DISPLAY

J3 Designations	Flat Cable Designations	Function	Operation
1	25	U47 SCAN OSC	500Hz 1/4 Duty
2	23	DECIMAL POINT	H = +10V At Digit Strobe for D.P.
3	21	BCD PRESET BIT B	H = +10V at digit Strobe to pre-set
4	19	EXTERNAL DEVICE ENABLE	+10V when external selected
5	17	LOAD COUNTER	H = +10V to Load pre-set
6	15	BCD PRESET BIT A	H = +10V at Digit Strobes to pre-set
7	13	COUNT	H = +10V to increment/decrement
8	11	STORE	H = +10V = Display Hold; L=0V=update
9	9	LEADING ZERO BLANKING	L = 0V For Blanking
10	7	DIGIT 6 STROBE	H = +10V During digit 6 Strobe
11	5	+10V REGULATED	+10V Reference
12	3	BCD OUTPUT BIT B	H = +10V at Digit Strobe
13	1	BCD OUTPUT BIT D	H = +10V At Digit Strobe
14	24	BCD PRESET BIT C	H = +10V At Digit Strobe to pre-set
15	22	BCD PRESET BIT D	H = +10V Digit Strobe to pre-set
16	20	COUNT INHIBIT	H = +10V = Count Input Inhibited
17	18	CLEAR	H = +10V = Reset all digits to zero
18	16	UP/DOWN	H= +10V to increment; L=0V to decrea.
19	14	SET	H = +10V = Nor; L=0V = forced to MSD
20	12	MINUS SIGN	0V=Off; +10V VIA 182Ω = On
21	10	ZERO COUNT	H = +10V when all digits = 0
22	8	PLUS SIGN	H = +10V = Nor; L=0V=On
23	6	GROUND	
24	4	BCD OUTPUT BIT A	H= +10V At Digit Strobe
25	2	BCD OUTPUT BIT C	H = +10V At Digit Strobe

5 THEORY OF OPERATION

5.0 Introduction

This section is a detailed description of the operation of the various circuits used in the 4400A Multipurpose Audio Test Set. Reference is made throughout the text to the schematics contained in section 8 of this manual. In addition, there are useful tables and other information contained in section 6 - Maintenance. Reference should also be made to Section 4 - Modifications.

5.1 System Interconnection

The 4400A Mainframe consists of a cabinet assembly which includes a rear panel and front panel.

The rear panel includes the power transformer, AC power connector and two multi-contact accessory connectors. The front panel contains a 10 station push button switch assembly and attached harness and 9 BNC connectors with attached harness.

The AC power connector incorporates an international standard power receptacle, a fuse and a facility for selecting any of four voltage taps on the transformer primary. The configuration is such as to afford maximum safety. Neither the fuse nor the voltage taps can be changed without first unplugging the AC power cord and the voltage tap cannot be changed without first removing the fuse. The table below shows the proper fuse and voltage selection for various line voltages.

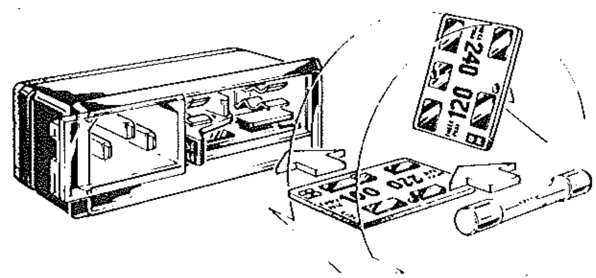
The power connector also incorporates an LC RFI filter to reduce the possibility of RF signal being introduced into the instrument by way of the power cord.

The power transformer provides multiple, taped primaries to accomodate the various line voltages. It contains two tapped secondaries. One of these secondaries supplies the raw power to the bulk of the instrument. The second secondary supplies the power to the output amplifier only. This permits the output amplifier to be completely floated with respect to the instrument itself. An electrostatic shield is provided between each secondary and between the secondary and the primary.

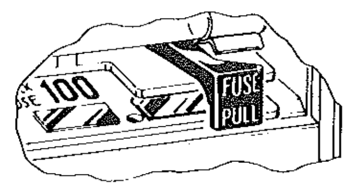
The construction of the transformer affords minimum interference. It uses a "C" core winding technique and is located in a metal enclosure to minimize radiation.

The BNC connectors are insulated from the front panel to prevent system ground loops. The connector ground and center conductor is fed via a shielded cable to a miniature connector at the signal location on the circuit board itself.

VOLTAGE AND FUSE SELECTION					
Input Voltage	Max	105	126	231	252
(48 to 440 Hz)	Min	90	108	198	216
Voltage Selection		100	120	220	240
Fuse Selection		500 mA		250 mA	



Operating voltage is shown in VS&F Connector window.



5.2 FRONT END and LINEAR RAMP GENERATOR

5.2.1 Front End or Preamp

The input to the receive portion of the 4400 consists of a switched gain differential/dual channel amplifier. This circuit is realized using five operational amplifiers U111, U112 U213, U313 and U314. The configuration provides a differential or dual channel input, three switch selected gains, constant input impedance, wide bandwidth and low noise.

The gain of the front end is changed by selectively changing the gain of each amplifier to provide the best dynamic range and lowest noise floor. The gain is changed by switching the feedback resistors using CMOS switches.

U111 and U112 are used in the inverting mode. In the DIFFERENTIAL mode their respective outputs are connected to the differential inputs of U213 which in turn is connected to the inverting input of U314. Thus the output of U314 (PREAMP "A" OUT) is the difference of the signals presented to INPUT A and INPUT B.

In the DUAL CHANNEL mode the respective outputs of U112 and U111 are connected to the inverting inputs of U314 and U313. Thus the outputs of U314 and U313 are signals corresponding to INPUT A and INPUT B. In the center position of the toggle switch, U213 configured as a unity gain inverting buffer, is inserted between U112 output and U314 input. This gives a 180° phase inversion to the PREAMP "A" OUT signal.

The input signal is coupled via two 20KΩ resistors and capacitors to the inverting inputs of the input op amps. The input capacitors (like coupling capacitors used elsewhere in the instrument) are polarized tantalum capacitors connected back to back to behave similar to a non-polar capacitor. Their value is chosen to preserve the low frequency response of the instrument.

The front end can be set to give one of three gains: -17dB , +13dB and +43dB. The first stage (U112 U111) can be set to -17dB or +13dB gain while the second stages (U314, U313) can be set to 0dB or +30dB gain.

The large input voltage swings possible (+30dBm = approx ±35V) require that the first stage operate in the loss mode when the instrument is set to the +30dBm to -30dBm range. This ensures that the voltage swing at the output of the first stage will be within the capabilities of the op amps. This loss is set up by considering the input resistance of 20kΩ and a feedback resistance of 90.9KΩ in parallel with approximately 2.9KΩ. This gives a ratio of approximately 0.14 or -17dB.

The mid range (0 to -60dBm) requires a gain of +13dB. This is set by an input resistance of 20KΩ and a feedback resistance of 90.9KΩ giving a ratio of approximately 4.5 or +13dB.

The low range (-30dBm to -90dBm) requires a gain of +43dB. This is set by a gain of +13dB in the first stage and +30dB in the second stage. The second stage input resistance is 4.99KΩ with a feedback resistance of 158kΩ giving a ratio of approximately 31.6 or +30dB.

The four CMOS switches are all configured to operate at ground or virtual ground to minimize distortion and maximize voltage swing capability.

Capacitors C22, C21, C20, C37, C48, C49, C41, C46, C47 and C40 neutralize the stray input capacitances of the op amps and ensure stable operation. Their values have been chosen to prevent high frequency oscillation while preserving a wide bandwidth.

5.2.2 Overload Detector

U49 is a level comparator that senses an excessive signal on either U314 or U313 output. Pin 2 has a reference voltage of 2.5V derived by the voltage divider R103 and R104 and the +15V rail. R107, CR62 and R106, CR61 rectify the signals at U314 pin 6 and U313 pin 6 respectively and present the higher of these across R105 and pin 3 of U49. C69 provides some filtering and "peak holding". When the analog signal exceeds the preset value U49 changes state, pin 3 goes high turning on Q16 and lighting the LED.

5.2.3 Linear Ramp Generator

This circuit generates a repetitive (500Hz) linear reference ramp for use with the A to D comparator of the digital plot recorder (schematic 7 location A-9). The start and stop points of the ramp are determined by the buttons activated in the WINDOW SELECT push button group. This ramp has a maximum amplitude of +10.0V DC to 0 V DC (60dB window) and a minimum amplitude of 1.67 V DC within this 10V range.

To generate the linear ramp, a capacitor is rapidly charged to a specific reference voltage (ramp start voltage) and discharged into a precision current sink. The choice of plotting window determines the ramp start voltage and discharge current.

The precision +10.00 V DC reference voltage generated on the meter board is inverted to -10.00V DC by U76, a unity gain inverting buffer. This -10.00 Volts is placed across the series voltage divider composed of R177 thru R182. This forms voltage levels at specific junctions of -10.00, -8.33, -6.67, -5.00, -3.33 and -1.67 V DC. One of these values is selected by the WINDOW SELECT group to appear at the left end of R145 and cause a particular current to flow into pin 2 of U83. RV6, a trim adjustment can add to or subtract from this current as can RV19, if S6 is closed. This produces a net voltage at U83 pin 6 with nominal values of +10.00V, +8.33V, +6.67V, +5.00V, +3.33 or +1.67V all ± any correction afforded by RV6 and/or RV19.

500Hz from the counters in the DIGITAL PLOT RECORDER (schematic 7) switches Q17 at a 500Hz rate causing contacts 3 and 4 of U73, a CMOS switch to open and close at a 500Hz rate. When closed they rapidly charge C92, a precision stable capacitor to the ramp start voltage. When they open, they allow C92 to discharge into Q19 and the particular combination of R193 thru R198 selected. The action of Q19, U84 and its surrounding circuitry causes C92 to discharge with a constant current, which generates a linear slope.

The WINDOW SELECT push button group S7 through S13 select one of 21 possible plotting windows. Two of the seven buttons are pushed to select the window which in turn sets the ramp slope and start points. The highest button pushed in the group, by chain connection of the switches, determines the ramp start voltage and hence the window ceiling value. The spacing between the two push buttons selected determines the value of the discharge resistance and thus the discharge current. This sets the ramp slope and therefore the ramp final value or window floor. The six 1MΩ resistors and interconnected switch contacts select various parallel combinations of resistors. For example, suppose the 0 to -60 dBm range is selected. If the -10 and -20 dBm buttons were pushed, S8 and S9, a single 1MΩ resistor would be selected causing a low discharge current and 1.67V overall ramp amplitude starting at 8.33V and falling to 6.67V If, on the other hand, -20 and -40 were pushed, S9 and S11, resulting in a 20dB window, two 1MΩ resistors would be selected in parallel giving a discharge resistance of 500KΩ. This would generate an overall ramp amplitude of 3.33V and the S9 button would start the ramp at 6.67V which would mean it would finish at 3.33V. If 0 and -60 were selected, all 1MΩ resistors would be put in parallel for a net value of 167KΩ, a ramp amplitude of 10V and a start point of +10.00V and end point of 0.00V. Other combinations will follow a similar pattern.

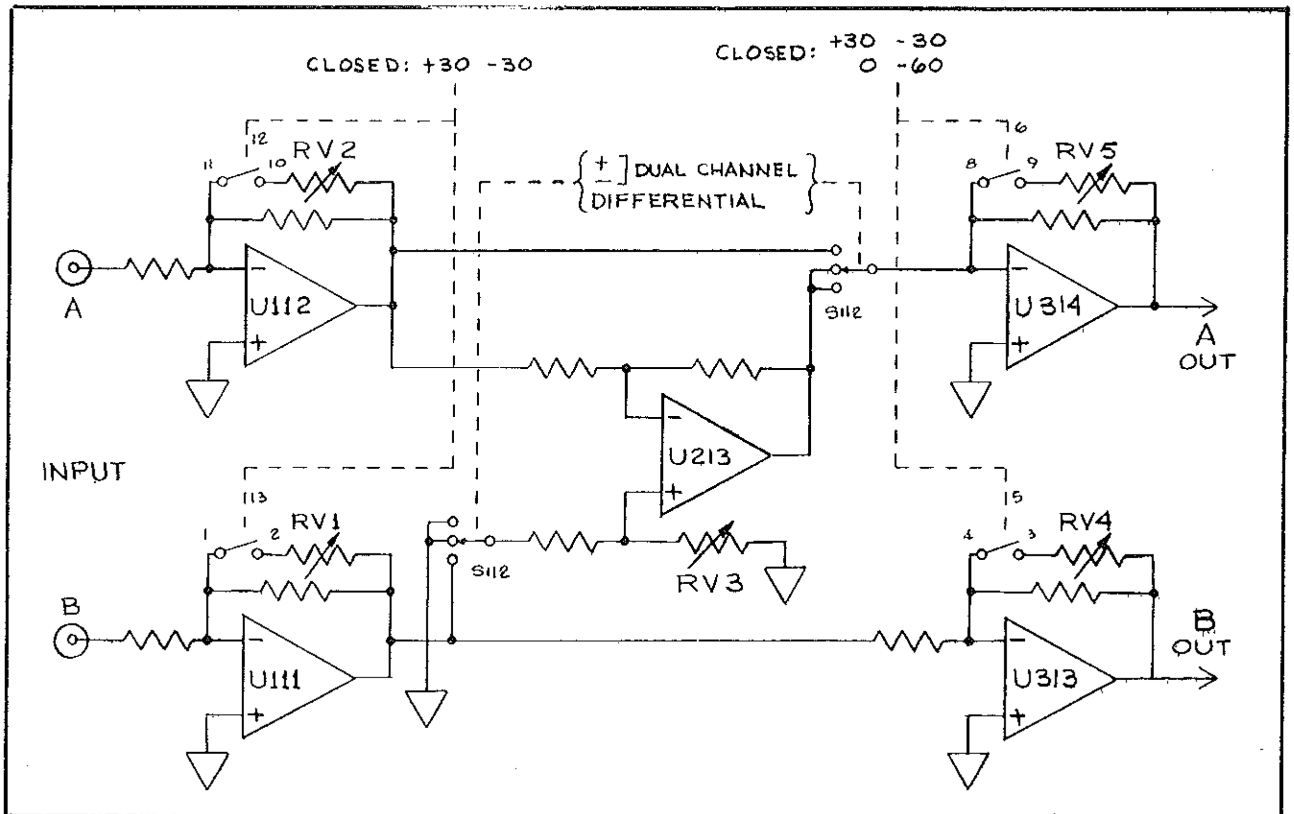


FIG 5.2.1 FRONT END SIMPLIFIED SCHEMATIC

TABLE 5.2.1 FRONT END GAIN

INPUT RANGE SELECTED		+30 −30	0 −60	−30 −90
U112, U111 GAIN		−17 dB	+13 dB	+13 dB
U314, U313 GAIN		0	0	+30 dB
FRONT END OVERALL GAIN		−17 dB	+13 dB	+43 dB
RANGE CODE LSB (J2-22)		L = −7V	L= −7V	H = +10V
RANGE CODE MSB (J2-21)		L = −7V	H= +10V	L = −7V
U214 CMOS SWITCH CONNECTIONS CLOSED		10 to 11; 1 to 2		
		8 to 9; 4 to 5	8 to 9; 4 to 5	
U214	12, 13	H = +7V	L = −7V	L = −7V
CONTROL PINS	5, 6	H = +7V	H = +7V	L = −7V

5.3 DIGITALLY PROGRAMMED FILTER

U712, U88 and U710 form a STATE VARIABLE filter which may be set to operate in the BAND PASS, BAND REJECT, HIGH PASS or LOW PASS mode by the RECEIVER FUNCTION switch S21.

U88 and U710 (B-6 & B-2) are the two integrators of the state variable network, and U712 the difference amplifier. Front panel control S22 (20Hz -20kHz/100Hz - 100kHz) selects either a 820 pf feedback capacitor for each integrator or 820 +3300 = 4120 pf, to produce the appropriate frequency ranges.

The effective input resistor value of each integrator is controlled either by front-panel potentiometers (one dual-ganged pot for coarse, one for fine) or in the SWEEP mode by digitally programmed attenuators controlled by the RIMAC code.

Since an integrator presents a virtual ground to the "low" end of the input resistor, the effective value of that resistance can be controlled either by varying the resistor value itself or by dividing the voltage applied to the high end. Either method varies the current flowing into the integrator input junction. Both methods are employed, in both the manual tune and swept tune modes.

Manual control is achieved by ganged potentiometers RV21, RV22 (fine) and RV24,RV23 (coarse). CMOS switches U86/6 and U87/6 are closed for manual tuning.

For digitally programmed control, six bits of the RIMAC code control the dual 4-input multiplexers U511 and U512, U513. The two halves of each multiplexer are in the corresponding locations of the input circuits of the two integrators, and are switched in parallel ("ganged") by the two bit code control applied to pins 9 and 10. The switches select the tapping points of the three voltage dividers in each input circuit. The two MSB commands control switch U514 to select one of four series resistors for each integrator. To cover a range of 20Hz to 20kHz (or 100Hz to 100kHz) requires the effective resistance to vary by a factor of 1000 or 60dB , in logarithmically spaced steps, ie constant dB per step.

To do this, the two MSB's of the RIMAC code control U514 to change the input resistance in 15dB steps; the next two bits switch U513 to divide the signal voltage in 15 ÷ 4 = 3.75dB steps; the next two bits control switch U512 to divide in 3.75 ÷ 4 = 0.9375dB steps; and the two LSB's switch steps of 0.9375 ÷ 4 = 0.234dB. Each divider output is buffered by a unity-gain LM310 follower to drive the top of the succeeding divider.

In the sweep mode the manually controlled input circuits are disabled by opening switches U87/6 and U86/6 and the INHIBIT line (pin 6) of U514 is held low to enable that switch. CR15 thru CR26 and R52 thru R56 and R109 freeze U511, U512 and U513 in their minimum attenuation mode during manual operation. The six LM310 voltage followers are left in the loop during manual operation so the filter will behave the same as in the swept mode. These followers add some phase shift and the high frequency characteristics of the filter would change if they were excluded from the circuit. However, in the manual mode the RIMAC may be cycling for other circuit requirements and must be inhibited from changing the state of the attenuators. The specified diodes and resistors accomplish this.

R245 and RV20 form the shunt element of internal feedback in the filter and determine the Q or quality factor of the filter. Variable resistor RV20 allows the Q or percentage bandwidth to take values from approximately 70% of center frequency to as low as 2% of center frequency. 2% bandwidth is equivalent to a Q of 50.

CR53 and CR54 form a simple AGC network to limit the positive feedback in FILTER OSCILLATE modes and keep the distortion low and thus indicate accurate center frequency.

Variable capacitor CV1 provides high frequency compensation to null out stray capacitances and resulting phase shifts at high frequencies. Absence of this capacitor would cause "Q" enhancement, center frequency shift, filter shape factor distortion and eventual oscillation as the center frequency was increased.

U89 is a CMOS switch used to change the configuration of the filter and cause oscillation. In the normal (filter) mode the positive feedback path R241, R240, CR53 and CR54 is disconnected and the output resistor R239 is grounded. Also "Q" feedback is via R243 and R242 to the non inverting input of U712 with R245, RV20 and R252 forming a variable shunt to adjust the amount of feedback and hence the Q. The source signal is coupled to the filter input via U713 12-5 also to the non inverting input of U712.

In the FILTER OSCILLATE mode, the input signal is disconnected by U89/14 changing from pin 12 to pin 13, a fixed Q feedback is established by R260 and R244 and positive feedback via R241 and R240 is provided from U88 output to U712 inverting input. CR53 and CR54 provide a limiting or AGC function. Signal output is taken from U88 pin 6 via R239 and coupled into the summing bus of U810.

U87/12 connects a COMB signal from the GENERATOR section to be mixed with the input signal when the MARKER is selected. The amplitude is set by RV18.

U89/9 can change the filter input from PREAMP A OUTPUT to generator SOURCE. If option pads H and I are connected and pad L is pulled to +7V, U89/9 will effect this change.

5.3.1 Post Filter Gain

Amplifier U810 (A-4 on the schematic) serves a variety of purposes. Using CMOS switch U86 and U87 it selects appropriate outputs from the three stage filter. In the Band Reject mode the High Pass and Low Pass modes must be summed together. As U80 is operating in the inverting mode it easily becomes a summing amplifier.

Feedback resistor R233 is normally in parallel with R229 giving an effective feedback resistance of 10KΩ. In conjunction with the 10kΩ input resistors this sets U810 to unity gain. When POST FILTER GAIN is selected (and available) U86 pins 10 and 11 open giving a feedback resistance of 316kΩ. This provides a gain of +30dB.

C114 and R232 are compensation components to ensure high frequency stability. C61 and C116 also preserve high frequency stability.

The signal at the output of U810 (FILTER OUT) is coupled via R236 and CR51 to R235, C119 and the non inverting input of U811. This forms a half wave rectifier and produces a DC voltage across C119 representative of the average value of the AC voltage at FILTER OUT. The negative input of U811 is connected to a reference voltage formed by a resistor divider R230,231. When the AC signal exceeds the capability of U810 the resulting DC voltage exceeds the reference voltage and causes U811 to change state, pin 6 goes high, current flows in R237 saturating Q24 and lighting the LED CR66.

5.4 FUNCTION SWITCH LOGIC, POWER REGULATORS, INPUT RANGE SWITCH

5.4.1 Function Switch

The Receiver FUNCTION switch, S21, in conjunction with logic formed by U79, U510, U611, U612 and diodes CR38 to CR50 converts the 11 position front panel rotary switch into proper commands to select filter modes and receiver operation.

The switch static logic is powered from ±7V to generate commands of this voltage to drive the CMOS analog switches. Pull down resistor network U85 holds gate inputs at -7V except when the wiper of S21 pulls them to +7V (logic high).

The first five positions of the switch set up various operating modes of the State Variable Filter. The four modes, band pass, band reject, high pass and low pass are set by selecting appropriate outputs from the three primary op amps of the circuit U712, U88 or U710. Positions 6 thru 11 by pass the filter and connect various amplitude and phase measuring circuits to the plot recorder.

The FILTER OSCILLATE button (S10 on the meter board) sets the filter into an oscillating mode at its natural frequency to determine what this center frequency is. To achieve this, a logic high (+10V) is sent on J2-20 to appropriate logic gates to disconnect the signal input, apply positive feedback with AGC stabilization and remove POST FILTER Gain, if selected.

The MARKER control, RV18 contains switch S5 to select markers. Two types of markers are generated by the 4400A. Swept sine waves require the digital markers described in section 5.6. The tuned receive or spectrum analysis mode mixes a portion of the COMB signal (section 5.12) into the input signal. The selection of which type of marker to use is determined by which position the FUNCTION SWITCH S21 is in. The FUNCTION SWITCH logic generates the appropriate commands to the required circuits to generate markers when required.

Q18 operates analog select switch U73/10 (schematic 5 location D-1) to select a DC voltage representative of the signal amplitude or a DC voltage representative of the phase difference to the plotter A to D converter. In positions 6 thru 9 of S21 this selection is obvious. In positions 10 or 11 Q18 is driven by a 250Hz drive from the plotter (schematic 7 location C-1). This causes the plotter to alternately convert phase and amplitude at a 250Hz rate. This 250Hz signal is injected via CR46 when CR40/CR39 is high. In non dual modes CR49/CR39 is low and the signal at the anode of CR46 is low allowing CR42/CR43 to control Q18.

CR41/CR44/CR38 operate Analog Select switch U59 (schematic 5 locations A-8, D-7, E-5) to route the appropriate signals to the detectors. When in positions 7, 9 or 11 Q23 is saturated to disable U66 (schematic 5 location E-2)

5.4.2 Input Range Switching

S14, S15 and S16 form a mechanically interlocked push button group that chooses the gain of the front end and thus the possible range of the input signal.

In addition to the three possible gains the front end may assume, an additional +30dB gain may be switched into the circuit after the filter. Thus there are actually 4 possible measurement ranges and therefore there are 4 led's to indicate the selected range. The POST FILTER GAIN may only be used when the filter has been selected and logic is included to both select and indicate the correct range under all conditions. For example if +30dB POST FILTER GAIN is called for by pushing S19 but the RECEIVER FUNCTION switch is in positions 6 thru 11 the gain will neither be selected nor indicated.

The logic for the led's is as follows: Say the 0 to -60dBm range is selected (S15 pushed) and POST FILTER GAIN is not selected (i.e. the filter is set to unity gain) then the 0 to -60dBm led will light. If PFG were now called for and available the led's would down range to -30dBm to -90dBm.

The anodes of the four Led's are tied together and via R129 are connected to ground. The cathode side is connected by a contact on S14, S15 or S16 and Q20 or Q21 to -7V. When PFG is requested and available Q20 saturates, Q21 opens and the appropriate Led is lit.

The INPUT RANGE SWITCH (S14, S15 and S16) operates the control pins of U214 (5, 6, 12 and 13) to select the proper feedback resistors of the front end and therefore its gain. It also generates a two bit range code to program the meter to include the front end gain in its computation before displaying a dBm reading.

5.4.3 Power Regulators

U44 is a 3-terminal 5V regulator providing the power to the digital portion of the Digital Plot Recorder. It receives the +9V unregulated from the meter board and provides a clean, regulated +5.0V DC to the logic.

U110 is a dual tracking regulator that generates a clean, regulated ±15V DC from the ±18V unregulated supply from the meter board. Q5 and Q6 increase the current capability of U110 and R21 and R22 provide current limiting to approximately 200 ma.

R16 through R19 form a voltage divider to generate ±7.5V DC from the ±15V DC to drive the darlington pairs Q1,Q2 and Q3,Q4. These transistors provide a regulated ±7V DC from the ±9V unregulated from the meter board. R15 and R20 provide overcurrent protection in the event of a short on the ±7 volt line.

5.5 RMS TO DC CONVERTERS, AGC AMPLIFIERS, PHASE COMPARATOR

5.5.1 RMS to DC Converters

This section contains two RMS to DC converters, some AC gain stages, some DC gain stages and ripple filters. All of this is used to convert the RMS amplitude of an AC voltage presented to the input to a DC voltage with a value between 0 and +10V DC. It may be configured in two possible ways: to measure the absolute amplitude of a single signal or secondly to measure the relative amplitude difference between two signals. See page 6-4 for a simplified schematic of these configurations.

In the case of an absolute amplitude measurement (dBm ABS) the signal comes in on the upper left hand corner (E-9) and is connected to U69 and U610. U69 is a 7dB gain amplifier whose purpose is to raise the +13dBm to -47dBm input signal to +20dBm to -40dBm as required by the RMS converter. The output of U69 is AC coupled to U68, the RMS converter. This monolithic device contains all of the circuitry to compute the RMS value of the AC signal and provide a DC voltage representative of the logarithm of this RMS value. The output signal at pin 6 is a DC voltage from +120mV to -60mV. This 180mV range is representative of the 60dB range of the input signal with a scale factor of -3mV per dB. Although the scale factor, and hence the 180mV range is fixed, the overall offset is a function of the reference current into pin 5. This current is set by RV13, a voltage divider from the precision +10V reference voltage generated on the meter board. It is set so an input AC level of 0dBm will produce a DC output voltage of 0mV. Thus the maximum input level of +20dBm will produce an output of -60mV and the minimum input signal of -40dBm will produce a DC output of +120mV. C95 and C104 provide integration of the signal conversion. The 0.47 uf value provides a fast response while the 22uf value provides a slow response or long integration time.

The millivolt output of U68 is connected via RV8, R162, RT1 and R170 to U67 which, with R163 at 36.5KΩ is configured as a x55 gain amplifier. This scales the 180mV input range to a 10 volt output range on U67 pin 6. In addition, a reference voltage via RV10, R185, R161 is summed to provide an offset and shift the bipolar input to a unipolar output from 0 to +10V DC.

RT1 provides positive temperature coeficient thermal compensation exactly inverse to the temperature drift of U68.

The 0 to +10V DC voltage at U67 pin 6 is coupled to U65 and associated components. This is a 3-pole bessel filter to remove residule ripple from the converted DC voltage. The cutoff frequency of this filter and the integrating capacitor of U68 are chosen to provide the best accuracy/settling time compromise. Accurate RMS conversions of low frequency signals implies a long integration time but convenience of use of the instrument requires a fast response. The four pole filtering of this combination provides a significant improvement over that of the single pole integration of U68 alone.

In the dBm absolute mode, the signal range is 60dB. The bandwidth of interest is 20Hz to 100kHz. At the extremes of these dimensions, that is low levels and high frequencies, the RMS to DC converter can produce substantial errors. This is characteristic of all AC to DC converters. To provide accurate plotting over this range, the amplitude range is divided into two 30dB ranges and each 30dB range is seperately converted. U68 and associated gain and filter stages described above operate on the upper 30dB portion (+20dBm to -10dBm or +10V to +5V). A second conversion chain is used for the lower 30dB portion. This second chain performs in the same manner as the upper chain with a couple of minor variations.

U610 is a 30dB AC gain stage to raise the input level to the lower conversion chain by 30dB. Thus it is able to operate on the lower 30dB levels as though they were 30dB above their actual level. For example, an input signal of -17dBm would appear at U68 pin 1 as -10dBm and at U77 pin 1 as +20dBm. The lowest input signal of -47dBm would appear as -10dBm at U77 pin 1.

U75 is a X55 gain amplifier like U67 but its offset via RV12,R183, R172 is "30dB" different than that of U67. It provides that a +90 mV signal at U77 pin 6 will generate a +10V DC signal at U75 pin 6. Thus an input level of -17dBm will produce AC levels of -10dBm and +20dBm respectively at U68 and U77 pin 1. These in turn will produce DC voltages of +90mV and -60mV respectively at U68 and U77 pin 6 and +5V at U67 and U75 pin 6. In other words, with the following exception, the DC output of each converter will be the same for a given AC input.

The exception is the errors of the upper converter at low levels and the saturation or overload of the lower converter at high levels. (U610 will be clipped at levels in the upper 30dB range) . However, the upper converter will be optimally accurate for the upper 30dB range and the lower converter optimally accurate for the lower 30dB range.

U66 is a level detector which senses what part of the range the signal is in and causes U73/11 to select the correct converter. Its nominal trigger point is just below +5V and hysteresis prevents chatter at the threshold point. As the signal level passes from the upper 30dB range to the lower, U66 changes state switching U73/11 and causing the DC output to the plotter converter to be fed from the most accurate RMS to DC converter. With all of the gain stages correctly adjusted the DC voltage at the outputs of both bessel filters will be identical at the switch over point and should cause no noticeable inflection in the plot. Fig 5.5.1 shows the various levels in the circuits.

The second mode of operation is the dB ratio mode where the difference of the RMS amplitudes of two signals is plotted. For this mode, the two RMS to DC converters operate in a similar manner. AC signals presented to the INPUT A and INPUT B inputs to the preamp appear as inputs to U69 and U78 respectively. Note that the 30dB gain stage, U610 is not used and U59/9 has selected PREAMP B output.

In this case the offset to U67 is via RV11, R184, R173 rather than RV10, R185, R161. At the same time the output of U75 is connected to U67 input via R175. As U75 is an inverting amplifier, U67 will be summing the DC output of U68 with an inverted output of U77. This equivalent to taking the difference between U68 and U77 or INPUT A and INPUT B. In this case U74 is not used and the composite difference of U67 is filtered by U65. Also during this mode U66 is inhibited by the function switch logic.

RV13 and RV14 set the respective reference current into U68 and U77 so an input of 0dB will produce an output of 0mV DC. RV8 and RV9 adjust the respective scale factors of U68 and U77 to produce a 10V DC output range for a 60dB input range. RV10, RV11 and RV12 adjust various offsets to place the 10V output in the 0 to +10V DC range.

5.5.2 AGC Amplifiers

U212, U312, Q8, Q12, Q11 and associated components form an automatic gain control amplifier. Operation is such that an input with a range of 60dB will produce an output with a range of only a few dB. U211, U311, Q7, Q10, Q13 and associated components form a second identical circuit. The two circuits receive the two input signals via the input preamp or generator meter send preamp and provide a leveled signal to the zero crossing detectors of the phase comparator. As each circuit is identical, the A circuit only will be described.

The input signal is coupled to R40, R38, Q8 a voltage divider. The signal at the junction of these three components is connected to the non-inverting input of U312, a 60dB gain amplifier. The drain-source resistance of Q8, in parallel with R38, is a function of the gate voltage. With the variation of gate voltage available, the voltage divider R40, R38, Q8 forms an attenuator with a range in the order of 45dB. U212 and U312 provide a combined gain of 74dB. CR72, CR73, Q12, Q11, CR14 form a full wave rectifier to convert the output of U312 to a DC voltage. This voltage is compared to a fixed reference voltage and an error voltage developed to provide gate drive to the FET. The circuit attemps to maintain the signal amplitude at U312 pin 6 constant by varying the attenuation provided by Q8.

5.5.3 Phase Comparator

The leveled AC signals provided by the two AGC amplifiers are connected to twin, dual zero crossing detectors U61, U62, U81 and U82. As with the AGC amplifiers each pair is identical.

U61 and U62 generate opposite polarity square waves with positive transitions at precise zero crossings of the AC signal. Each circuit has hysteresis to prevent erratic operation near the zero cross transition. This hysteresis is configured to displace the negative transition only, these transitions are not used in the following comparators.

U81 and U82 operate in an identical manner to U61 and U62. Their outputs are differentiated by C74, R130 and C75, R131 into sharp positive going spikes.

These square waves and differentiated spikes clock and reset two D type flip flops U63. This produces a variable duty cycle rectangular wave at their Q outputs whose duty cycle ratio is proportional to the time between zero crossings of the two AC signals. In other words, the duty cycle ratio is proportional to the phase difference of the two input signals. The flip flops are powered from 0 and +10V DC giving a rectangular waveform output with the same amplitude.

U71 and U72 are two 3 pole series connected bessel low pass filters which take the average value of the variable duty cycle wave form. They output a DC voltage between 0 and +10V DC proportional to the duty cycle of 0 to 100% which in turn is proportional to a 0 to 360° phase difference.

The four zero-crossing detectors and two flip flops are arranged to provide inverse rectangular waves using all four zero crossing transitions of the input signals (positive and negative A and B). The resulting waveforms are "summed" by R121 and R122 into the bessel filter. Using all four transitions improves the accuracy by cancelling errors and significantly reduces the resulting ripple and therefore the filter cutoff frequency/ response time of the circuit.

The output of U61, containing zero cross information of INPUT A signal, is also used in the swept sine wave marker generator. R263 couples this signal to the marker circuit of schematic 6.

The final DC voltage at U72 pin 6 is available at U73/10 as is the final DC voltage from the RMS conversion circuit. Function switch logic determines the state of U73/10 and thus the signal to the analog to digital converter in the digital plot recorder.

5.5.4 Under Range Detector

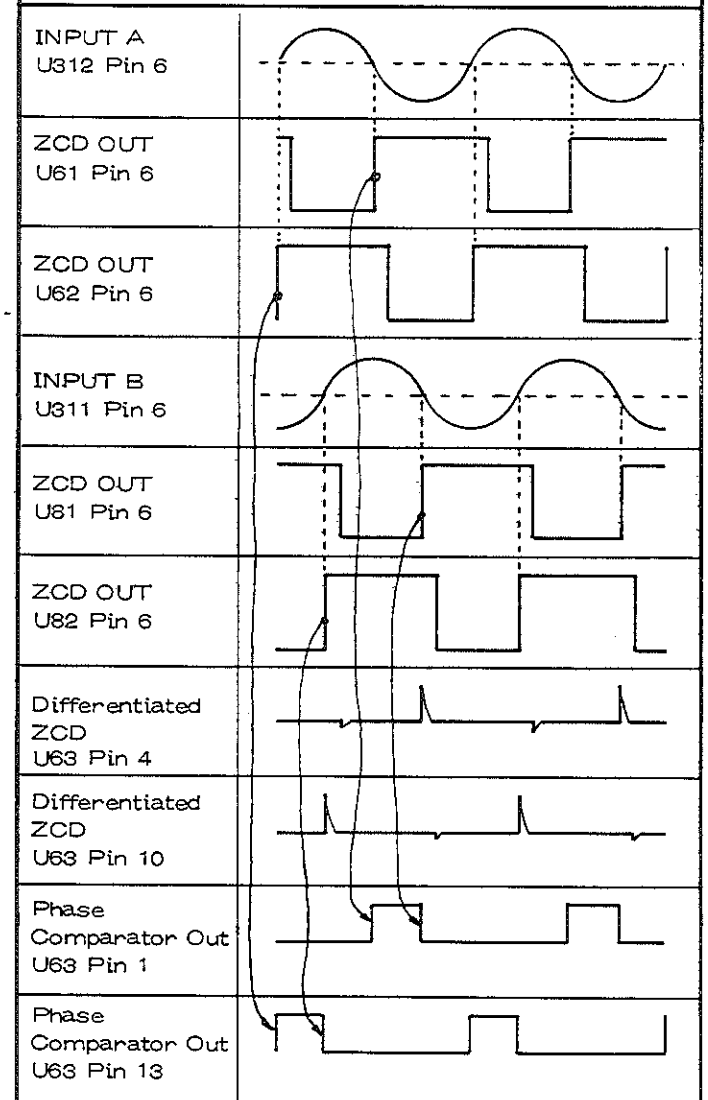
U48 (A-7) is a level detector that senses when the DC voltage at the output of the full wave rectifiers in the AGC amplifiers have exceeded a preset value. This happens when the input signal is a very low value. When the DC control voltage becomes more negative than -7V U48 changes state saturating Q15 and turning on CR55, the UNDER led.

Fig. 5.5.1.1 dBm ABSOLUTE MEASUREMENT LEVELS								
INPUT A	dBm rms	0	−10	−20	−30	−40	−50	−60
Preamp A out	dBm rms	+13	+ 3	− 7	−17	−27	−37	−47
U69 Pin 6	dBm rms	+20	+10	0	−10	−20	−30	−40
U68 Pin 6	mV DC	−60	−30	0	+30	+60	+90	+120
U67 Pin 6	V DC	+10.0	+8.33	+6.67	+5.00	+3.33	+1.67	0.0
U610 Pin 6	dBm rms	>+13	>+13	>+13	+13	+ 3	− 7	−17
U78 Pin 6	dBm rms	>+20	>+20	>+20	+20	+10	0	−10
U77 Pin 6	mV DC	<−60	<−60	<−60	−60	−30	0	+30
U75 Pin 6	V DC	>+5.0	>+5.0	>+5.0	+5.0	+3.33	+1.67	0.0

Fig. 5.5.1.2 dB RATIO MEASUREMENT LEVELS								
INPUT A	dBm rms	−10	−10	−10	−10	−10	−20	−30
Preamp A out	dBm rms	+ 3	+ 3	+ 3	+ 3	+ 3	− 7	−17
INPUT B	dBm rms	−40	−30	−20	−10	0	0	0
Preamp B out	dBm rms	−27	−17	− 7	+3	+13	+13	+13
U69 Pin 6	dBm rms	+10	+10	+10	+10	+10	0	−10
U68 Pin 6	mV DC	−30	−30	−30	−30	−30	0	+30
U78 Pin 6	dBm rms	−20	−10	0	+10	+20	+20	+20
U77 Pin 6	mV DC	+60	+30	0	−30	−60	−60	−60
U67 Pin 6	V DC	+10.0	+8.33	+6.67	+ 5	+3.33	+1.67	0

ZCD AND PHASE COMPARATOR WAVEFORMS

FIG. 5.5.3



5.6 MARKER GENERATOR

5.6.1 Marker Generator

The Marker Generator circuitry has three waveform inputs, ten switch (select) inputs and a single output.

Signal Inputs 1. 1.024 MHz clock (J1-17, at D-9)
2. $\overline{\text{SWEEP}}$ command (J1-25, at B-9)
3. INPUT ZERO CROSSING pulses (at A-9)

Select Lines: (E-4, E-5): ten connections from comb/marker frequency select switches on front panel. Contacts to +7V when buttons are pushed; lines are pulled down to GND by the resistors of network U10. Limiting resistors of network U46, U47, U29 allow the +7V "high" levels to drive the AND gate inputs shown, the latter operating from the +5V supply line.

Output: OCTAVE MARKER OUT goes to Plotter digital circuitry to provide a stored marker "pip" on the display whenever the sweep crosses an octave frequency which has been selected by one of the switches mentioned above.

The TIME-OUT COUNTER consists of the half shown of U17, plus U58. It is a straight binary counter. If its reset line (U17 pin 7, U58 pin 11) were held inactive (low), U17 pin 6 would exhibit a frequency of 1.024 MHz ÷ 16, or 64 kHz; and the pins of U58 would carry frequencies successively divided by two to the right. Two pins of the 4040 carrying 32kHz and 16kHz are not shown; pin 6 would carry 8kHz, pin 5: 4kHz, and so on to pin 1 at 16.125 Hz.

In practice the reset line carries pulses which occur once per cycle of the input waveform, at its positive zero crossing. One-shot U44/6 provides a 2µS output pulse for every positive-going edge of the ZCD square wave. Each pulse causes all outputs of U17 and U58 to go to low levels. Thus, whether a particular output of the TIME-OUT COUNTER can even undergo a single transition depends upon the frequency of the input waveform. For example, as the input frequency sweeps upwards through 500Hz, U58 pin 12 (which would carry 250Hz if the reset were left low) goes from a condition of just achieving a positive transition to one of just failing to do so. fig. 5.6.1 illustrates this point.

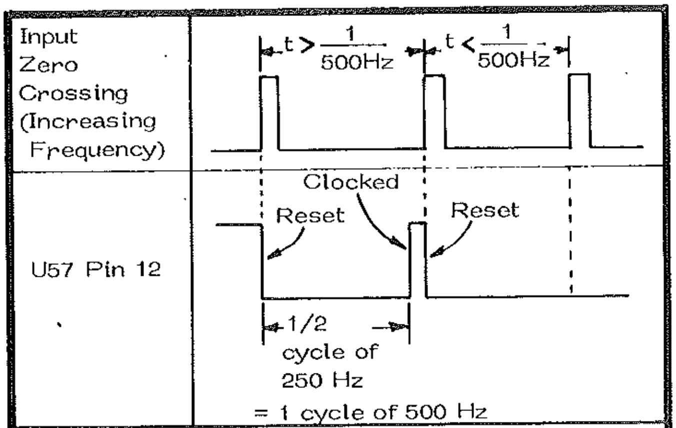


FIG 5.6.1

The OCTAVE COUNTER U57 is a different type of counter, namely a "ring" counter. When the reset line (pin 15) is high, or after it has gone low but before a clock pulse (CP) occurs, pin 3 is high. The first CP on pin 14 causes pin 3 to go low, pin 2 high. The next causes pin 2 to go low again and pin 4 to go high, and so on from right to left with each pin staying high for one clock interval.

Octave marker generation proceeds as follows. When $\overline{\text{SWEEP}}$ goes low (i.e. during sweeping) the INPUT frequency begins to climb from about 20Hz. (Note that the Octave Marker Generator works only for "UP" sweeps). As long as it remains below 31.25 Hz, there will always be a positive transition of U58 pin 1 before each new INPUT ZERO CROSSING pulse. This causes the current in the resistor between U58 pin 1 and U57 pin 3 to drop to zero. Then zero current flows in power supply pin (16) of U57. (all other outputs of U57 are low, so any current from their resistors flows in the ground pin of U57). This turns off transistor Q14; it's collector goes low, so that flip-flop U45/13 is preset (pin 12 goes low). This shuts off gate U54/13 and prevents the succeeding INPUT ZERO CROSSING pulse from clocking U57.

On the first occasion when the succeeding INPUT zero crossing pulse wins the race and appears before U58 pin 1 has gone high, it will get through gate U55/13 and advance the state of U57 (pin 2 goes high). This happens when the input frequency passes through 31.25 Hz. U55 pin 13 drives the non retriggerable one shot U44/10 which provides the output pulse, subject to other inputs to gate U55/1.

a) U55 pin 2: high if the select button corresponding to the frequency in question is pushed (see AND-OR logic, using OCTAVE COUNTER outputs).

b) U55 pin 3 Marker Pulse
One-shot U44/10 provides standardized 2uS pulses for each pulse out of gate U55/13 which is sufficiently long to trigger U44/10. This avoids the possiblity that a short "spike" from the gate could advance the Octave Counter but fail to propagate through to register a marker in the memory of the digital plot recorder.

c) U55 Pin 4: single-cycle constraint. After the sweep passes through 16kHz, the OCTAVE COUNTER will cycle continuously, "searching" for a higher frequency and causing false marker pulses to appear at U55 pin 3. The flip-flop U45 gates these off. U45 pin 1 is clocked "high" by the leading edge of the SWEEP waveform, at the start of the sweep. It is cleared to a low again on the first negative going transition of U57 pin 11, which is inverted, and differentiated by C-66 and the shunt resistor to give a short "pip" on the reset input of flip-flop U45/1.

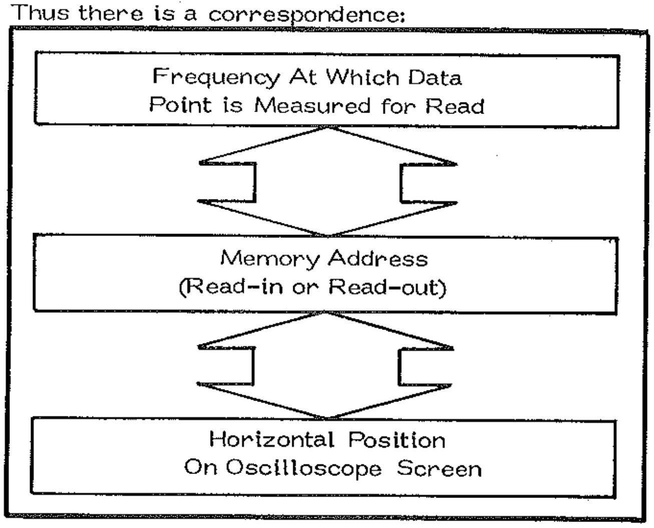
d) U55 Pin 5: the "MARKER ON" switch input. This pin is high (+5V) when the MARKER control on the front panel is ON.

5.7 DIGITAL PLOT RECORDER

Before detailing circuit functions of this section, a little review is in order.

The display on the user's oscilloscope screen consists of a plot of some quantity (dBm level, dB ratio, or phase difference) versus frequency. The selected memory in the 4400A is slowly filled with the incoming data, the "read-in memory address" changing with the frequency at which the quantity in question is being measured. To generate the display, the contents of the memory are rapidly and repetitively read out (non-destructively, i.e. without changing those contents), converted to analog form, and applied to the scope vertical axis as the scope sweeps horizontally in the normal fashion.

Thus there is a correspondence:



There follows a breakdown of the circuitry by "functional blocks", after which a sequential description is given.

5.7.1 Functional Blocks

The digital circuitry of the Digital Plot Recorder can be subdivided, for purposes of understanding its operation, into six functions:

a) Scan Counter (U15, U14; E-7, E-8 of schematic)
This binary counter runs constantly, clocked by the 1.024 MHz input to U15 pin 2. It provides timing services to the other blocks, and the "scan" address count which sequences data out of the memory for the display.

b) Cursor Comparator (U11, U12; E-4, E-5 of schematic)
This compares the scan-count address from U15, U14 with the RIMAC count (Read-In Memory Address Counter) which specifies the address at which new data is currently being stored. From this it is possible to generate the cursor (or "spike") on the display, showing the user the point to which the frequency plot has progressed.

c) Address Switches (U21, U22; D-4, D-5 of schematic)
These are switches which drive the RAM address lines from the Scan Counter or from the RIMAC count as required. The control pins are 14 and 9. Normally the ACO ("Address Change-Over") line to pins 9 is low, $\overline{ACO}$ high, and the signals on pins 7,5,3,1 reappear respectively on pins 10,11,12,13 of each 4019. Thus the Scan Counter drives the memory. When $\overline{ACO}$ goes high, ACO low, pins 6,4,2,15 are switched to 10,11,12,13. Thus the new data word is written into the memory at the address specified by the RIMAC.

d) RAM's (Random Access Memories) U31 through U38
The term RAM's is used to distinguish the bank of eight 2102's from the "memories". (A,B,C and D) referred to on the front panel legends. The latter are not separate hardware blocks but are quarters of the RAM bank, divided as described later.

Each 2102 contains 1024 locations, each corresponding to a combination of the 10 address bits. Single-bit data, (a 1 or a 0) appearing on the input pin (3) is entered at the address specified by the address code when the $\overline{WRITE}$ line (to pins 3) is low. Data in a location, whether newly entered or not, appears at the output pin (12) when the location is addressed.

Two of the ten address lines of the RAM bank are used to specify one of the four "memories", leaving eight bits to be switched by the 4019's as described above. Each memory then has 256 locations.

e) Input Logic and A to D Conversion
The gates, flip-flops and switches to the left of the 2102's perform functions, to be detailed below, associated with the analog-to-digital conversion and entry of new data into memory.

f. Output Circuits
To the right of the 2102's are: an eight-bit register (U42 and U43) to re-time (clean up) and invert the RAM outputs, and inhibit display of data being entered; a digital-to-analog (D/A) converter U52; and an output buffer amplifier/filter, U51. This section also contains Logic and switches to generate the amplitude reference lines.

g. XY Recorder interface U18/1 (B-8) is used to change the mode and speed of data readout for plotting on an external XY recorder. The XY mode is set by momentarily pulling J1-21 high (+5V) which clocks U18 causing Q (pin 1) to go high. This maintains the high manually placed on J1-21 to activate external interface logic.

5.7.2 Sequence of Operations

5.7.2.1 Data Conversion Input

U64 (A-9) is a precision high speed comparator. Its inputs are the linear ramp (schematic 2) and the DC level from the RMS converters or phase detectors (schematic 5). The output (pin 7) is a rectangular waveform with a duty cycle determined by the slope and end points of the linear ramp (a function of the Window Select control group) and the DC conversion level.

A 500Hz square wave is available at U26 pin 15. This waveform is used in linear ramp generator to define the start and stop times of the linear ramp. The output of U64 provides a timed interval the length of which represents the quantity being measured. The data for entry into memory is the state of a counter at the end of this interval.

The Scan Counter is employed for this purpose; thus it has two completely separate and distinct functions: memory scanning for display output, and generation of input data.

The input description begins with the 500Hz driving U73/5 (schematic 2). This is driven by a waveform originating at U14 pin 5 (Scan Counter). This is a square wave at 500Hz, thus its period is 2 milliseconds. When a marker is generated, switch U26/15 is thrown to select a delayed version of the 500Hz wave for a short interval; details of this function are given later and are of no concern here.

The data conversion timing interval begins when the 500Hz is low, and throwing switch U73/5 to allow the timing capacitor C92 to discharge into the current sink as described in section 5.2.3. The timing interval ends when voltage comparator U64 provides a low-going edge into U24 pin 5.

Fig. 5.7.2.1 shows the sequence initiated by that low-going edge. The next positive edge of the clock (256 kHz) connected to U24 pins 3 and 11 causes the Q output, pin 1, to go low. Similarly, the next edge after that caused U24 pin 13 to go low. During the 4 microsecond interval between these edges, gate U16/11 is qualified (both inputs high) and puts out the low-going pulse $\overline{\text{ACO}}$. As described in section 5.7.1, this causes eight of the memory address lines to be switched momentarily from the scan counter to the RIMAC. In the middle of $\overline{\text{ACO}}$, a $\overline{\text{WRITE}}$ pulse is generated, with transitions will separated in time from the instants of address change (a requirement of the 2102's) to enter the data in memory. This is generated by gate U28/1 as detailed in Fig. 5.7.2.1. $\overline{\text{ACO}}$ also drives U16 pin 9 to inhibit the clock to the output registers (see section 5).

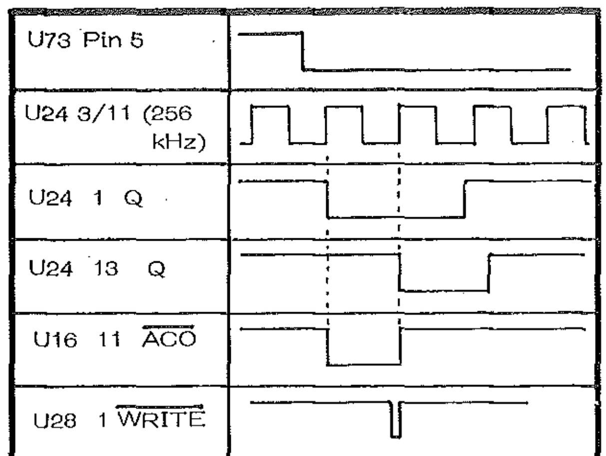


FIG 5.7.2.1

The data entered is the state of eight bits of the Scan Counter. Since the data conversion interval started when the bit to the right of these went from "1" to "0", the eight-bit count word was then 00000000. Thus its state at the end of that interval is equal to the length of the interval, measured in increments equal to the rate at which the 8-bit count changes.

5.7.2.2 Forced Entry for Signals Below Range

DC Signal levels from the analog section which are too high to generate a waveform out of the voltage comparator U64 (i.e. higher than the +10 volt reference level) automatically register a saturation level at the top of the display amplitude range. Flip-flop U24 pin 1 is preset to a high level before conversion starts, the sequence described above for data entry will take place.

However a problem arises if the DC level output is below 0V DC. In this case the output of U65 is high throughout the conversion cycle and if no special provision were made, no data would be entered into memory at all.

This would leave old data (or the random data entered at power turn-on) in the memory in all locations addressed while this condition occurred. The problem is dealt with by the 8-input gate U23/13. This gate decodes states 1111 1110 and 1111 1111 of the count supplied to the RAM inputs, i.e. the last two states in the longest possible conversion interval. If U65 has not already driven U24 pin 5 low by the time this count appears, gate U23/13 does so via the diode CR5, and initiates a data entry sequence.

5.7.2.3 Octave Marker Entry

Octave marker commands are generated elsewhere (see schematic 6). The markers are entered into the memory as reductions in the value of the data word entered into a few locations following receipt of the marker command. This entry function is implemented by the flip-flop U27 and counter 1/2 U17 (C-8 of schematic).

The positive-going transition of the narrow marker command pulse presets U27 causing U27 pin 2 to go low. This removes the reset on the counter Pin 15. The counter then increments until its pin 11 goes high. This causes switch U26/10 to select U27 pin 13 to drive the A to D converter. This is a delayed version of the normal drive waveform, so that conversion counts are reduced by a fixed amount from the value they would otherwise have taken. The amount of reduction is determined by how long U17 pin 11 remains high. When it goes low U25/6 provides a positive going clock input to U27 pin 3. Then U27 pin 2 goes high again since the D input is held low resetting the counter, and remains high until the next octave marker command. (Note that the clock pulse on U27 pin 3 is therefore very narrow and failure to observe it on a scope should not suggest that it is not occuring.) The counter is clocked by the least significant bit of the RIMAC count, so that the delaying condition on the conversion lasts for a fixed (selected) number of input samples.

5.7.2.4 Data Output From RAM's to Display

As the Scan Counter increments, each successive word is entered into the register U42-U43 at the positive-going edge of the clock on pin 6. This clock is inhibited at time of data entry by gate U16/10. This prevents data being entered, which is unrelated to that being displayed, from appearing on the display as a "dancing glitch".

The registers "clean Up" the output data from the RAM's by re-timing it. The propagation delays associated with memory addressing (both outside and inside the 2102's) cause output data to appear at poorly defined times after the nominal time when an address changes, or even to bounce around before settling. The registers are clocked at a time when all of this is over and they present clean, simultaneous inputs to the D/A converter U52.

The D/A converter U52 draws a current into pin 4 which is proportional to the numerical value of the code presented at the digital input word on the left. This current flows in the feedback resistor of U51 and provides a proportional output voltage at J7-4.

Three DISPLAY SHIFT modes are possible by selection of miniature rocker switch sections O, P and Q.

In mode 1 data and reference lines of the B/D trace are shifted when the SHIFT control is pulled and rotated. In this mode switch P and Q are closed. Pulling the control opens S1 and allows 125Hz to control U41/10. Thus for two frames of the output data (125Hz high) during the reference line and data of trace A/C the operation will be normal. When the 125Hz goes low for two frames (data and reference lines B/D) U41/10 changes state and connects the variable DC offset control RV17 into U51. This will cause a vertical offset or shift to this data proportional to the setting of RV17.

Mode 2 is similar to mode 1 except only the data of trace B/D is shifted (reference lines remain stationary). In this mode all three rocker switches O, P, and Q are closed. Operation is similar to mode 1 except 125Hz and 62.5Hz (via switch O) are controlling U41/10. This allows U41/10 to change state during only one of the four frames, that is, when data B/D is being displayed.

Mode 3 is different. It causes trace B/D to magnify x5 and allows it to be shifted. (No reference lines shift.) In this mode only rocker switch O is closed. With switch P open the gain of U51 is increased to 5 times its former value. RV7 allows this to be set to exactly 5 times. During data B/D switch U41/10 disconnects U53 pin 3 - 12, R93, RV7 from the feedback path leaving only R91 and injects a DC offset from RV17. This provides the magnification and shifting. At all other times U41/10 has contacts 15 and 1 connected and the gain of U51 is its normal unity gain.

5.7.2.5 Painting of Amplitude Reference Lines

Amplitude reference lines on the display are painted at the top, the centre and the bottom. When reference lines are selected (switch at E-2 of schematic) the right end of R86 containing a 62.5 Hz square wave is connected to several gates and ground removed from these gates. This waveform is four frames long: high for two frames, low for two. During the low period, nothing differs from the case when no lines are selected. During the high period, four inputs are activated:

a) the registers U42 and U43 are held reset, so that their internal state is 0000.

b) The high-frequency (32kHz) waveform on U15 pin 11 is gated through to drive the normal/invert control pins of the registers, causing their outputs to change from 0000 to 1111 and back at the 32 kHz rate.

c) Switch U41/11 is thrown so that the most significant bit input of the D/A converter, pin 5, is now driven from U15 pin 6. (64kHz)

d) The filtering feedback capacitor C59 (C-2 of schematic) is now returned to ground by switch U41/9, instead of to the summing junction of U51.

The results of (a), (b) and (c) above are shown in Figure 5.7.2.5. As the two-bit count from U15 pins 6 and 11 progresses, the states listed appear on the D/A converter inputs, resulting in the waveform shown.

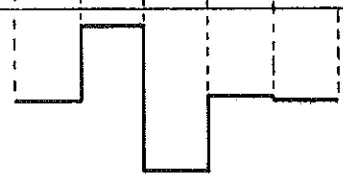
U15 Pin 11	0	0	1	1	0
U15 Pin 6 and D/A MSB (Pin 5)	0	1	0	1	0
All Other D/A Bits	1	1	0	0	1
Numerical Input To D/A (range 0 to 256)	127	255	0	128	127
Output Waveform					

FIG 5.7.2.5

The difference of one LSB (one 256th of display amplitude) between the two middle levels is neglected.

Finally, (d) above results in more rapid switching of the output waveform from one level to the next than would be possible if the smoothing filter were left connected.

5.7.2.6 XY Data Read Out Mode

When the XY mode has been selected (momentarily pulling J1-21 high with an external push button) Q output of U18/1 remains high. When Q is high (XY mode) several functions are changed: $\overline{\text{WRITE}}$ is inhibited to prevent destruction of data in the memory $\overline{\text{ACO}}$ is held high forcing the ram's to be addressed at all times by the RIMAC, the CURSOR is inhibited, and the REF LINES ARE inhibited.

All of this causes the Oscilloscope output display to change to a single level display of the initial value of the selected plot. That is, the output on J7-4 (and Oscilloscope VERTICAL) will be a fixed level DC voltage corresponding to the initial value of the plot stored in memory and selected by the MEM ENTER controls. In the XY mode the MEM ENTER controls become "XY DATA" controls.

If the SWEEP UP button is pushed when in the XY mode the DC voltage at U51 pin 6 will change to represent the data being read out of the memory at the speed selected by the SWEEP SPEED control. Remember that in the XY mode the $\overline{\text{WRITE}}$ line is inhibited so the 4400A goes through all the motions of entering a plot into the memory when in fact it is reading a plot out of the memory. This slow speed is such that the X drive of the XY recorder can move the pen to plot the trace. (The Y drive is a DC voltage derived from an 8 bit D to A converter driven by the RIMAC and located in the external XY interface card).

At the conclusion of the "sweep", the $\overline{\text{SWEEP}}$ line goes high and resets U18/1 back to its normal (non-XY) mode. The oscilloscope display resumes.

5.8 METER ANALOG, AC TO DC CONVERSION, POWER SUPPLY RECTIFIERS and REGULATORS

5.8.1 Functional Description of Meter Board Operation

The meter board measures frequency, absolute signal amplitude (dBm) or a variable determined by some external device. The first two functions are self-contained; the external function requires circuitry in a unit external to the 4400 and is not of concern here.

Frequency measurement is performed in the ususal way, by counting cycles of the unknown frequency over a period of one second, and displaying the resulting number.

To measure dBm level, the incoming signal is filtered as called for by front-panel selection switches; subjected to the appropriate gain, set both manually and automatically; rectified in an AC to DC converter; filtered to remove ripple; and compared to a decaying exponential waveform to derive a time interval proportional to the logarithm of signal level, i.e. to dBm. By counting a constant clock frequency over this time interval, a number is generated for display. However, before accumulating this count, the counter is pre-loaded with a number determined by the total gain between instrument input and the RMS-to-DC conversion. This corrects the reading for this gain, so that the reading represents dBm at the instrument input.

In a case where circuitry applying gain to the signal is located off the Meter Board, a digital code indicating the magnitude of the gain is brought onto the Meter Board and fed to the pre-loading logic.

Provision is made for internal switching of the instrument's Generator output to the Meter Board, for measurement of its level or frequency. In this case, two "gain" bits from the output attenuator level switching circuits are brought onto the Meter Board for the purposes described above.

Update rate for the dBm measurement is 10 samples per second.

5.8.2 Meter Analog

The various signals from other locations in the instrument enter the meter board via J5,J6,J9 and J8. These are in turn routed to the MEASURE select group S7,S8 and S9. Pushing one of these plus the condition of none selected provides the 4 conditions to select INPUT A, INPUT B, FILTER OUT or GENERATOR OUT. The selected signal is presented to the input of U48, a differential input switched gain amplifier. The differential configuration helps to avoid errors caused by ground differences between the meter board and those of the other two boards.

U48 can be switched, with U311/9, to one of two gains: +3dB or -7dB. The normal gain is +3dB but when the input signal exceeds a nominal maximum value an overrange command is generated (schematic 9) to switch U48 to -7dB. This 10dB variation is included in the computation to display the true absolute signal level.

From U48 the signal can optionally pass through two analog filters or weighting networks. The first is a 20kHz 3-pole low pass filter to reject high frequency noise in the measurement. The 20kHz filter is realized with operational amplifier U49 (E-4) and passive components R75,R76,R77, C65,C66,C67. It is the classic 3-pole Butterworth configuration giving an 18dB per octave roll off beyond 20kHz. It is selected by pushing S5. J11 can accept an optional weighting network as described in section 4. The user may use passive component networks to form filters or standard weighting curves. Power is also provided on J11 for networks requiring active devices. U310 normally forms a part of the network and provides a buffered, low impedance output from the network. S6 when pushed in selects the weighting. Note that either or both S5 and S6 can be selected to allow composite filtering.

The signal is next passed to U312, a switched gain amplifier which can assume gains of unity (0dB) or +30dB. This amplifier is the auto range amplifier and its gain, determined by the setting of U311/11, is established by the auto range logic circuitry described in section 5.9.

To preserve high frequency response an LM318 is used. C40,C41 and R32 provide a lead/lag compensation network to ensure stability and preserve the response at 100kHz and +30dB gain. With only R28 4.99kΩ and R33 158kΩ in the circuit the gain is x31.6 or +30dB. With U311/11 set to connect pins 12 and 14, the effective feedback resistor is the series/parallel combination of R33,R36,R35 and RV3. This has a nominal resistance of 5kΩ to match the input resistor R28. RV3 trims the nominal unity gain to be exactly 30dB less than the nominal +30dB gain.

The autoranged AC signal at U312 pin 6 then goes three places: to the zero crossing detector (schematic 9) for frequency counting; to the RMS to DC converter and to the AVERAGE/PEAK AC to DC converter.

5.8.3 AC to DC Converters

U315 is a monolithic device that computes the RMS value of the input AC signal (pin 1) and provides a DC voltage representative of its amplitude at pin 6. C48 and C18 set the internal integrating time constant. In the FAST RMS mode only C48 is selected. In the SLOW RMS mode C18 is added in parallel with C48 to provide a longer integration time as required for low frequency signals or time varying signals such as noise.

U410 and U411 form a full wave precision absolute value detector to calculate the average value of the AC signal. The input signal takes two paths: R74, U410 and associated components form a precision diode providing half wave signal at the junction of R71 and CR18; R46 inputs the AC signal into U411. R47 injects the half wave signal also into U411. The summing junction at pin 2 of U411 adds these two waveforms. Since R47 is half R46 the resulting signal at U411 pin 6 is the sum of the AC signal and twice its inverted half wave rectified component. The result is a full wave rectified signal whose amplitude is the absolute value of the input AC signal.

CR17 and Q8 with the "keep alive" bias provided by R73 improve the high frequency response of the circuit by reducing the switching time requirement of U410. RV6, R44 and R45 inject a positive offset into summing amplifier U411 to overcome the error introduced by R73 and allow adjustment to compensate for the offset errors of the op amps. C69 provides some simple filtering of the full wave signal.

U313 is a peak hold detector. The absolute value signal at U411 pin 6 is buffered by U313 and CR16 which form a precision diode. The output at the cathode of CR16 charges C70 via R40. When the signal drops below the value of the charge on C70,U313/CR16 effectively disconnects itself from R40 which lets C70 discharge into R41 at a slow rate. RV4 provides adjustment of the offset error of U313.

Each of the above three circuits presents a DC voltage representative of the RMS, AVERAGE or PEAK value of the input AC signal. Selection of one of these is effected by S3, S4-B or a board jumper. The jumper chooses either the PEAK or AVERAGE output while the push buttons select RMS or PEAK/AVERAGE. The selected DC voltage is filtered by U29 and associated components which form a low pass Bessel filter. This removes any remaining ripple on the DC signals from the converters and provides a clean DC voltage to the A to D converter (schematic 9) and the small analog meter M1.

5.8.4 Power Supply Rectifiers and Regulators

The lower left corner of the schematic shows the six bi-phase rectifiers and filter capacitors to convert the AC voltages from the secondaries of the power transformer (located on the rear panel) to the six unregulated DC voltages. R1 and R2 provide some isolation of the heavy pulsed current demands of the LED drive in the meter from the +9V used elsewhere in the instrument.

U314 is the ±15V DC dual tracking regulator to provide the supply voltages to the analog circuits of the meter board. Q2 and Q3 provide current boosting to U314 and R20 and R21 are overcurrent sense resistors to limit the current drain in the event of a malfunction.

U13 is a precision +10.00V reference regulator. U14, Q1 and associated components provide current boosting. U14 is a high impedance buffer to receive the +10V from U13 and provide a drive to the emitter follower Q1. U14 seeks to maintain the voltage at the emitter of Q1 at exactly what is on U13 pin 2. This 10.00V is used to power the CMOS circuitry of the meter and provide a precision reference to A to D converters used in the instrument.

5.9 METER DIGITAL

This schematic describes all the meter logic, counting, preseting and display driving circuitry. It receives a DC level or zero crossing pulse from the analog sections described in section 5.8 and processes this data into a displayed numeric readout. It also receives range bits indicative of gain on other boards. The schematic may be divided into five major functions:

a) Analog to Digital conversion. In FREQ this consists of simply counting zero crossing pulses during a 1 second gate time. In AMPL this consists of converting a DC level to a variable duty cycle waveform and then to a numeric count.

b) Auto-ranging detection logic. This measures the DC voltage level and, if necessary, sends commands to the analog section to change the front end gain.

The job of the remainder of the meter logic circuitry is similar in both frequency and amplitude to count the number of waveform cycles occuring during a specified interval, and drive a display showing that number.

c) Counting and Display of Converted Number: All of the logic functions required for these operations are provided by the LSI counter U47. Its internal operation is described in section 5.9.1.

d) Cycling Counters and Control Logic: (lower left quarter of schematic) This hardware defines the control cycles for the two modes (FREQ, dB). It provides command pulses to activate various functions of the LSI counter, and (in dB mode) numbers for pre-loading of the counter.

e) Display Drivers and Display: (to right of U47) Switches driven by the multiplexed segment and digit outputs from U47 drive the light-emitting diode (LED) display.

5.9.1 LSI Counter IC

The MK50395 counter U47 has the following capabilities, as used here:

a. Counting: The MK50395 will count in binary-coded-decimal (BCD) format, upwards or downwards, with a maximum capacity of 999999. The COUNT, COUNT INHIBIT, CLEAR and UP/DOWN inputs (left of U47) perform the functions named, for this count. The ZERO line is high when the count is at 000000.

b. Display Buffering, Multiplexing and Driving: The state of the MK50395's internal BCD counter can be loaded into a display buffer register by pulsing the STORE input. The counter is then free to accumulate more counts, while the contents of the display buffer are multiplexed digit-by-digit into a BCD-to-seven-segment decoder. This provides segment drives to a multiplexed display, at pins 3 through 10 at the upper right of U47. The digits are sequenced from most to least significant, and the appropriate digit line (pins 24 through 29, lower right of U47) is raised for each digit. Simultaneously, the BCD codes are presented digit-by-digit at pins 11 through 14 (lower right) but the 4400A makes no internal use of them.

Leading zero blanking is provided as an option, for the seven-segment outputs. When the LZB line (pin 3, top left) is low, all zero digits to the left of the leftmost non-zero digit are blanked. Thus a count 327 appears that way, not as 000327.

c. Counter Pre-loading: The six-digit BCD counter can be pre-loaded with a number, when the "LOAD COUNTER" line (pin 31) is high, by sequencing the desired 4-bit parallel digit codes onto pins 16 through 19, digit-by-digit in synchronism with the digit count available from pins 24 through 29.

5.9.2 Analog to Digital Conversion.

A DC level from schematic 8 enters at the upper left hand corner (E-9) to R24 and CMOS switch U311/10. This level is sampled and held by U311 and C39. Sampling is at a 10Hz rate from counter U21. The same 10Hz signal alternately switches Q9 on and off which causes C28 to be rapidly charged to a reference voltage (approximately +5V DC) and discharged into RV2 and R15. This creates an exponential ramp on C28 and thus on pin 2 of U210.

U210 is a comparator that changes state when the reference voltage (ramp) on pin 2 equals the DC level on pin 3. As the ramp is exponential the output is a rectangular waveform whose duty cycle is proportional to the log of the DC level. This variable duty cycle is then converted into a count by the succeeding logic.

5.9.3 Auto-ranging Circuit

U312 and U48 (on schematic 8) are the auto-ranging amplifiers switched automatically to give one of three values of gain. The appropriate gain is selected to bring the output signal into a suitable range to drive succeeding circuits.

The resistor switching is controlled by level-sensing comparators U27, U28 (E-7) monitoring the DC level at the output of the filter following the AC-to-DC converter. The changeovers called for by these comparators are timed by the flip-flops U41/15 and U32/15 to occur at the correct point in the measurement cycle.

When the signal out of the AC-DC converter via the filter U29 (schematic 8) is lower than the voltage at the other input of comparator U28, the latter provides a high level into the K inputs of the flip-flops. This causes each flip-flop to assume the zero state (if not already in it) at the next positive edge of the clock signal. These zero states (U41/15 high; U32/14 low) respectively cause switch U311/33 to disconnect feedback resistor R36 (schematic 8). This places U312 in its highest-gain condition, where it remains whether or not the gain switching caused the signal level to rise just above the trip level of comparator U28.

If the rectified signal level now rises further, beyond the voltage to which U27 pin 2 is returned the lower flip-flop will see a high into the J input, pin 10. At the next clock edge U32 pin 15 will go high, pin 14 low, and the switched feedback resistor to U312 will be reconnected to the circuit. This leaves the gain of U312 at unity.

The difference in gain between the two ranges controlled by the lower flip-flop is 30dB. The ratio of d.c. voltages at the high/low comparator trip points is greater than 30dB. Thus there is no possibility of loop oscillation, i.e. of the gain being switched back and forth continuously when the signal is near the boundary of the ranges.

The above actions take place in any of the three gain ranges selected by the INPUT SENSITIVITY switches on the front panel. For large input signals, a special over-ranging provision is made, by means of an auxiliary flip-flop U41/15. This controls a switch to shunt the feedback resistor of amplifier U48 and reduce the gain by 10dB.

If the front-panel switch is set to the highest signal range (-30dBm to +30dBm) and the main auto-ranging control flip-flop U32/15 is in the "1" state, U39 pin 9 (B-3) will be high (as explained later in section 5.9.6.1). If the rectified and filtered signal is still higher than the trip level of the upper comparator, gate U42/11 (E-6) will have both inputs high and will qualify the J input pin 10 of U41/15. The next clock edge on U41 pin 13 will cause U41 pin 15 to go high, throwing switch U311/9 and causing R72 to shunt the feedback path of U48. This reduces the gain of U48 by 10dB (schematic 8).

The high level on U41 pin 15 performs two other functions:

a) it pulls up the trip level of the lower comparator U28, causing it to respond sooner to a decreasing signal level.

b) It holds the main auto-ranging control flip-flops U32/15 preset so that when comparator U28 does respond to a falling signal level and output a "high", only flip-flop U41/15 will be set back to the zero state by the next clock edge.

The clock frequency applied to the auto-ranging flip-flop is equal to the sampling rate for the measurement being made (1Hz for FREQ, 10Hz for dBm). This ensures most rapid possible response of the auto-ranging circuits.

5.9.4 Cycling Counters and Control Logic:

5.9.4.1 Cycling Counters

Timing services for the whole meter board are provided by the counter chain U11-U21-U31 down the left-hand edge of the schematic. These counters free-run. U11 is a 12-bit binary counter. It receives a 1.024 mHz crystal controlled clock from the Generator Board via J1-17. The signal appearing at U11 pin 14 is this frequency divided by 1024, or 1.00kHz. This clocks the dual decade counter U21, producing a 100Hz output at pin 6 and a 10Hz output at pins 13 and 14 (different waveshapes).

The latter clocks one of the two decade counters of U31 (the other is not used), to produce 1.00Hz at U31 pins 5 and 6.

5.9.4.2 Store/Clear Sequencer

In either FREQ or dBm mode, the STORE and CLEAR terminals of U47 (the LSI counter) must be pulsed rapidly in that order at the end of the measurement cycle. This stores the accumulated count in the display buffer register inside U47, and clears the counter for the start of the next measurement cycle.

The two pulses are produced as follows. A positive-going level change, occuring just before they are required, drives the D input U33 pin 5 (B-7). About 4 microseconds later, the flip-flop is set to the "1" state by the 256 kHz clock on pin 3. During that four microseconds both inputs to gate U25/10 are high, and the gate puts out a low-going pulse, which is the STORE command for U47. This pulse also enters a two-bit shift register, and two clock periods later U34 pin 12 provides a high-going pulse to the CLEAR command input of U47.

5.9.5 Frequency Measurement

The cycle of frequency measurement is very simple. All contacts of the FREQ switch (S2) are in the "down" position (not the "up" position shown).

The output of the auto-ranging amplifier U312 (schematic 8) drives U211 (C-8) which is connected as a crossover detector with a small amount of positive feedback. This feedback provides a "snap" action to prevent noise-induced multiple edges at the crossover times, which would cause false counts.

The output of U211 is a square wave at signal frequency. It is gated off while the STORE and CLEAR pulses are generated (sec. 5.9.4.2) by means of gate U22/11, controlled by flip-flop U35/13. The flip-flop "D" input (pin 9) is wired high, so that the rising edge of the 1Hz clock waveform from U31 pin 6 causes the Q output pin 12 to go low. Eight microseconds later the flip-flop is reset by the next rising edge from U11 pin 5; pin 12 goes high again. During that short period the STORE and CLEAR pulses are generated as described previously.

During a given one-second period (minus eight microseconds) between these short sequences, a count of the unknown frequency is accumulated by U47. At the end of that second the count is transferred into the display buffer register in U47, to be multiplexed out to the display as described in Section 5.8.4.6. Meanwhile the counter can accumulate a new count.

5.9.6 Amplitude (dBm) Measurement

The dBm level of the input signal is measured as described briefly in section 5.9.2. The autoranging procedure has already been detailed, including the RMS-to-DC conversion and ripple filtering which need no elaboration. This section will detail the procedure proportional to the dBm level.

Q9 is alternately turned on and off at a 10Hz rate via CR15 and R14. The precision +10.00V DC reference voltage is divided down to approximately +5V DC by R30, R31 and RV11. This voltage appears on the collector of Q9. When saturated, Q9 pulls C28 to the reference voltage and when open, C28 exponentially discharges into RV2, R15 at a rate determined by the setting of RV2. C28 is a highly stable capacitor to reduce calibration drift of the circuit.

This exponentially decaying ramp waveform is presented to pin 2 of U210, configured as a comparator.

The voltage comparator's output goes from positive to negative when the decay waveform passes through the DC level from the Bessel filter. The time from the start of the discharge is found by solving the discharge equation (see also Fig. 5.9.6)

$$V = V_0 e^{-t/RC}$$

$$\text{for } t = -RC \ln \left(\frac{V}{V_o} \right)$$

$$= RC (\ln V - \ln V_o)$$

$$= RC (\ln V_0 - \ln V)$$

where ln = natural logarithm

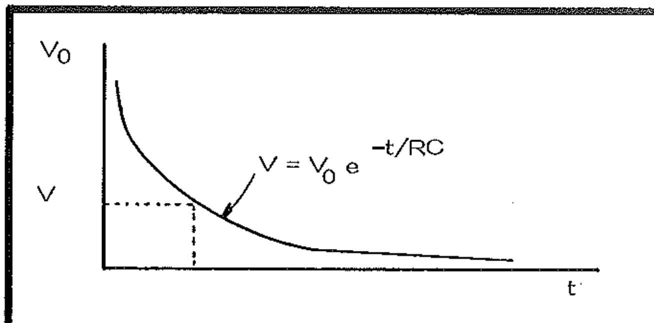


FIG 5.9.6

This shows that the time to crossover varies linearly with the logarithm of the voltage at the positive input of U210; that is, the time can represent the dB level of that voltage, as required.

The procedure is as follows:

a. Pre-load the counter in U47 with a number representative of the gain seen by the signal.

b. Perform the decaying exponential conversion, incrementing or decrementing the counter state from the pre-loaded number.

Expressed another way, the counter is pre-loaded with a number equal to that dBm level which would give an output from the RMS-to-DC converter equal to the DC reference voltage from which the exponential decay starts (resulting in zero counts during the conversion). The counts accumulated during the conversion then represent dB's below that level, hence are algebraically subtracted from the number in the counter. Thus the counter counts downward from the preloaded number for levels above 0 dBm, to display a smaller number; and upwards for levels below 0 dBm, to display a larger number. The sign to be displayed is determined when the conversion is complete.

Sections 5.9.6.1 and 5.9.6.2 following detail the preloading logic and the exponential-decay conversion.

5.9.6.1 Counter Pre-loading

The total gain seen by the measured signal is made up of three components:

a) Auto-ranging gain
b) Manual gain set by front panel controls
c) Post filter gain (in the case of filter measurements only)

From the circuit providing each component of gain comes a one-bit or two-bit code, the numerical value of which is equal to the gain (relative to the minimum value) of that circuit in units of 30dB. These codes are fed to an adder (U38, A-3) on the Meter board, which sums them to give a total gain number. This number is used to pre-load the counter in U47.

The main auto-ranging gain is either 0 or 30dB. An overrange condition occurs for signals greater than about +27 dBm on the input or output, and an attenuation of 10dB is switched on. However this is dealt with separately. A bit specifying the main auto-ranging gain (0 for 0dB, 1 for +30dB) is fed to U38 pin 6.

The auto-ranging circuit is on the Meter board (see section 5.9.3). Its operation is unaffected by settings of any of the Meter "FUNCTION" or "MEASURE" switches.

The two-bit Manual Ranging Gain code comes from one of two sources according to the setting of the "SEND" switch (S7). If the SEND switch is out, the Meter is measuring the signal coming from the instrument INPUT terminals in the Receiver section, via amplifiers controlled by the INPUT RANGE switches. Contacts on these switches provide a two-bit gain code to the Meter board. If the Filter switch is pushed, the signal is also routed on the Receiver board through the state-variable filter, where a post-filter gain of 0 or +30 dB may be selected. A bit from a contact of that select switch is routed, via the FILTER switch on the Meter board, to U38 pin 9.

If the SEND switch is in, the Meter measures the signal from a switched gain preamp being fed by the output of the instrument's Generator section. The gain of this preamp is set by the OUTPUT ATTENUATOR switch, which also provides a two-bit gain code to the Meter board, to correct the amplitude reading for the gain change. Contacts on the SEND switch route this code to U38.

Either way (SEND switch in or out) the two-bit code arriving at pins 5 and 7 of U38 gives the manual ranging gain value as follows:

Pin 5	Pin 7	Relative Gain
0	0	0
0	1	+30dB
1	0	+60dB

The pre-loading logic is at the lower right corner on the schematic, consisting of U38, U37 and associated gates.

U38 is an adder. Inputs 6 and 7 are the LSB inputs, and pin 9 the CARRY input having the same weight as an LSB input. Input 5 has twice the weight of an LSB or carry input. This is the MSB of a two-bit gain code. All higher-order inputs to U38 are wired to logic zero (ground).

The gain sum code can range from 000 to 100, hence requiring three output bits from U38. These are pins 12, 11 and 10, in descending order of significance.

The gain sum code is used in two ways. First, it indicates when the METER is in the highest range, i.e. the signal is above 0 dBm. This corresponds to a gain sum code of 000, which is detected by gate U39/9. The use made of the signal or U39 pin 9 will be detailed in section 5.9.6.2. Secondly, the gain sum code is converted by combinational logic into the appropriate codes to pre-load the counter in U47. Fig. 5.9.6.1 shows the conversion.

Only the most significant digit of the three-digit dBm display is effected, since all preset values are multiples of 10.0 dBm.

The gates to the right of U33 translate the gain code to the BCD codes required. An additional input, from the overranging flip-flop, drives three exclusive - OR gates (U26) to provide a 4 instead of a 3 for the overrange case.

5.9.6.2 dBm Measurement Cycle

The measurement cycle for dBm is 100 milliseconds long. It is defined by the waveforms at pins 13 and 14 of counter U21 (A-9). The cycle is depicted in Fig. 5.9.6.2. It proceeds as follows:

While U22 pin 3 is high (A-8) two actions are taken. Digit 3 of counter U47 is pre-loaded with the number derived as explained above, and the initial direction of counting is set.

Pre-loading consists of strobing the pre-loading number onto pins 16, 17, 18 and 19 of U47 (B-3) at the correct time to load Digit 3. While U22 pin 3 drives the LOAD COUNTER pin (31) of

U47 high, U47 pin 6 the Digit 3 strobe causes U37 to select the bit appearing at the upper of each pair of inputs and apply it to the corresponding output: pin 15 to pin 13, 2 to 12, 4 to 11, 5 to 10. This caused the pre-loading code (see Fig. 5.9.6.2) to be loaded into the third decade of the BCD counter inside U47.

For the count direction function, flip-flop U32/1 (A-6) is set initially to a 1 or 0, placing U47 initially in a "count down" or a "count up" mode. Count down is used only when the measured signal is greater than 0dBm. In this case U39 pin 9 is high, so that gate U22/10 is qualified when U22 pin 3 goes high. This resets flip-flop U32/1, placing a 0 on pin 40 of U47 so that U47 is initially in a count down mode. If the count goes to 000000, U47 pin 39 is raised, qualifying the J input (pin 6) of U32/1. U32 pin 3 receives the inverse of the clock that U47 uses in dBm modes thus when the next positive edge arrives at U47 pin 36, U32 pin 1 has gone high and U47 instead of going from 000000 to 999999, goes to 000001 and thereafter continues counting upwards.

As noted in fig. 5.9.6.1, all other gain codes cause the counter in U47 to count up throughout the measurement. U39 pin 9 is low, flip-flop U32/1 gets preset to the "1" state (Q high) and stays there.

The remainder of the measurement cycle is readily understood by reference to the timing diagram fig 5.9.6.2. The sample/hold switch U311/10 disconnects the D.C. output signal of the Bessel filter U29 from the storage capacitor C33. The exponential-decay waveform, generated by applying the sample/hold command waveform to the network R21-R15-C17, is compared by U210 to the sampled-and-held level on C39. The output of U210 is re-timed by flip-flop U33/13, which receives the inverse of the 128kHz clock connected to U47 pin 36, the COUNT input. When the comparator output goes high, U33 pin 13 and the COUNT INHIBIT pin of U47 follows 13 follows on the next clock edge, disabling further counting by U47. Counting was enabled at the start of the decay period when U22 pin 3 and the LOAD COUNTER pin went low. The counter therefore counts up or down from the pre-loaded number by a number proportional to the decay time to sample level, as required. The resulting final state of the counter is loaded into the internal display buffer register of U47, and the counter cleared, by the STORE and CLEAR strobes which are generated as described in Section 5.9.4.2

The sign to be displayed (+ or −) is determined by observing whether the U47 counter was counting up or down when counting ceased. The D type flip flop U35/1 (A-6) is qualified by the up/down control flip-flop U32/1, and clocked by the COUNT INHIBIT waveform, to produce this effect. Its output drives Q7 which illuminates the vertical bar of the + sign when high. The horizontal bar is always on in dBm mode. Flip-flop U32/1 is held preset during FREQUENCY operation, when no sign is displayed.

5.9.7 Display Drive

As explained in Section 5.9.1, the LSI counter U47 contains a buffer storage register into which the contents of the BCD Counter can be transferred by pulsing the STORE command line. The contents of the storage register are multiplexed out to drive displays. That is, the four-bit code representing the value of each of the decimal digits is output pins (11, 12, 13 and 14 of U47 -B-4 of schematic) whence it is made available to the accessory connector on rear of the instrument. Internally in U47, the code is applied to a BCD-to-seven segment decoder which drives pins 4 through 10 (upper right of U47) in the pattern required to illuminate the appropriate segments of the digit concerned. Meanwhile the digit line (one of pins 24 through 29, lower right of U47) corresponding to the position of the digit in question is driven high, all the others being low.

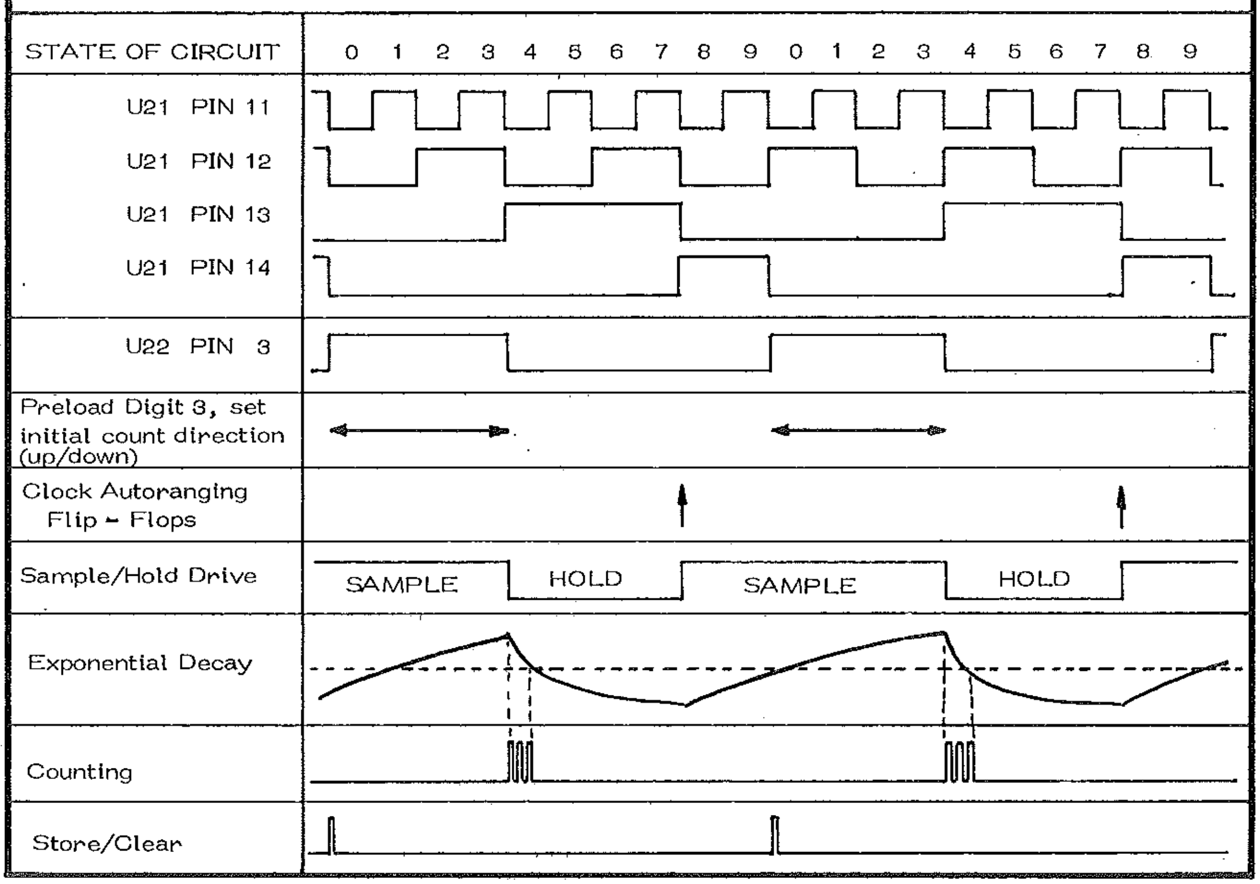
The segment drives from pins 4 through 10 are buffered by emitter followers in the array U43, current limited by resistors in the array U45 and drive corresponding segments of all digits in parallel (the "a" drive is connected to all "a" segments, "b" to all "b"s, etc.). The digit drives are buffered by Darlington connected grounded emitter stages in U36 and U46 to ground the common cathode return of the selected digit (pin 14 or 15 of a digit pair). Corresponding pins of U36 and U46 are all paralleled for greater drive capability except for the ground returns in which sharing resistors ensure fairly even division of load currents between them.

Digits are selected and illuminated in sequence at a rate determined by the digit clock on pin 21. This clock is 512 Hz, with a duty of 3/4 (waveform is 75% high) arranged by the diode gating near U21 (A-9). This duty ensures that a given digit is illuminated for 3/4 of its allocated time, instead of 1/2 as for a square-wave clock.

FIG. 5.9.6.1 METER BOARD COUNTER PRE-LOADING

GAIN CODE (U38 pins 12,11,10)			OVER RANGE FLIP FLOP Q U41 PIN 15	TOP OF RANGE	PRESET DIGIT 3 to: U37 NUM	13	12	11	10	COUNT DIRECTION
0	0	0	1	+40 dB	4	0	1	0	0	Down, change to up at count zero
0	0	0	0	+30 dB	3	0	0	1	1	Down, change to up at count zero
0	0	1	0	0 dB	0	0	0	0	0	Up
0	1	0	0	-30 dB	3	0	0	1	1	Up
0	1	1	0	-60 dB	6	0	1	1	0	Up
1	0	0	0	-90 dB	9	1	0	0	1	Up

FIG 5.9.6.2 METER BOARD dBm MEASUREMENT CYCLE



5.10 FUNCTION GENERATOR

Schematic 10 is the Function Generator. This is an oscillator, tunable over two ranges (20 Hz-20kHz and 100Hz - 100kHz) by either manual or electronic (digital) control, and capable of producing high quality sine, triangle and square wave outputs.

5.10.1 Sine Waves

For generation of sine waves, the Function Generator is configured as a state-variable filter with just sufficient positive feedback applied to cause oscillation. An automatic gain control maintains the net positive feedback at this level.

U71 and U61 are the two integrators of the state variable network, and U62 the difference amplifier. The front-panel control S1 (20Hz - 20kHz/100kHz) selects either an 820 pf feedback capacitor for each integrator or 820 + 3300 = 4120 pf, to produce the appropriate frequency ranges.

The effective input resistor value of each integrator is controlled either by front-panel potentiometers (one dual-ganged pot for coarse, one for fine) or in the SWEEP mode by digitally programmed attenuators controlled by the RIMAC code and the FINE control.

Since an integrator presents a virtual ground to the "low" end of the input resistor, the effective value of that resistance can be controlled either by varying the resistor value itself or by dividing the voltage applied to the high end. Either method varies the current flowing into the integrator input junction. Both methods are employed, in both the manual and swept modes.

Manual control is achieved by ganged potentiometers RV9 - RV10 (fine) and RV11-RV12 (coarse). Switches U73/13 and U73/6 are closed for manual tuning.

For digital control, six bits of the RIMAC code control the dual 4-input multiplexers U32, U33, U34. The two halves of each multiplexer are in the corresponding locations in the input circuits of the two integrators, and are switched in parallel ("ganged") by the two-bit control code applied to pins 9 and 10. The switches select the tapping points of the three voltage dividers in each input circuit. The two MSB's control switch U54 to select one of four series resistors for each integrator. To cover a range of 20Hz to 20kHz or 100Hz to 1000kHz requires the effective resistance to vary by a factor of 1,000 or 60dB, in logarithmically - spaced steps, i.e. constant dB per step. To do this, the two MSB's of the RIMAC code control U54 to change the input resistance in 15dB steps; the next two bits switch U34 to divide the signal voltage in 15/4 = 3.75dB steps; the next two bits control switch U33 to divide in 3.75/4 = 0.9375 dB steps; and the two LSB's switch steps of .9375/4 = 0.234 dB. Each divider output is buffered by a unity-gain LM310 follower to drive the top of the succeeding divider.

In "swept" mode, the manually controlled input circuits are disabled by opening switches U73/1 and U73/9, and the INHIBIT line (pin 6) of U54 is held low to enable that switch.

As the RIMAC code increments, the resistance at the input of each integrator decreases and the frequency of oscillation increases.

Automatic gain control is achieved by rectifying the output signal level of the oscillator, comparing it with a fixed d.c. value, filtering the difference signal and driving a voltage - variable resistor (FET) to adjust the negative feedback to the right level for sustained oscillation, i.e. just balancing the positive feedback.

To reduce rectification ripple, four phase rectification is used. Three phases of the signal are available directly from the state variable circuit. The fourth is generated by the inverting amplifier U91 (just below U71). The four diodes CR17, CR18, CR19 and CR20 select the most positive voltage at any instant, and the common cathode line carries the waveform shown in Fig. 5.10.1

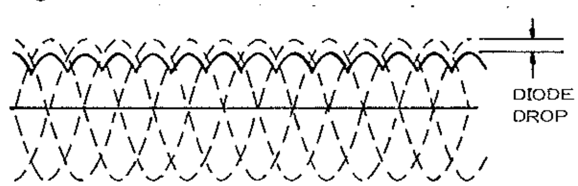


FIG. 5.10.1 FOUR PHASE RECTIFICATION

The comparison and filtering functions are performed respectively by the input and feedback circuits of U82. The waveform of Fig5.10.1 is applied to the summing junction via R132. A direct current of opposite polarity via R133 subtracts from this, and normal op amp action causes the difference current to flow in the feedback circuit. A multiple RC network provides filtering to stabilize the oscillator over its whole frequency range. The filtered output is attenuated and level-shifted by a resistor network to drive the gate of FET Q12.

The resistance of Q12 varies with the voltage applied to its gate, and this controls the amount of negative feedback applied to the state-variable filter by shunting the signal appearing at U63 pin 12. If the amplitude of oscillation goes up, the output of U82 goes down, driving Q12 towards cutoff and so increasing its resistance. This results in less shunting of the negative feedback, therefore more negative feedback, which overcomes the positive feedback to reduce oscillation. The converse is true if oscillation amplitude tends to decrease. Thus the oscillation amplitude stabilizes at a value giving an average current in R132 equal to the current in R133.

5.10.2 Triangle Waves

Triangular waves are generated by the standard integrator/Schmitt trigger arrangement. Integrator U61 (C-3) drives U81 (B-5) via R126 and the compensating or "speed-up" capacitor C64. U81 is connected as a Schmitt trigger by feedback from the output to the positive input via the divider R140-R131 (switch U73/12 is closed) and the resistor U63/8,7. U71 is connected as a unity-gain buffer by means of switch U73/5 which is closed for triangle wave generation. U71 drives integrator U61 via the manual controls which operate as for sine waves.

Fig.10.2 shows waveforms in the circuit, Starting with U81 pin 6 low, the resulting low signal into the integrator U61 produces a positive going ramp at U61 pin 6. The voltage at the mid-point of the feedback divider around U81 is a weighted attenuated sum of the voltages at each end; when this signal rises to ground level U81 wakes up and snaps its output voltage to "plus" saturation level by positive feedback. This generates a negative ramp out of U61 until the same thing occurs in reverse; then the cycle repeats.

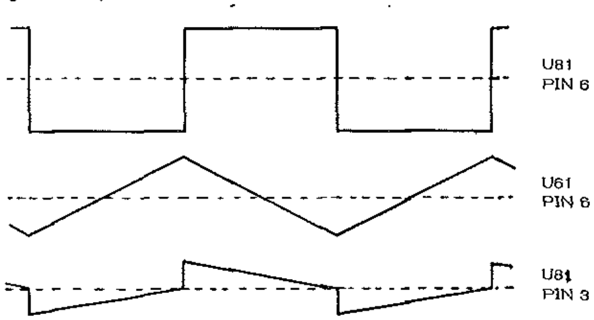


FIG. 5.10.2 TRIANGLE WAVE GENERATOR

The ratio of input to feedback resistance in the Schmitt trigger is calculated to give triangle-wave oscillation at approximately the same frequency as the sinewave, for the same settings of the frequency controls. The output attenuator R140-R131 sets amplitude levels relative to the saturation voltages of U81.

5.10.3 Clipped and Rectangular Waveforms

Sine or triangle waves generated by the circuits described previously are presented to U44, a summing/clipping amplifier via C66, C67 and U72 pin 2/3. This waveform is added to the DC voltage established by RV14, the front panel CLIP LEVEL/DUTY CYCLE control via R93. At the same time, a compensating DC level is applied to the positive input of U44 via R153 and R154. This compensating level maintains the waveform at a constant level and varies the clip level rather than a fixed clip level and varying waveform if not present.

When the current into the summing node of U44 (pin 2) is positive, it is removed by conduction of CR14; when negative by conduction of CR15 via R97. Thus the voltage across R97 reproduces the sine or triangle wave when the net current is below a certain level. This gives the clipped sine or triangle waveform which is buffered by U83 and presented to the output bus via U64/5.

Q9 and Q10 and associated components form a high gain switching amplifier. When U44 pin 6 is positive of its pin 3 (i.e. CR 15 conducting) the current in R145 flows in CR21 and CR22. When U44 pin 6 is negative of its pin 3 (i.e. CR14 conducting) the current in R145 is diverted into Q10. When Q10 conducts, Q9 is switched on, the junction of R144 and R146 is driven high and clamped at +7.5 volts by CR23. When Q10 and Q9 do not conduct the R144, R146 junction is pulled down by R146 and clamped by CR24 at -7.5 volts. R127 and R128 attenuate this ±7.5 volt signal to a level similar to the peak level of the sine and triangle waveforms.

The purpose of Q8 is to disable the variable control RV14 and provide a 0v reference signal to U44. This produces a square wave. Q8 is turned on by a level from the function switch when SQUARE WAVE is selected.

Q7 is used to disable the entire circuit when it is not required. When positions other than 3,4,5 and 6 of the GENERATOR FUNCTION switch are selected, Q7 is turned on and pulls the summing node of U44 negative turning off the circuit. This prevents spikes from being added to the clean waveforms due to circuit crosstalk of the fast edges of the rectangular waveforms.

5.11 FUNCTION SWITCH LOGIC DC POWER REGULATOR, MASTER CRYSTAL CLOCK AND PSEUDO-RANDOM NOISE GENERATOR

Schematic 11 contains a variety of related and unrelated functions.

5.11.1 Function Switch Logic

The static logic in the top left corner of the schematic accepts the switch contact inputs shown (selected contact high, all other low) and translates them into the control outputs labelled to the left. The relationships are self-explanatory.

5.11.2 DC Power Regulators

The ± 15 Volt rails are regulated by U11, with current boosting by Q1 and Q2. R1 and R2 provide current sensing for the current limiting provision of U11.

R4,R5,R6 and R169 are voltage dividers providing ±7.5 volt base drive for the darlington pairs Q3,Q4 and Q5,Q6.

5.11.3 Master Crystal Clock

At the lower left corner of the schematic, transistors Q21 and Q22 form an emitter-coupled oscillator with the crystal X1. Diodes CR48, CR49 provide protection against excessive reverse emitter-base voltage.

This form of oscillator is non-saturating and therefore reliably self-starting.

The 3.072 MHz output from the collector of Q22 is coupled to U79 for division down to 384kHz for the COMB generator and to the divide by 3 counter formed by U710 to generate the 1.024MHz master clock signal. A short exercise with the truth table of a JK flip-flop will show that the divide-by-three counter progresses through the stages 00, 01, 10 and back to 00, where the right-hand flip-flop contains the most significant (left) of the two bits of each word. This in turn is coupled to U79 for division down to 128kHz for the COMB generator and via R123 to the flat cable bus and the rest of the system.

Q19 inhibits U79 to shut down the COMB generator and NOISE generator during the continuous gate and sine wave mode to eliminate crosstalk during this mode.

Q18 is a level shifter to translate the 0 to +10V signal from U79 to a ±7V signal for the random noise generator.

5.11.4 Pseudo-Random Noise Generator

The shift registers U711 and U811 with their feedback path via the exclusive-or gate U77 together form a pseudo-random binary sequence (PRBS) generator. The total shift register length is 26 stages, and the pulse pattern coming out of any terminal does not repeat for $2^{26}-1$ clock intervals (about 67 million). At a clock rate of 128kHz from U79 pin 13 via Q18, this time is 524 seconds, or nearly 9 minutes. For all practical purposes the pattern never repeats, hence the name "pseudo-random binary sequence".

The waveform at pin 9 of U811 is two-level; by passage through a low-pass filter this becomes a smooth "analog" waveform. U16 and the multistage feedback ladder of C11 through C17 and R16 through R22 forms a low pass filter with a close approximation to a linear 3dB per octave roll off curve over the 10Hz to 50kHz range. This converts the "white" noise (constant power per Hz of bandwidth) appearing at the output of the PRBS generator, into "pink" noise, which has constant power per unit of fractional bandwidth. e.g. the same power in any one-third octave band. The output of U16 is the PINK NOISE terminal of the GENERATOR FUNCTION switch.

A precautionary measure is required in case the PRBS shift register should accidentally attain the all-zeros state, from which it would never change since the exclusive - or junction of 0 and 0 is 0, which would go back into the input U711 pin 4 (via two inversions). Such a condition could be present for example immediately after power switch on.

The two flip-flop-flops U812 protect against this eventuality as follows: Both are clocked by the 4kHz output from Q14. The positive edge of this waveform causes U812 pin 1 to go high, unless a high level is simultaneously present on U812 pin 4 (in which case there is no problem). If, as will normally occur, the succeeding sequence of 26 shifts (one full length of the shift register) produces one or more high levels at U811 pin 9, the flip-flop U812/1 is reset. The next positive edge of the 4kHz waveform enters a zero into the second flip-flop, so that U812 pin 12 is high. If, however, the shift register were stuck in the all-zeroes state, the first flip-flop would remain in the "1" state (pin 1 high) between positive edges of the 4kHz wave, and the second flip-flop would enter a one. The resulting low on pin 12 would force a high level at U89 pin 11, to start the PRBS generator going.

5.12 COMB GENERATOR

The COMB GENERATOR receives 128kHz and 384 kHz clock drives from the divide by eight counters in the master clock generator (schematic 11). These are coupled to the binary counters U45 and U46.

The outputs of the upper binary counter U45 form a set of square waves at octave intervals. The first two stages of each (outputs on pins 9 and 7) are not used; the signal on pin 6 is therefore 1.024MHz divided by two five times over, or 16kHz. On pin 5 we have 8kHz; on pin 3, 4kHz, etc. to pin 1, which carries 31.25Hz.

Similarly, a set of signals at octave spacings appear on the outputs of U46. Each of these has three times the frequency of the signal on the corresponding pin of U45, since U46 receives a clock that is three times higher. Further, the outputs of U46 are aligned with those of U45 by applying a reset "pip" to pin 11 of U46 from the positive going edge of the slowest output from U45. This results in the waveform transitions of each U45 output being in line with every third transition of the corresponding waveform from U46, as depicted in Fig. 5.12.

Fig. 5.12 COUNTER WAVEFORMS	
Waveform From U45	
Waveform from corresponding output of U46.	

If a square wave of fundamental frequency 3f and amplitude 1/3A is subtracted from a square wave of fundamental frequency f, amplitude A, the former exactly cancels out the third harmonic component of the latter. There results a waveform of fundamental frequency f, having no harmonics below the 5th. This can be filtered more readily to produce a sinusoidal output than could a simple square wave.

This operation is performed for ten "f-3f" pairs of frequencies from U45 and U46. The schematic only shows the circuitry for the 31.25Hz case. When that frequency is selected, pin J2-9 (E-7 of schematic) is high and gates U13/11 and U14/3 are passing signals. These signals are combined via 3:1 weighting resistances (in favour of the fundamental). Since U13/11 inverts the signal and U14/3 does not, the signal at 3 x 31.25 = 93.75 Hz is subtracted from the 31.25 Hz signal, and the third harmonics cancel as described.

The circuit within the dotted enclosure is a five-pole low-pass Butterworth filter. Its output, adjusted in amplitude by the trimpot RV-13, is summed with the output frequencies from all of the other similar circuits into the op amp U56, the output of which goes to the COMB switch U64/6 controlled by the GENERATOR FUNCTION switch.

The 1kHz square wave from U36/3 is filtered by the three pole butterworth filter composed by U55 and its surrounding passive components. RV17 is a level trim to adjust the sinewave signal at U55 pin 6 to a level the same as that produced by the function generator. This is the cue as described elsewhere.

5.13 GATE LOGIC AND SWEEP LOGIC AND 1KHz SENSE

5.13.1 Gate Logic

The upper portion of the schematic shows the output gating logic. This consists of counter U813 (D-7) and associated control logic to implement the functions named on the front panel controls, and the number set on switch S15 which selects outputs of the counter.

Counter U813 and its associated multiple switch S15 serve two completely separate functions. When both the TIME and the CYCLES switches are out (UP, on schematic) U813 is clocked by the RIMAC CLOCK via Q20 and S15 selects the sweep time, i.e. the rate at which the RIMAC counter, U65, U66) will be clocked. In this case the instrument is being used for plotting of a response or spectral curve. On the other hand when it is desired to gate a burst of the generator output, S15 selects the number of generator waveform cycles in the burst or the time duration of the burst, according to whether TIME or CYCLES is pushed. If TIME is pushed, U813 gets clocked by a 62.5Hz waveform brought in from the comb generator.

If CYCLES is pushed, the zero-crossing signal (schematic 14) provides a clock coincident with the zero-voltage crossings of the signal.

Apart from the source of the clock to U813 circuit operation is identical in either TIME or CYCLES mode.

Gate operation may be either SINGLE in which case a single burst of the selected duration is programmed or REPETITIVE in which case a continuous stream of on/off bursts is programmed. In this mode the ON and OFF times are both equal to the selected burst duration.

In the SINGLE mode, selected by S12 being out (up in the schematic), pressing the START button generates a low-going step at U88 pin 4 (C-8), the switch action being "debounced" by the flip-flop U88/4 -U88/3 so that a single clean transition results. Either this or a clean low-going EXT GATE signal gives a high-going step at U88 pin 11, which is differentiated by the R-C network to form a short "spike" which resets flip-flop U810/1.

The reset flip-flop produces a low on the Q output, pin 1 which causes U89 pin 10 to go high and U75 pin 4 to go low. This enables U813 to begin counting the clock signal presented to its pin 10. This signal is either zero crossing transitions or 62.5Hz as determined by the TIME or CYCLES buttons. U813 increments until the selected output, via S15, goes high, clocking U810/1 which provides a high at Q which becomes a high at U813 pin 11 and resets U813.

For the duration of this count Q of U810 (pin 2) has been high and this high, via the TIME or CYCLES switches S10-B and S9-A provides a high at the D input of flip-flop U810/13. On the next positive going zero crossing transition of the signal waveform after the D input is held high U810/13 clocks changing the states of Q and $\overline{Q}$ and closes the gate switch to let the signal pass. At the end of the selected duration, D goes low and on the next positive going zero crossing transition U810/13 again clocks and Q and $\overline{Q}$ return to their normal state turning off the signal. This retiming provided by U810/13 ensures that gate on and off switch times will always be at zero crossings to always provide a burst of an integral quantity of cycles.

Q17 serves to light the GATE ON led CR88 when Q is high.

When the SINGLE /REPEAT button is in (repetitive mode, down on the schematic) U89 pin 10 is held permanently high, U75 pin 4 permanently low and U813 is free to count continuously. In this case the selected output, via S15, will be a square wave whose period is twice the selected duration with a high and low time equal to the duration. This signal is coupled via S12, S10-B, S9-A to the D input of U810/13 to control the gate directly.

If TIME and CYCLES are both out, the signal on U88 pin 11 (C-8) which is low while START is held in, is substituted for the signal from S12. This allows the START button to be used as a "momentary" or direct manual gate control. The retiming provided by U810/13 is, of course, still in effect.

Finally, if the CONT (continuous) button is pushed, the preset input of U810/13, pin 8, is held permanently high which holds the gate in a permanent ON state.

5.13.2 Sweep Logic

The "sweep logic" in the lower portion of the schematic consists of the 8-bit up/down counter U65-U66 and the logic to the left which sets up its direction of counting, the conditions under which its clock is driven, and the state in which the counter stabilizes at the end of a sweep. The circuit will be described by referring to conditions set up by the function switches S4, S5, S6, S7 and S8.

The DOWN and UP buttons set and reset the "up-down" flip-flop control pin 10 of the up/down counters, setting the direction of counting. It also controls other logic to be described.

The remaining three switches control the conditions under which the clock is applied to the RIMAC counter. The modes are:

MOMENTARY: clock runs as long as UP or down push-button is held in, stops when it is released. Sweep stops when it arrives at top or bottom end (counter state = 1111 1111 or 0000 0000).

SINGLE: each press of button causes sweep to start at one end, progress to the other end and reset to the first end. If direction of sweep is UP, RIMAC state starts and finishes at 0000 0000; if DOWN at 1111 1111.

CONTINUOUS: Sweep goes repetitively in direction set by UP/DOWN controls, resetting automatically and pausing for 1,2, or 4 seconds before starting again.

In MOMENTARY operation, pressing either the DOWN or the UP button causes a high to appear at U86 pin 4 (C-7). This raises the J input of a flip-flop (C-5) and the next positive clock edge on U76 pin 3 causes the Q output to go high. If the counters U65,U66 are not in an end state (0000 0000 if counting down, 1111 1111 if counting up) then the final carry output signal on U66 pin 7 (C-3) is high, and U89 pin 3 is high. Thus gate U74/6 is qualified and the clock on U74 pin 4 is gated through to the counter. With the MOMENTARY button pressed, the EN pins are low and the counters are enabled to count. Also, conditions are set up for the UP or DOWN "SWEEPING" LED (A-4,A-5) to blink at clock rate, according to the state of the Up/Down flip-flop.

Counting stops when either of two events occurs:

a) the DOWN or UP button, whichever was being pressed, is released. Then the J input, U76 pin 6, goes low and the flip-flop synchronously resets (Q low) at the next clock edge.

b) the counter reaches an end state: 0000 0000 if counting down, 1111 1111 if counting up. In this case U66 pin 7 (CARRY OUT) goes low. Since U77 pin 6 (C-5) is held low, U77 pin 4 is high, so the low on U66 pin 7 appears at U74 pin 3 and shuts off the clock.

   If the direction of counting is reversed by pressing the DOWN or UP button, the CARRY OUT signal will disappear and counting can recommence.

In SINGLE mode, pressing of DOWN or UP sets the state of the up/down flip-flop and raises U86 pin 4 as before. This pin is now connected to reset flip-flop U76/15. This drops $\overline{\text{SWEEP}}$ and allows the counter to count. Note that in either SINGLE or CONTINUOUS mode, the PRESET line (pin 7) of the clock control flip-flop U76/1 is permanently high, so that the clock is always present. If counting direction is up, U86 pin 11 (B-7) is high and the exclusive OR gate U77/3 will invert the signal from pin 1 to pin 3. Therefore when the counter MSB changes from 1 to 0 (ie the state of the counter carries from 1111 1111 to 0000 0000) a positive going edge appears on U76 pin 13. This changes the flip-flop state back to "1", raising $\overline{\text{SWEEP}}$ and stopping the count.

The quiescent state of the counter is determined by the state of the Up/Down flip-flop U86/3 - U86/11(B-7). U86 pin 3 drives the "jam" or asynchronous preset input lines of U65 - U66: pins 3,4,12 and 13. When $\overline{\text{SWEEP}}$ is high, pin 1 is high (the PRESET ENABLE lines) and the counter IC's take the state appearing on the jam lines. Thus a down-count starts at 1111 1111, an up-count at 0000 0000, as required.

In CONTINUOUS mode, the RESET input U76 pin 12 (B-6) is driven by the output of the PAUSE COUNTER U67. (Pin 14,15 or 1 as determined by conditional jumpers). The flip-flop $\overline{Q}$ output in turn drives the reset of the counter, pin 11. The flip-flop is clocked on the end carry of the RIMAC counter as for SINGLE mode, releasing the reset of the PAUSE COUNTER which begins to increment at the 500Hz clock rate. 1 second later, pin 14 goes high (or 2 seconds 15 goes high or 4 seconds 1 goes high). The flip-flop immediately resets and in turn clears the counter. (Note that the high-going pulse on U67 pin 14 is very narrow and will not be seen on an oscilloscope). Thus the RIMAC can begin counting again, after spending one, two or four seconds in the appropriate state to begin the next sweep (0000 0000 for up sweeping, 1111 1111 for down sweeping) which allows the circuit under test to stabilize.

5.13.3 1kHz Tone Detector

When GENERATOR FUNCTION switch S2 is set to AUTO START REP, +7V power is supplied to U92, a tone detector. The signal input to U92 comes from an output of the front end preamp and is thus the Receiver input signal. The capacitors and resistors surrounding U92 set its operating frequency to 1kHz. This means that every time the input signal is 1kHz and at a sufficient amplitude the output of U92 pin 8 will go low. This causes current to flow in R159 and and CR89 and light the 1kHz SENSE led.

Level shifter Q11 converts this 0 to +7V signal to a ±7 volt drive to U75 pin 7 and S4 and S5. When 1kHz is sensed this signal is +7V which inhibits the operation of S4 and S5. As soon as the 1kHz tone ceases (and sweeping begins) Q11 collector goes low (−7) and, if the UP or DOWN button were being held, the RIMAC would begin counting to load a plot into the memory. (This assumes SINGLE has been pushed).

If both CONT and SINGLE are pushed this operation is automatic. When the 1kHz stops, U75 pin 7 goes high causing a momentary high on U86 pin 9. During this time U67 is clocking and a 62.5Hz signal is present on pin 8 of U86. On the next high going edge of this clock U86 pin 10 goes low. This has the same effect as momentarily pushing the UP button and starting the RIMAC counter. This action causes U67 to be held reset and U86 pin 8 to remain low.

At the conclusion of the swept signal the 1kHz reappears, the tone detector senses it and Q11 goes high and the circuit waits for the 1kHz to again disappear.

To ensure reliable operation the circuit is inhibited from starting for 16 ms. When the RIMAC has completed its full count the reset pin of U67 (pin 11) goes low and U67 begins to increment. 16ms later pin 6 goes high for 16ms after the RIMAC completes its count, the low in U67 pin 6 inhibits U86 pin 10 from going low and prevents false triggering by the tone detector from starting the RIMAC count prematurely. The differentiating circuit composed of C80 and R157 hold U86 pin 9 high for longer than 16ms to ensure operation.

Thus when the 1kHz again disappears U86 is started.

5.14 ANALOG GATE, ZERO CROSS DETECTOR POWER AMPLIFIER, OUTPUT ATTENUATOR AND METER SEND AMPLIFIER

5.14.1 Signal buffer and Analog Gate

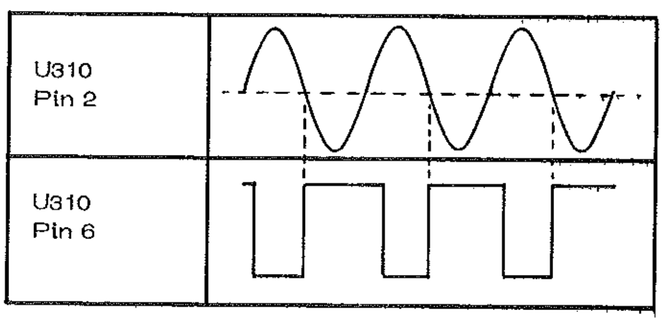
The signal selected by the GENERATOR FUNCTION switch appears on U28 pin 3 (E-8) via a selected 4066 CMOS switch. U28 buffers the signal and it is available at the SOURCE output connector and the INT/EXT switch S14. The signal selected by S14 appears on R39 and is connected by the analog gate, U27/12 and U27/6 to U29 pin 3. The gate is configured as a series/shunt switch with inverted drives from the gate logic to provide a high degree of attenuation in the off mode. The virtually infinite input impedance of U29 prevents the CMOS switch from introducing non linearities.

U29 may have a gain of 0 or +10dB as determined by U18/5. This sets the feedback condition as determined by the requirements of S16, the output attenuator. (see the GENERATOR BOARD OUTPUT POWER AMPLIFIER table for details on this function.)

U815 (E-5) is a differential buffer to permit the power amplifier to be operated in a floating mode. U815 and the entire power amplifier are powered from an isolated power supply to permit this entire block to be referenced to a ground potential differing from that of the 4400A circuit common.

5.14.2 Zero Cross Detector

U310 receives a sample of the SOURCE signal via R48 and C29. R50, R51 and R52 form a Schmitt Trigger with hysteresis to convert the SOURCE waveform into a square wave. The circuit is configured such that as the SOURCE waveform just crosses 0 volts in a negative going direction the output, pin 6, swings positive changing the reference voltage on pin 3. The signal must then go positive of 0 volts in the opposite direction to change the state of pin 6 of U310. This ensures that the positive going transitions of the squarewave output coincide with the negative zero crossing transitions of the signal for proper gate operation. The negative square wave transitions will be displaced in time due to the hystersis action.



Q24 is used to inhibit the action of the zero cross detector when it is not required. When the CONT gate button is pushed, Q24 is saturated to shunt the SOURCE signal and inhibit the operation of U310. This ensures clean signals free from the potential leakage of the sharp spikes present during the transitions of U310.

5.14.3 Output Power Amplifier

U815 is a differential input buffer with a loss of 12dB used to bridge the instrument referenced ground of the SOURCE signal to the output circuit. The divide by four configuration gives the circuit a common mode range of over 50 volts, the maximum swing of the output power amplifier. This allows the output high to be connected directly to instrument ground and the signal taken from the output floating ground. This gives complete freedom of use of the two output terminals for use with balanced, floating loads.

U815 is coupled to RV15 the OUTPUT LEVEL control. This has a range of 0 to about -14dB loss. The signal is then coupled into U814 inverting input via R89 and, if RL7 is closed, R88. RL7 sets the gain of the power amplifier to +16dB or +26dB nominally as determined by the requirements of the OUTPUT ATTENUATOR. (see the GENERATOR BOARD OUTPUT POWER AMPLIFIER table).

The op amp U814 provides most of the loop gain of the output amplifier. It is supplied from the "floating" ±50V rails via zener regulators. U814 output drives the base of Q25. The signal is also shifted in D.C. level by the thermally variable potential across Q30 to drive the base of Q27.

Q25 and Q27 are the "driver" pair. They provide complementary signals to the bases of the output pair Q29-Q31: as current increases in Q25 it decreases in Q27, and vice versa. This causes complementary signal currents in the output pair, to drive the load positive and negative of the common terminal.

Transistors Q26 and Q28 provide short-circuit protection. If the output is short-circuited or loaded with too low a resistance, and if relay RL6 (0-1) is closed, the output amplifier will attempt to maintain signal voltage across it by providing large signal currents. However if the in Q29 (for example) approaches 200mA, voltage appearing across R74 will cause Q26 to conduct and divert base drive current from Q29.

Overall feedback is via the network R82/C32. Audio-frequency feedback is via R82, giving an overall gain of approximately 6 or 22. The capacitor provides phase-lead feedback to suppress ringing or oscillation in the output, and to give the best transient response.

5.14.4 Output Attenuator

R72 and four voltage dividers formed by R54,55, 56,57,66,67,68 and 69 provide 5 levels of attenuation from 0 to -80dB. This, in conjunction with the 0 or 10dB gain of U29 and the +16 or +26dB gain of the power amplifier provides 11 steps of output level in 10dB increments. The output attenuator is designed to present a constant 50Ω source impedance to the load at any setting of the controls.

Relays are used to select the tap point for the output due to the low impedance and high voltage swings and to prevent non linearities that electronic switching would introduce. The 1% resistors produce accurate 10dB steps throughout the range. The relays are driven by diode logic addressed by the OUTPUT ATTENUATOR switch S16. See the GENERATOR BOARD OUTPUT POWER AMPLIFIER table for details.

5.14.5 Meter Send Amplifier

U210 and U17 form a switched gain preamplifier to provide a signal representative of that on the OUTPUT connector to the meter and internal phase reference. Their purpose is to buffer the floating output and provide a ground referenced signal with an amplitude range lower than 60dB although the OUTPUT signal can vary more than 120dB.

U210 is a differential input amplifier with a gain of -17dB or +13dB. U17 has a gain of unity of +30dB. Three sets of overall gains of -17dB, +13dB or +43dB are selected by the OUTPUT ATTENUATOR switch S16 to correspond to the requirements of the OUTPUT signal and the meter send range. Again the table gives details of the operation of the CMOS switch U18 to establish these gains. Trim controls RV1, RV2, RV3 and RV4 align the gains of the pair to exactly, 30dB increments. The various capacitors provide amplifier stability.

Caution. This instrument contains CMOS and other types of semiconductors that are sensitive to electrostatic discharge. These parts can be permanently damaged or their reliability dimmished unless proper handling procedures are followed.

Before removing the cover of this instrument study these procedures carefully and follow them rigorously to avoid damaging your instrument.

1) USE A STATIC FREE WORK STATION.

This includes an antistatic work surface grounded via a 330KΩ resistor to a hard ground. Avoid all plastics, vinyl and styrofoam including styrofoam cups, plastic coffee cups, plastic coffee cup holders, cigarette packages with cellophane wrappers, plastic combs, vinyl books or folders, plastic covers on work sheets, plastic bottles, plastic bags, potato chip bags, plastic purses, plastic solder suckers and plastic ashtrays.

2) ENSURE THAT YOUR BODY IS GROUNDED BEFORE TOUCHING ANY STATIC SENSITIVE DEVICE.

Develop habits to prevent discharging your body into static sensitive devices. When approaching a test bench touch a ground first. When working on equipment wear a metalic wrist strap connected via a 330KΩ resistor to hard ground. If not wearing a grounding strap hold on to a ground while touching any semiconductor (unpowered of course).

3) KEEP PARTS AT GROUND POTENTIAL

Store parts in antistatic containers such as special antistatic integrated circuit storage tubes or special conductive foam. Pick up parts by the the body of the item, not the leads. Do not subject semiconductors to sliding movements over any surface at any time.

4) USE GROUNDED TEST EQUIPMENT

This includes soldering iron tips, voltmeters, oscilloscopes etc. Never probe or test semiconductor circuitry with a volt-ohm meter.

COMPONENT REMOVAL AND REPLACEMENT

Components that are soldered in place must be removed with great care to avoid permanently damaging the printed circuit board. Amber circuit boards are among the highest quality available but, as with all boards with high component density, small somewhat fragile traces are used. Improper component removal could pull these traces off the board necessitating major repair.

To remove a defective or suspect component first remove solder from the mounting pad. Use a good quality vaccum solder removal tool or similar technique to remove solder from around and inside the plated through hole that mounts the component. After this is done, carefully free the leads one by one which will probably be sticking to one side of the hole. Use care to avoid damaging the pad. It is suggested that where possible, the component be crushed to allow each lead to be removed individually. If this is not possible cut each lead close to the component body, remove the body then the leads one by one. Do not use excessive force to pull the leads out of the board. They should either fall out by gravity or be able to be gently removed by applying a slight heat to the lead with a soldering iron. Avoid overheating the pad as this could destroy the adhesive holding the pad and trace to the board substrate. Examine each removed lead to see if the internal hole plating has been removed by accident. If so this pad will have to be soldered on both sides of the board when the new component is inserted to maintain continuity.

Careful practice in component removal will prevent any board damage and leave the component mounting pads and surrounding board area in the same state it was in before component removal.

Section 6

4400A AUDIO TEST SET ADJUSTMENTS AND CALIBRATIONS

6.0 General Notes:

Due to the nature of the 4400A all calibrations, with one exception, can be made using the 4400A itself and an external oscilloscope. This one exception is the absolute amplitude calibration of the digital dBm measuring circuit. This requires either another calibrated 4400A or an equivalent, accurate meter capable of measuring amplitude in dBm.

The use of an oscilloscope is not essential for all calibrations but its use is recommended to observe waveforms during all adjustments.

If a complete calibration is being done it should follow the order outlined in this section as some calibrations are done using other circuits of the 4400A which are presumed previously calibrated.

Generally, all the adjustments are analog and amplitude in nature. Frequency adjustments are not required as these circuits use the 3.072 MHz master clock for their reference. This clock is generated using a crystal whose basic accuracy and long term stability is far better than required for most purposes.

Certain frequency related variables cannot be referenced to this master clock (sweep end points, for example). In these cases stable, ±1% precision components are used and absolute accuracy can be verified using the crystal based circuits. (for example, the sweep end points can be measured with the frequency counter and the plot with markers, both of which derive from the crystal.)

The 4400A measures and plots amplitude with the designation dBm. The proper definition of this term requires the measurement to be made across a 600Ω resistor. Most measurements will be the same absolute amplitude (i.e. voltage) with or without a 600Ω termination, if they are made in typical points within the 4400A, as the source impedance is below 1Ω. Strictly speaking, these measurements, when made without a 600Ω termination and with a conventional high impedance AC voltmeter (or "dBm" meter), should be specified in dBv. However, two conventions are popular as a reference for dBv. One states that 0dBv = 1V RMS while the other states 0dBv = 0.775V RMS (=0dBm across 600Ω). To avoid this confusion and to agree with the panel designations used in the 4400A the term dBm will (incorrectly) be used throughout the calibration procedure.

To summarize:

0dBm = 0.775V RMS as measured with a high impedance voltmeter that presents virtually no load to the measuring point. The same voltmeter would read 0dBm if placed across a 600Ω resistor dissipating 1mW. Most contempory AC voltmeters fulfill this description.

6.0.1 Measuring Amplitude

The 4400A resolves to 0.01dB although has a specified absolute accuracy of typically ±0.2dB. To achieve this or better calibration accuracy implies the use of a meter capable of measuring to better than ±0.1dB or about ±1%. Few instruments are capable of such accuracies and even fewer over any frequency range or below a few hundred millivolts.

When performing the calibration of the 4400A, particularily in the digital dBm display section, bear in mind the actual error of the external measuring meter. This error will often be a composite of an absolute error plus a reading error, plus a low level offset plus an attenuator error plus a frequency response error. It is not uncommon for good quality meters to have a cumulative absolute error of over ±0.5dB at mid frequencies.

6.0.2 Simplified Schematics

It is suggested that the reader observe the various simplified schematics in this section. The general functional schematic at the end together with the calibration summary shows all the calibrations referred to in this section. Additional partial functionals throughout the text serve to clarify signal path and functional layout of specific circuits.

6.1 RECEIVER BOARD CALIBRATIONS

Adjustments and calibrations in the receiver board can be classified into four basic areas:

1) Preamp or front end
2) Filter
3) Digital plot recorder analog section
4) Digital plot recorder digital section.

6.1.1 Preamp or Front End

There are five trim adjustments in this area. The preamp can be set to one of three gains with a nominal 30dB difference between each gain. Four of the trims set these gain differences to precisely 30dB while the fifth adjusts the gain symmetry between A and B inputs or the CMRR (common mode rejection ratio) in the differential configuration. Note that the absolute gain or loss is not critical at this point only the 30dB difference between gains. See Fig 6.1.1

Equipment Required:

AC voltmeter measuring in dBm with an absolute accuracy of ±0.2dB or better.

DC Oscilloscope
Procedure:

1. Set up generator section of 4400A to provide a fixed frequency sine wave around 1kHz. Connect the GENERATOR OUTPUT to INPUT A and monitor this point with the external meter.

2. Set RECEIVER FUNCTION switch to any non-filter position, for example positions 6 through 11.

3. Set the INPUT RANGE pushbutton group to -30 to -90dBm.

4. Send a level of -40dBm to INPUT A. Read the signal level at FILTER OUT (the output of the preamp in this case). It should be +3dBm ±1dB. Note the actual level.

5. Change the INPUT RANGE to 0 to -60dBm and change the signal level at INPUT A to -10dBm (exactly 30dB above the previous level). Observe the level at FILTER OUT. It should be nominally +3dBm. Adjust RV5 for the same reading as in step 4. (i.e. if the reading in step 4 was +2.8dBm adjust RV5 for +2.8dBm)

6. Raise the input level to +20dBm (exactly 30dB above the previous level) and change the INPUT RANGE to +30 to -30dBm. Look for a reading of +3dBm at filter out. Adjust RV2 for a level of exactly the same as the reading in step 5). (Using the previous example the reading would be +2.8dBm).

7. Return the INPUT A level to -10dB. Select -0 to -60 INPUT RANGE. The signal at FILTER OUT should be approximately +3dBm. Move the signal to INPUT B and select DIFFERENTIAL on the toggle switch. The signal at FILTER OUT should be approximately the same as that read when the signal was on INPUT A. Now connect the signal to both INPUT A and INPUT B at the same time (Using a Y cable or T connector.) The level at FILTER OUT should drop by several dB. Adjust RV3 for minimum signal. It should be possible to adjust for a cancellation of more than 50dB (i.e. around -50dBm).

8. Repeat step 7. with a signal level of +20dBm and INPUT RANGE of +30 to -30dB. Now adjust RV1 for maximum cancellation. Again look for 50dB or more cancellation.

9. The final control, RV4, will be adjusted using the meter in section 6.3 paragraph 16. The preamp should now have three gains differing by exactly 30dB.

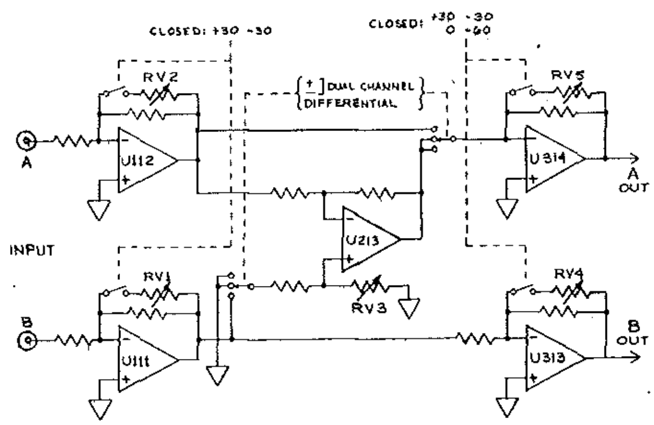


FIG. 6.1.1
SIMPLIFIED PREAMP SCHEMATIC

6.1.2 Filter

A single adjustment is provided in the filter section, a high frequency compensation variable capacitor.

The purpose of the filter frequency compensation is to provide a constant filter center frequency gain at all frequencies. Without compensation, at high Q values and high frequencies, "Q enhancement" occurs. This is caused by the gain bandwidth product limitations of the operational amplifiers. It shows up as a higher pass band gain at frequencies over 10kHz and increases with frequency. The error is compensated with a single variable capacitor in the feedback path.

Equipment Required:

Oscilloscope or AC Voltmeter

Procedure:

1. Connect the oscilloscope or external meter to FILTER OUT.

2. Connect SOURCE out to INPUT A and select the +30 to -30 INPUT RANGE. Select 100Hz to 100kHz on both the GENERATOR and RECEIVER. Select SWEEP MAN START on the generator and SWEEP FREQ on the receiver. Select MOM sweep and a suitable SWEEP SPEED (around 8 secs to start).

3. Turn the FILTER Q control to minimum Q (fully CCW) and the generator and receiver FINE FREQUENCY controls to their mid position.

4. Using the UP and DOWN buttons advance the generator and filter to a mid band frequency (around 1kHz). Tune the FILTER FINE FREQUENCY for a maximum reading on the external oscilloscope or meter. Advance the FILTER Q control to its maximum Q position and carefully retune the FINE control. Note the maximum reading obtained as the control goes through the peak.

5. Repeat step 4) but at a frequency of around 60kHz. Start with low Q then advance to high Q. Adjust CV1, the variable capacitor on the receiver board for the same reading as observed at 1kHz. Note that some settings of the trim capacitor will cause the filter to oscillate. Verify that the filter is not oscillating when the correct reading is obtained by temporarily disconnecting the INPUT A signal. FILTER OUT should have no signal under this condition.

6.1.3 DIGITAL PLOT RECORDER

Analog Section

The analog section of the Digital Plot Recorder consists of several AC gain stages, two RMS to DC converters, several DC gain stages, a phase comparator and a linear ramp generator. This section describes the adjustment of the DC gain and ramp levels to cause accurate plotting.

The reader may wish to refer to the simplified functional of the three basic configurations of the plotter analog section.

Note that two independant RMS to DC converters are used in the plotter. In the dB RATIO mode each converter measures the respective amplitude of the A and B signal inputs. The difference of the logs of these two amplitudes is then plotted.

In the case of dBm ABS both RMS converters act on the same signal. To permit an accurate conversion over the full amplitude and frequency dimension the amplitude range is divided into two 30dB windows with each window being measured by its own converter. As both are operating simultaneously the transition from one converter to the other (auto ranging) is smooth and unnoticeable, provided each converter is properly calibrated. The exception is under certain dynamic conditions where a rapidly varying signal near the crossover point will produce a minor jog in the plot. This is due to the fact that the time constants of the RMS converter is somewhat dependant on the signal level (a condition of virtually all AC to DC converters).
Thus the top converter will be at the end of its range, where it is slow, and the bottom converter will be at the top of its range, where it is fast. The "fast" and "slow" are minor variations and should not be confused with the pronounced FAST and SLOW RMS selection shown on the front panel.

Equipment Required:

AC Voltmeter measuring in dBm with an absolute accuracy of ±0.2dB or better.
DC Oscilloscope.

Procedure:

1. This procedure assumes the preamp has been correctly adjusted as described in section 6.1.1.

2. Select 0 to -60dBm input level range on preamp, select dB RATIO mode with RECEIVER FUNCTION switch and INPUT B on PLOTTER INPUT SELECT toggle.

3. Connect a mid-band signal (approx. 1kHz) to INPUT B at a level of -20dBm. This signal should appear at an amplitude of approximately 0dBm at the inputs (pin 1) of both RMS to DC converters.

4. Connect an oscilloscope probe to the first RMS converter, U68, pin 6. Set the sensitivity to about 5mV per division or less. Adjust RV13 for a minimum DC reading. As the control is turned end to end the voltage may swing up to ±50mV.

5. Using a similar procedure to 4. above adjust RV14 for a minimum DC voltage at PIN 6 of U77.

6. With the same signal amplitude and frequency levels specified in 2. and 3. connect the signal to INPUT A, select - DUAL CHANNEL (mid position of toggle) and PHASE INT REF on the RECEIVER FUNCTION switch.

7. With a probe from the DC oscilloscope look for a level of approximately +5V DC at pin 6 of U72. Adjust RV15 for exactly +5.0V DC.

8. Look on Pin 2 of U64 and observe a linear ramp with a slope between +10V DC and 0V DC. Adjust RV16 so the bottom of the ramp just hits 0V DC. See figure 6.1.3.1

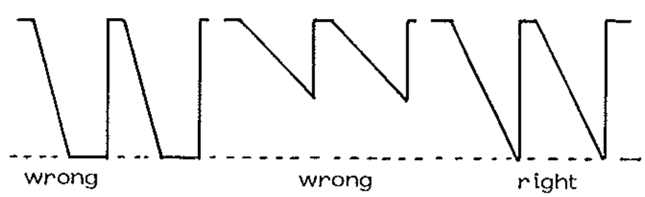


Fig. 6·1·3·1 RV16 Ramp Adjustments

9. Set up the oscilloscope to view the digital plot recorder. Using the set up of 6. sweep the recorder. It should plot near the center reference line. Adjust RV6 so it plots exactly on the center line.

10. Change the RECEIVER FUNCTION switch to dBm ABS. With the same signal as before (-20dBm) adjust RV10 so the plotter will put a line at what should be -20dBm on the oscilloscope screen. (For convenience, set the upper and lower reference lines on two graticule lines separated by 6 major divisions. Each major line will then correspond to a 10dB step.)

11. Change the input level to -10dBm and adjust RV8 for the proper plot.

12. Check -20 and -10 again and verify that they are correct. If not, repeat steps 10. and 11.

13. Change the input level to -50dBm and adjust RV12 for a proper plot.

14. Change the input level to -40dBm and adjust RV9 for a proper plot.

15. Step the input level over the range 0 to -60dBm in 10dB steps and check if all steps fall on a major line on the scope.

16. Finally send a level of about -20dBm to both INPUT A and INPUT B and select dB RATIO mode on the RECEIVER FUNCTION switch. Adjust RV11 so the plot is just on the center reference line (i.e. 0dB difference).

17. Change the input levels at A and B over the range -5dBm to -50dBm. The plot should not deviate more than ±1.5dB.

DIGITAL SECTION

A single trim control requires adjustment in this section. This control, RV7, sets the x5 magnify mode to be exactly 5 times the normal (x1) mode.

Equipment Required:

DC Oscilloscope

Procedure:

1. Set the internal miniature rocker switch to the x5 mode. (Switch 3-0 to be closed see section 4. for detailed instructions.)

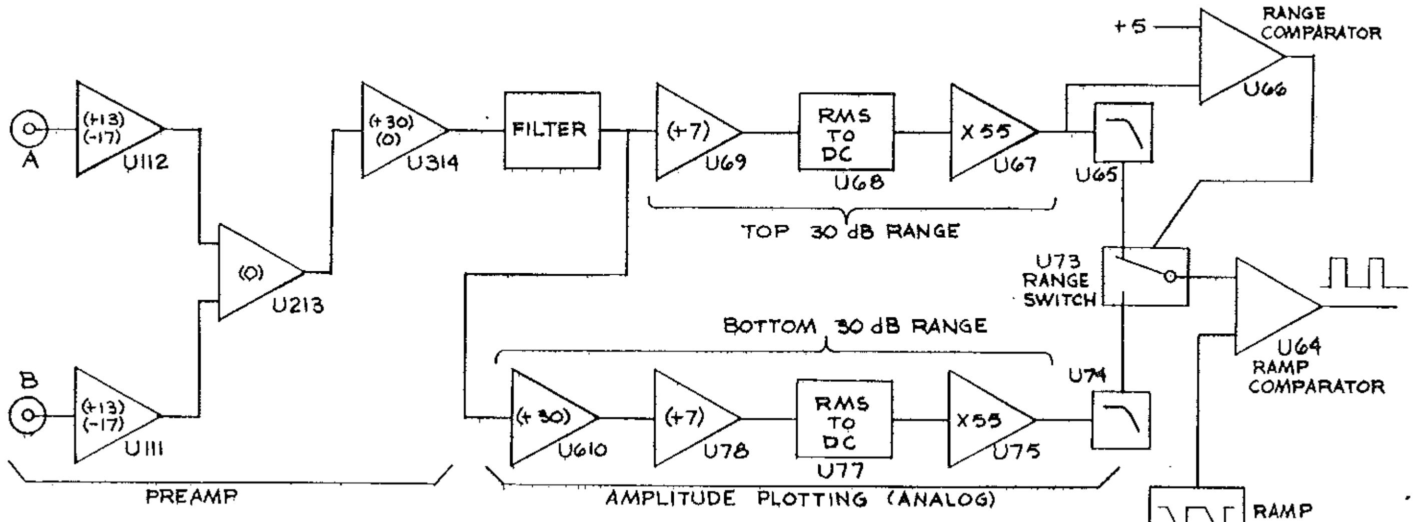
2. Connect the oscilloscope to the 4400A and set up all controls to view the digital memory (plotter) output. Connect OUTPUT to INPUT A.

3. Select a fixed frequency mid band signal on the generator. Select a 50dB window and an INPUT RANGE of 0 to -60dBm. Send a signal of about -10dBm. Select MEM ENTER into trace B or D.

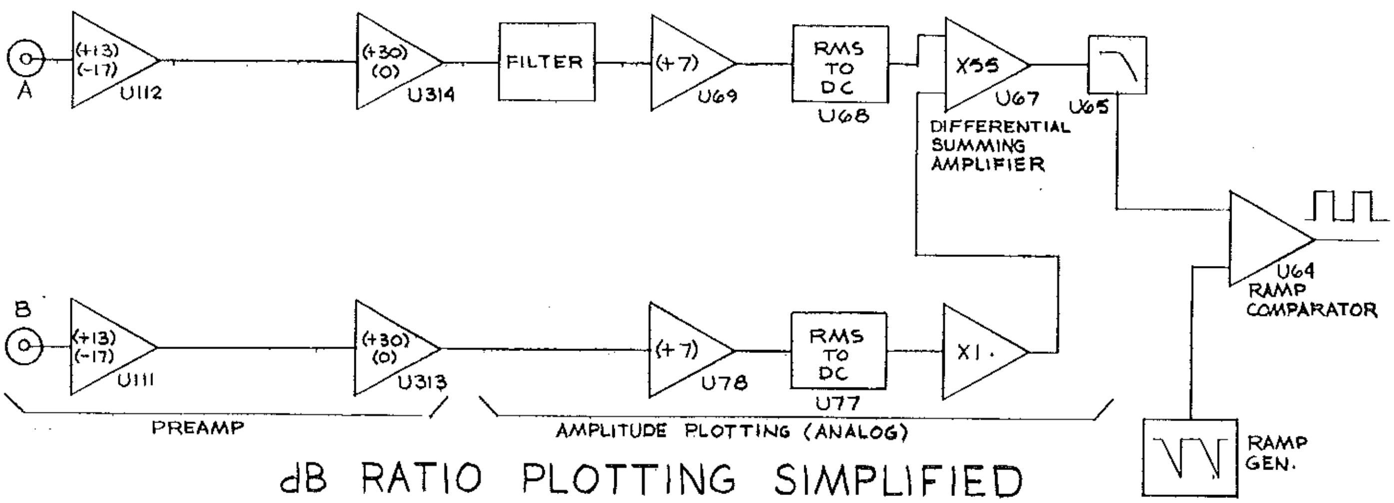
4. Push the UP button and plot a step pattern by lowering the send level by exactly 10dB during the plot.

5. Pull the TRACE SHIFT x5 control. The 10dB step created in step 4 should be expanded to be approximately the total height between the top and bottom reference lines.

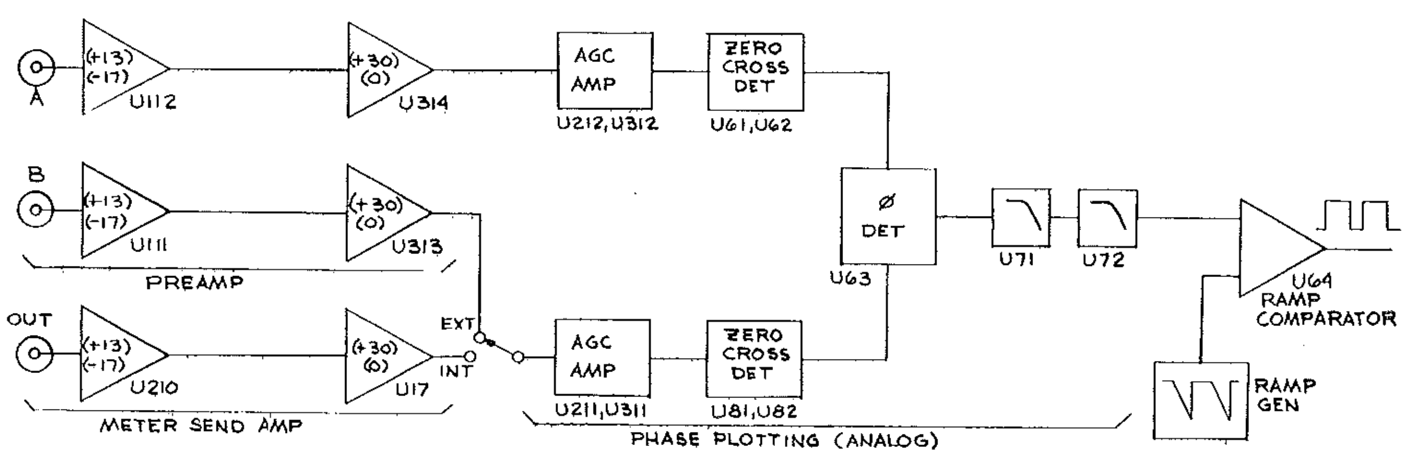
6. Using the TRACE SHIFT control RV7 and adjust the reference lines so they fall exactly on the step pattern.



dB ABSOLUTE PLOTTING SIMPLIFIED



dB RATIO PLOTTING SIMPLIFIED



PHASE PLOTTING SIMPLIFIED

6.2 GENERATOR BOARD CALIBRATIONS

Generator board calibrations divide into four areas:

1. COMB GENERATOR and 1kHz send amplitude
2. 1kHz Tone Decoder Frequency
3. Power amplifier Offset and Bias
4. Meter Send Amplifier Gains

6.2.1 Comb Generator Amplitude Adjustments

The comb generator starts by generating 10 square waves of the required frequencies and 10 square waves equal to but opposite in phase to the third harmonic of these fundamentals. These signals are summed individually and sent to 10 low pass filters. Component variations due to finite tolerances will present amplitude variations at the outputs of the respective filters. This procedure adjusts each of the 10 circuits to give identical output amplitude.

Equipment Required:

AC voltmeter with a frequency response accuracy of ±0.1dB or better 30Hz to 20kHz or an Oscilloscope.

Procedure:

1. Connect the AC voltmeter or Oscilloscope to SOURCES out and select COMB on the GENERATOR FUNCTION switch. Select 1kHz with the COMB/MARKER pushbuttons and adjust RV13-6 to its midpoint. Note the level observed.

2. Turn off the 1kHz and select each frequency in turn one at a time and adjust their respective trims (RV13-1 through RV13-10) for an amplitude equal to that observed in step 1.

6.2.2. 1kHz Auto Start Tone Adjust

The 1kHz sine wave used to generate the cue tone to syncronize sweep and memory enter functions in the AUTO START mode is generated by filtering a 1kHz square wave clock signal. This procedure adjusts its amplitude to be the same as the swept sine wave.

Equipment Required:

AC voltmeter or an Oscilloscope.

Procedure:

1. Connect the AC voltmeter or oscilloscope to SOURCE out. Select AUTO START REC mode on the GENERATOR FUNCTION switch.

2. Select MOM sweep and using the UP and DOWN pushbuttons advance the sweep to a midband frequency (approximately 1kHz). Note the level at SOURCE out.

3. Select SINGLE sweep and let sweep advance to the end so the 1kHz cue tone appears. Adjust RV7 so the level at SOURCE out is the same as that noted in 2.

6.2.3. 1kHz Tone Detector Adjust

The 1kHz tone detector is energized when in the AUTO START REP mode and decodes a 1kHz signal at INPUT A to provide a logic command to start the plot recorder in syncronism with an externally generated sweep.

Equipment Required:

An external 1kHz accurate oscillator or the 4400A generator set to 1kHz.

Procedure:

1. The COMB generator or 1kHz AUTO START generator cannot be used as the GENERATOR FUNCTION switch must be in AUTO START REP.

2. Put the SWEEP controls in the MOM mode and sweep up to 1kHz. Use the FINE control to set the generator to as close to 1000Hz as is possible.

3. Connect the OUTPUT to INPUT A. Send a level of just under 0dBm and set the INPUT RANGE pushbuttons to 0 to -60dBm.

4. Adjust RV8 so the 1kHz SENSE led lights. Lower the output (send) level until the led goes out. Re-adjust RV8 so the led comes on. Repeat until the lowest level is reached where no further optimization of RV8 is possible.

6.2.4 Power Amplifier Offset

This procedure adjusts the output power amplifier for minimum DC offset.

Equipment Required:

DC Oscilloscope.

Procedure:

1. Connect the oscilloscope to the OUTPUT BNC Connector.

2. Select +30 on the OUTPUT ATTENUATOR, push in the DC OFFSET control (concentric to the output level control) and select EXT with the OUTPUT pushbutton. There should be no AC signal on the output except noise.

3. Adjust RV-6 for minimum DC offset. The extremes of the control may permit up to ±150 mV DC and proper adjustment should yield virtually no DC component.

6.2.5 Power Amplifier Bias

The power amplifier output stage requires a quiescent bias to eliminate crossover distortion as the signal goes through zero volts. With no bias there will be a dead band at the zero crossing which will show up as distortion. The distortion will be inversly proportional to signal amplitude i.e. high at low signal levels. The correct bias will completely eliminate this crossover distortion. Too much bias will cause excessive quiescent current drain through the output devices which could cause excessive heat dissipation.

Equipment Required:

Oscilloscope

Procedure:

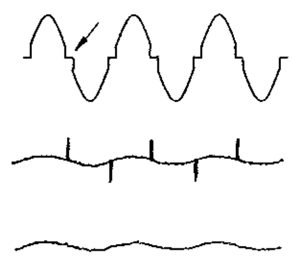
1. Connect the OUTPUT BNC to INPUT A BNC and the oscilloscope to FILTER OUT.

2. Select the first position on the GENERATOR FUNCTION switch, fixed frequency SINE WAVE. Select the first position on the RECEIVER FUNCTION switch, fixed frequency BAND PASS. Select maximum FILTER Q.

3. Tune the GENERATOR to a frequency around 10kHz. Tune the FILTER to the same frequency and using the FINE control tune for a peak.

4. Change the RECEIVER FUNCTION switch to the second position, BAND REJECT. Push POST FILTER GAIN and adjust the oscilloscope for a useable sensitivity. Change the FILTER Q to minimum. If necessary retune the FILTER for a null.

5. Turn the BIAS trim control, RV5, counter-clockwise and observe short sharp spikes on the nulled waveform. Carefully turn this control clockwise until the spikes just disappear. Be careful not to advance the control past the point where the crossover spikes are just eliminated. This would cause excessive bias current producing excessive power dissipation in the output transistors and eventual distruction of the output devices.



6.2.6 Meter Send Amplifier Gains

The meter send amplifier provides a ground referenced signal to the meter board with a level range within the capabilities of the meter while the generator output may vary over a much larger level range. It monitors the actual output connector and is similar in configuration to one half of the input preamp. Its gain is set automatically by the OUTPUT ATTENUATOR switch and this gain is reported to the meter in order that the true absolute output level be displayed on the digital readout. The following calibration procedure assumes the input preamp has been calibrated as in section 6.1.1. The meter need not be accurately calibrated as it is only used for comparisons.

Equipment Required: None

Procedure:

1. Connect the OUTPUT BNC connector to INPUT A BNC. Select the GROUND REFERENCED output mode (mid position of toggle switch). Select a mid band (approximately 1kHz) sine wave. Select -30 to -90 dBm input level range on the receive input.

2. Select -40 on the OUTPUT ATTENUATOR. Select INPUT A on the meter MEASURE pushbuttons. Adjust the OUTPUT LEVEL control for a reading of -40.00dBm on the display.

3. Select SEND on the meter MEASURE pushbuttons and adjust RV2 for the same digital readout as in step 2.

4. Select -10 on the OUTPUT ATTENUATOR and 0 to -60dBm on the INPUT RANGE pushbuttons. Select INPUT A on the meter and adjust the OUTPUT LEVEL for a reading of -10.00dBm.

5. Select SEND on the meter and adjust RV1 for the same dBm reading as obtained in step 4.

6. Select +20 on the OUTPUT ATTENUATOR and +30 to -30 dBm on the INPUT RANGE pushbuttons. Select INPUT A on the meter and adjust the OUTPUT LEVEL control for a reading of +20.00dBm.

7. Select SEND on the meter and adjust RV3 for the same dBm reading as obtained in step 6.

8. Without disturbing the level set up of step 6, disconnect the cable from the OUTPUT connector and INPUT A. Select the FLOAT mode on the toggle switch and using a suitable cable connect the OUTPUT signal, inverted, to INPUT A. That is, the center conductor of the OUTPUT BNC will go to the shell of INPUT A and the shell of the OUTPUT BNC will go to the center conductor of INPUT A.

9. Repeat step 7. but adjust RV4 instead of RV3 for the same level.

10. Reconnect as in step 1. and verify that the three levels specified in step 2., 4., and 6. are the same in both INPUT A and SEND modes under the conditions described.

6.3 METER BOARD CALIBRATIONS

This adjustment procedure calibrates the meter board itself for correct dBm readings. The meter board receives signals from the other two boards of an amplitude between +13dBv and -47dBv (i.e. a range of 60 dB). It also receives logic commands to indicate gains in earlier stages. These analog signals and digital commands are used to generate the digital display. This procedure involves adjustments to affect the gain of the input autoranging circuitry that converts the 60dB input range to a 30dB measurement range and adjustments to the RMS to DC converter, the average and peak detectors and the log analog to digital converter to provide an accurate digital display.

All meter calibrations assume the INPUT PREAMP has been calibrated as described in section 6.1.1. The reader is also advised to note the observations of section 6.0.1.

Equipment Required:

Ac voltmeter with an absolute accuracy in dBm measurements of ±0.2dBm or better.
DC Oscilloscope.

Procedure:

1. Select RMS FAST and INPUT A on the meter. Select 0 to -60dBm INPUT RANGE on the receiver and connect a mid band signal (approximately 1kHz) to INPUT A. The AC voltmeter should also be connected to this point. Install a clip lead from the right end of R64 to the top end of R78. This supplies +10V to R64 and holds the autorange switch in the low gain mode to facilitate the following adjustments.

2. Set the INPUT A level to -31dBm and adjust RV11 for a display readout of -1.00dBm. (The display will flash but the -1.00 will be correct).

3. Change the INPUT A level to -41dBm and adjust RV2 for a display readout of -11.00dBm.

4. Check the -31dBm (-1.00dBm) reading again and if necessary repeat steps 2. and 3. to obtain proper results.

5. Remove the clip lead.

6. Change the INPUT A level to -10dBm and adjust RV3 for a display readout of -10.00 dBm.

7. Change the INPUT A level to -1 dBm and check that the display readout is -1.00dBm. Inability to obtain this reading indicates either RV11, RV2 or RV3 have been improperly set and steps 2. through 6. should be repeated or the AC meter being used has a cumulative absolute error close to that being displayed.

8. Change the INPUT A level to -20dBm and adjust RV10 for a display readout of -20.00dBm.

9. Change the INPUT A level to -30dBm and adjust RV1 for a display readout of -30.00dBm.

10. Select an INPUT RANGE of +30 to -30dBm and change the INPUT A level to +30dBm. Adjust RV5 for a display readout of +30.00dBm.

11. The meter is now calibrated in the RMS mode. Verify by making some spot checks at various levels. Again, bear in mind that the digital readout which resolves to 0.01dB will display errors in the meter circuit, the input preamp and the external AC voltmeter. All elements would have to be accurate to better than 0.05% cumulative error, an unlikely prospect, for the digital display to show all digits perfectly.

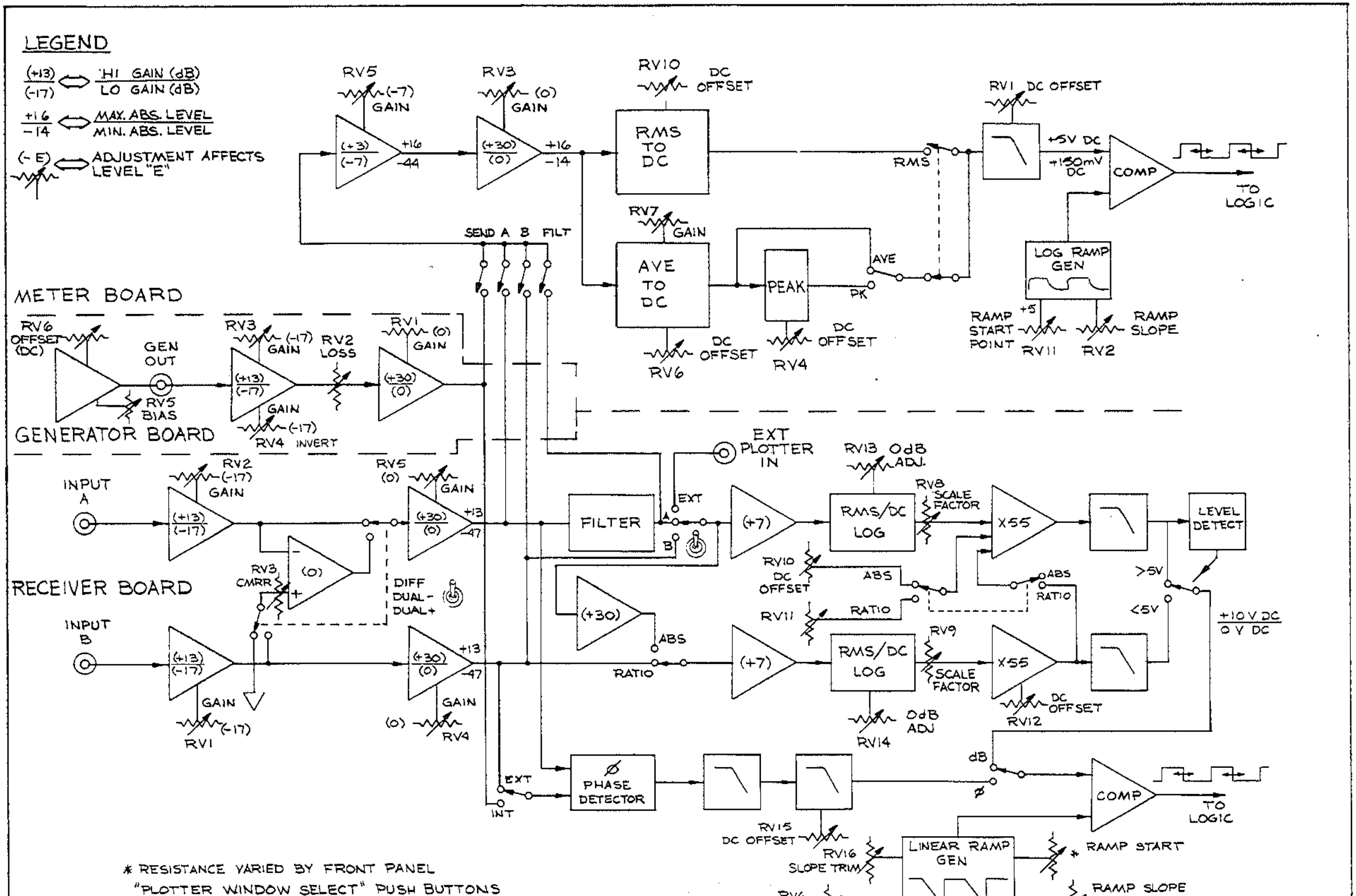
12. Change the input level to -10dBm and select the 0 to -60dBm INPUT RANGE. Adjust the signal level for a display readout of exactly -10.00dBm.

13. Push both RMS FAST and SLOW to select AVERAGE (or PEAK) response. Adjust RV7 for a display readout of -10.00dBm.

14. Change the INPUT A level to -30dBm and adjust RV6 for a display readout of -30.00dBm.

15. If PEAK is used repeat step 14. using RV4 and RV6.

16. Select DUAL CHANNEL on the input preamp. Connect a signal to both INPUT A and INPUT B. Select +30 to -30 INPUT RANGE and adjust the input signal level to some value between +10dBm and +20dBm. Select INPUT A on the meter and note the amplitude being shown on the readout. Now select INPUT B (release all buttons) and adjust RV4 on the input preamp (on the receiver board) for the same reading as INPUT A. This RV4 should not be confused with the RV4 in the meter board.

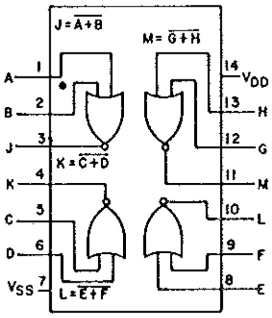


AMBER MODEL 4400A TEST SET
SIMPLIFIED CALIBRATION SCHEMATIC

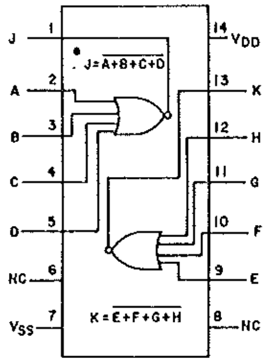
CALIBRATION SUMMARY

Location	Desig.	Function	Trim Procedure
Generator	RV1	U17 0dB Gain ADJ	Adjust for Nominal 0dB Gain to be exactly 30dB less than nominal +30dB gain.
"	RV2	Meter send gain adjust	Adjust for correct GENERATOR meter send level, i.e. correct dBm display reading.
"	RV3	U210 normal -17dB gain adjust.	With OUTPUT ground at instrument ground, adjust for nominal -17dB gain to be exactly 30dB less than nominal +13dB gain.
"	RV4	U210 reverse -17dB gain adjust.	With OUTPUT 'hot' at instrument ground, adjust as RV3 above.
"	RV5	Power Amp. bias adj.	Adjust to just eliminate crossover distortion.
"	RV6	Power Amp. offset adj.	Adjust for minimum OUTPUT DC offset.
"	RV7	1 kHz amplitude adj.	Adjust for same amplitude 1 kHz tone at AUTO START RECORD as SWEPT SINE WAVE.
"	RV8	1 kHz tone detector adj.	Adjust for correct center frequency of U92 1 kHz PLL tone detector.
"	RV13-1 thru RV13-10	COMB generator individual frequency amplitude adjust.	Adjust so each of ten COMB frequencies is same relative amplitude.
Receiver	RV1	U111 -17dB gain adjust	Adjust for nominal -17dB gain to be exactly 30dB less than nominal +13dB gain.
"	RV2	U112 -17dB gain adjust	Adjust same as RV1 above but on U112.
"	RV3	U213 CMRR adj.	With DIFFERENTIAL selected and equal 1 kHz signals at A and B inputs, adjust for minimum output from U213.
"	RV4	U313 0dB gain adjust	Adjust for nominal 0dB gain to be exactly 30dB less than nominal +30dB gain.
"	RV5	U314 0dB gain adjust	Adjust same as RV4 above but on U314.
"	RV6	LIN Ramp generator offset	Adjust for 0^o phase diff. to plot on center reference line.
"	RV7	x5 DISPLAY mode	Adjust so x5 DISPLAY mode is exactly 5 times normal (x1) mode.
"	RV8	U68, U67 gain adjust dB scale factor adjust	Adjust in absolute dBm mode so top 30dB of 60dB window shows correct plot change for corresponding amplitude change at input.
"	RV9	U77, U75 gain adj., dB scale factor adjust	Adjust as RV8 above but for lower 30dB of 60dB window.
"	RV10	Plot offset, top 30dB	Adjust as RV8 above but for correct absolute plot value for corresponding input value (in top 30dB) .
"	RV11	Plot offset, ratio	Adjust after RV12, in ratio dB mode for center reference line plot with 0dB difference at inputs.

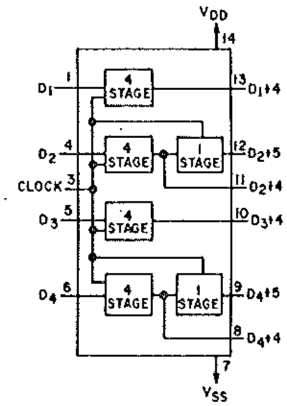
Location	Desig.	Function	Trim Procedure
Receiver	RV12	Plot offset, lower 30dB	Adjust as RV10 above but for lower 30dB.
"	RV13	U68 scale adjust	Adjust so 0dBm at U68 Pin 1 results in 0VDC ±5MV AT U68 PIN 6.
"	RV14	U77 scale adjust	Same as RV13 above but on U77.
"	RV15	U72 offset	With 0^{o} phase shift between two inputs adjust for +5.0V DC at U72 pin 6.
"	RV16	Linear ramp scope adjust	Adjust so bottom of ramp just touches 0V.
Meter	RV1	U210 offset	Adjust for correct absolute dBm readings at very low levels in RMS mode.
"	RV2	Log Ramp slope	Adjust so a given input change in amplitude shows correct digital display change in dB.
"	RV3	U312 0dB gain adjust	Adjust for nominal 0dB gain to be exactly 30dB less than nominal +30dB gain.
"	RV4	U313 offset	Adjust for correct absolute dBm readings of low level signals in PEAK mode.
"	RV5	U48 -7dB gain adjust	Adjust for nominal -7dB gain to be exactly 10dB less than nominal +3dB gain.
"	RV6	U411 offset	Adjust for correct absolute dBm readings of low level signals in AVERAGE mode.
"	RV7	U411 gain	Adjust for desired dBm calibration in AVERAGE or PEAK mode.
"	RV8	U315 offset	Not used.
"	RV9	U315 offset	Not used.
"	RV10	U315 offset	Adjust for correct absolute dBm readings of low level signals in RMS mode.
"	RV11	Log Ramp start point	Adjust for correct overall dBm RMS calibration .



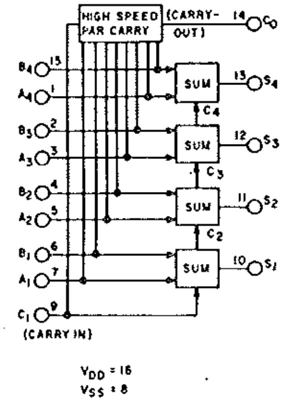
CD4001
Quad 2-Input NOR



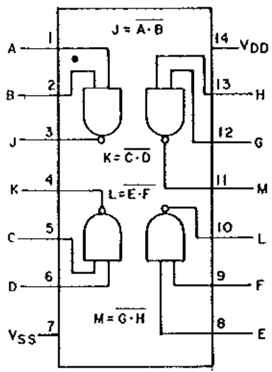
CD4002
Dual 4-Input NOR



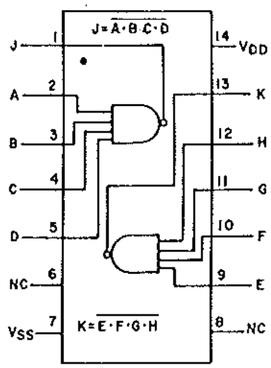
CD4006
18-Stage



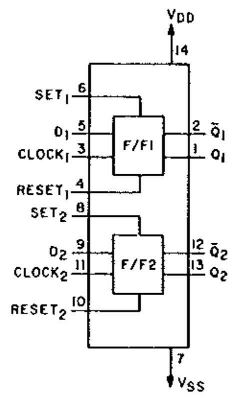
CD4008
Four-Bit Full Adder with
Parallel Carry Out



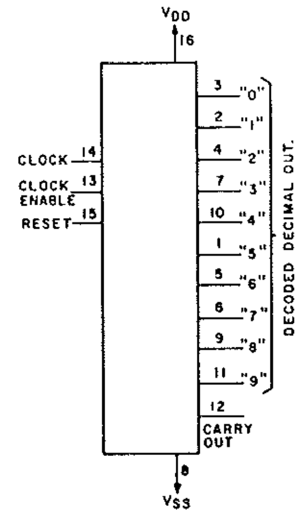
CD4011
Quad 2-Input NAND



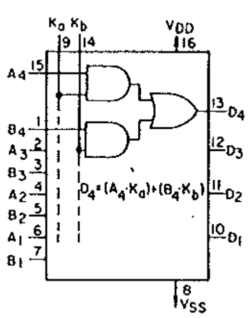
CD4012
Dual 4-Input NAND



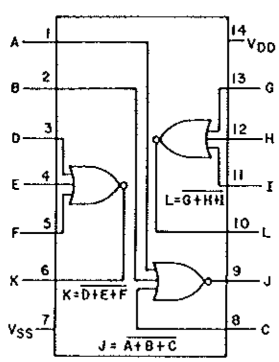
CD4013
Dual "D" with
Set/Reset Capability



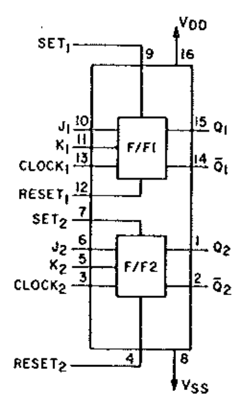
CD4017
Decade Counter/Divider
Plus 10 Decoded Decimal Outputs



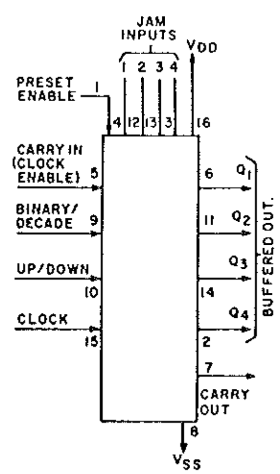
CD4019
Quad AND/OR Select



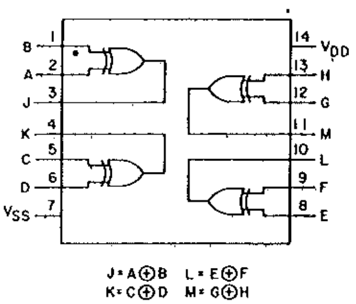
CD4025
Triple 3-Input NOR



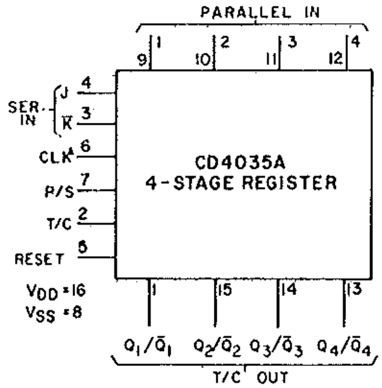
CD4027
Dual "J-K" with
Set Reset Capability



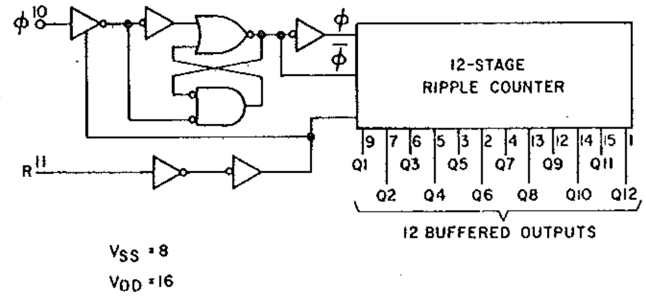
CD4029
Presettable Up/Down Counter
Binary or BCD-Decade



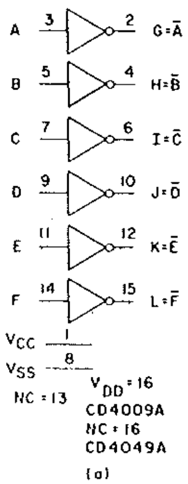
CD4030
Quad Exclusive-OR



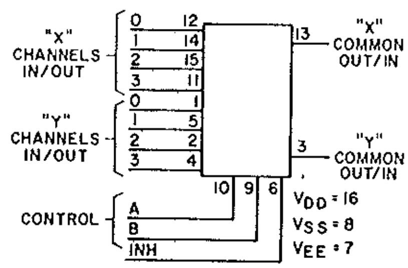
CD4035
4-Stage Parallel-In/Parallel-Out with J-K Input and True/Complement Output



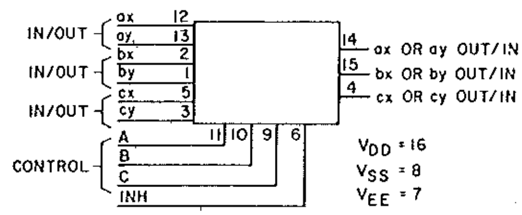
CD4040
12-Stage



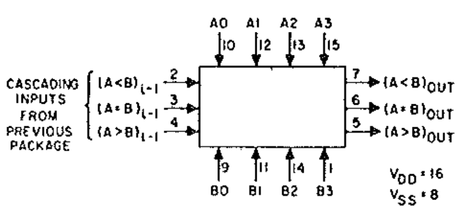
CD4009, CD4049
Hex Buffer/Converter Inverting Type



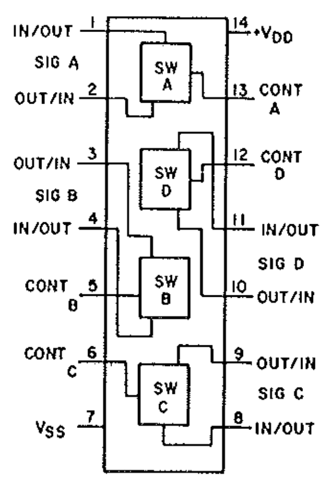
CD4052
Differential 4-Channel



CD4053
Triple 2-Channel

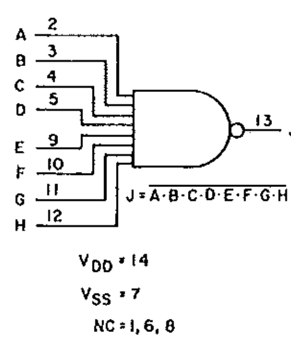


CD4063
4-Bit Magnitude Comparator

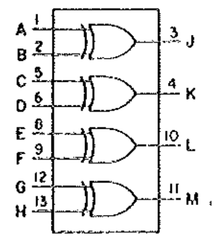


CD4016 **CD4066**

Quad Bilateral Switch

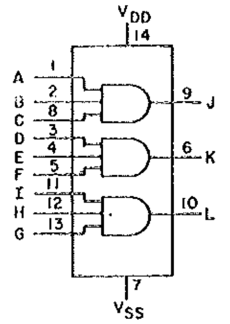


CD4068
8-Input NAND



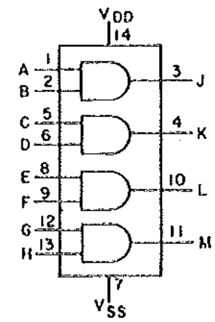
$J = A \oplus B$ $M = G \oplus H$
$K = C \oplus D$ $L = E \oplus F$
$V_{SS} = 14$
$V_{DD} = 7$

CD4070
Quad Exclusive-OR



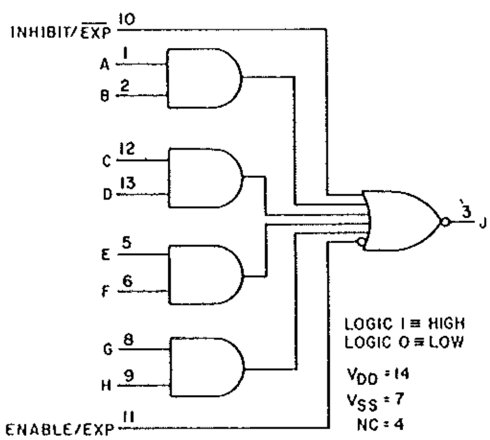
$J = A \cdot B \cdot C$ $L = G \cdot H \cdot I$
$K = D \cdot E \cdot F$

CD4073
Triple 3-Input AND



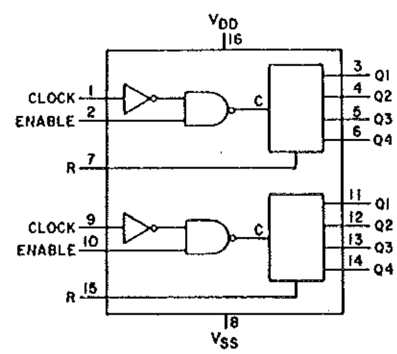
$J = A \cdot B$ $M = G \cdot H$
$K = C \cdot D$ $L = E \cdot F$

CD4081
Quad 2-Input AND



$J = \overline{INH + \overline{ENABLE} + AB + CD + EF + GH}$

CD4086
Expandable 4-Wide, 2-Input
AND/OR Invert (AOI)



CD4518
Dual BCD
Up-Counter

CD4520
Dual Binary
Up-Counter

GENERATOR BOARD OUTPUT POWER AMPLIFIER

Output Attenuator Knob Position	Absolute Output dBm		Power Amplifier Output		Power Amp Gain dB	Power Amp Input U29 out	U18 – 4066 Control Pin levels H = +7V L= –7V				Relays Operated	Meter Range H= +10V L = 0V		Meter send sig. U17 out	
	MIN	MAX	MIN	MAX			12	6	13	5		MSB	LSB	MIN	MAX
+30	+20	+34	+20	+34	+26	+20	H	H	H	H	RL6 RL7	L	L	+3	+17
+20	+10	+24	+10	+24	+16	+20	H	H	H	H	RL6	L	L	–7	+7
+10	0	+14	0	+14	+16	+10	H	H	H	L	RL6	L	L	–17	–3
0	–10	+4	+10	+24	+16	+20	H	H	H	H	RL4 RL5	L	L	–27	–13
–10	–20	–6	0	+14	+16	+10	L	L	H	L	RL4 RL5	L	H	–7	+7
–20	–30	–16	+10	+24	+16	+20	L	L	H	H	RL3	L	H	–17	–3
–30	–40	–26	0	+14	+16	+10	L	L	H	L	RL3	L	H	–27	–13
–40	–50	–36	+10	+24	+16	+20	L	L	L	H	RL2	H	L	–7	+7
–50	–60	–46	0	+14	+16	+10	L	L	L	L	RL2	H	L	–17	–3
–60	–70	–56	+10	+24	+16	+20	L	L	L	H	RL1	H	L	–27	–13
–70	–80	–66	0	+14	+16	+10	L	L	L	L	RL1	H	L	–37	–23

All signal levels in dBm for a sine wave source. Individual comb signals approximately 10dB lower.

Min/Max levels are variations with rotation of output level control.

METER DIGIT PRESETTING LOGIC TRUTH TABLE

INPUT RANGE SELECTED		+30/−30			0/−60		−30/−90		+30/−30		0/−60		−30/−90	
POST FILTER GAIN		0 dB							+30 dB					
INPUT SIGNAL LEVEL	MAX	+40	+30	0	0	−30	−30	−60	0	−30	−30	−60	−60	−90
	MIN	+30	0	−30	−30	−60	−60	−90	−30	−60	−60	−90	−90	−120
U38	Pin 5 MSB	L	L	L	L	L	H	H	L	L	L	L	H	H
	Pin 6 AUTO	L	L	H	L	H	L	H	L	H	L	H	L	H
	Pin 7 LSB	L	L	L	H	H	L	L	L	L	H	H	L	L
	Pin 9 PFG	L	L	L	L	L	L	L	H	H	H	H	H	H
	Pin 10	L	L	H	H	L	L	H	H	L	L	H	H	L
	Pin 11	L	L	L	L	H	H	H	L	H	H	H	H	L
	Pin 12	L	L	L	L	L	L	L	L	L	L	L	L	H
U25	Pin 4	H	H	L	L	H	H	L	L	H	H	L	L	H
	Pin 11	H	H	L	L	H	H	H	L	H	H	H	H	L
U26	Pin 3	L	H	L	L	H	H	L	L	H	H	L	L	H
	Pin 4	L	H	L	L	H	H	H	L	H	H	H	H	L
	Pin 10	H	H	H	H	L	L	L	H	L	L	L	L	H
	Pin 11	H	L	L	L	L	L	H	L	L	L	H	H	L
U39	Pin 9	H	H	L	L	L	L	L	L	L	L	L	L	L
U42	Pin 4	L	L	L	L	L	L	H	L	L	L	H	H	L
U47 (during Digit 3)	Pin 16 D	L	L	L	L	L	L	L	L	L	L	L	L	H
	Pin 17 C	H	L	L	L	L	L	H	L	L	L	H	H	L
	Pin 18 B	L	H	L	L	H	H	H	L	H	H	H	H	L
	Pin 19 A	L	H	L	L	H	H	L	L	H	H	L	L	H
DIGIT PRESET		4	3	0	0	3	3	6	0	3	3	6	6	9

INTEGRATED CIRCUIT POWER SUPPLY VOLTAGES

RECEIVER BOARD

DEVICE	TYPE	PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
U11	4063	8	GRD	16	+5V		
U12	4063	8	GRD	16	+5V		
U13	10K RNET						
U14	4520	8	GRD	16	+5V		
U15	4520	8	GRD	16	+5V		
U16	4011	7	GRD	14	+5V		
U17	4520	8	GRD	16	+5V		
U18	4013	7	GRD	14	+5V		
U19	100KRNET						
U110	LM325N	7	-15V	11	GRD	14	+15V
U111	LF356	4	-15V	7	+15V		
U112	LF356	4	-15V	7	+15V		
U21	4019	8	GRD	16	+5V		
U22	4019	8	GRD	16	+5V		
U23	4069	7	GRD	14	+5V		
U24	4013	7	GRD	14	+5V		
U25	4049	1	+5V	8	GRD		
U26	4053	7	-7V	8	GRD	16	+5V
U27	4013	7	GRD	14	+5V		
U28	4012	7	GRD	14	+5V		
U29	10K RNET						
U210	4081	7	GRD	14	+5V		
U211	LF357	4	-15V	7	+15V		
U212	LF357	4	-15V	7	+15V		
U213	LF356	4	-15V	7	+15V		
U214	4066	7	-7V	14	+7V		
U31	2102	9-13	GRD	10	+5V		
U32	2102	9-13	GRD	10	+5V		
U33	2102	9-13	GRD	10	+5V		
U34	2102	9-13	GRD	10	+5V		
U35	2102	9-13	GRD	10	+5V		
U36	2102	9-13	GRD	10	+5V		
U37	2102	9-13	GRD	10	+5V		
U38	2102	9-13	GRD	10	+5V		
U39	4086	7	GRD	14	+5V		
U310	4086	7	GRD	14	+5V		
U311	LF356	4	-15V	7	+15V		
U312	LF356	4	-15V	7	+15V		
U313	LM318	4	-15V	7	+15V		
U314	LM318	4	-15V	7	+15V		
U41	4053	7	-7V	8	GRD	16	+7V
U42	4035	8	GRD	16	+5V		
U43	4035	8	GRD	16	+5V		
U44	4098	3	+5V	13	+5V	16	+5V
U45	4013	7	GRD	14	+5V		
U46	10KRNET						
U47	10KRNET						
U48	LM301	4	-15V	7	+15V		
U49	LM301	4	-15V	7	+15V		
U410	LM310	4	-7V	7	+7V		
U411	LM310	4	-7V	7	+7V		
U412	LM310	4	-7V	7	+7V		
U413	LM310	4	-7V	7	+7V		
U51	LF356	4	-15V	7	+15V		
U52	3408	3	-15V	13	+5V	1,2,15	GND
U53	2KRNET						
U54	LM340 & 5.0	1	+9V	2	+5V	3	GND

INTEGRATED CIRCUIT POWER SUPPLY VOLTAGES

RECEIVER BOARD sheet 2 of 2

DEVICE	TYPE	PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
U55	4012	7	GRD	14	+5V		
U56	4049	1	+5V	8	GRD		
U57	4017	8	GRD	16	+5V		
U58	4040	8	GRD	16	+5V		
U59	4053	7	-7V	8	GRD	16	+7V
U510	4011	7	-7V	14	+7V		
U511	4052	7	-7V	8	-7V	16	+7V
U512	4052	7	-7V	8	-7V	16	+7V
U513	4052	7	-7V	8	-7V	16	+7V
U514	4052	7	-7V	8	-7V	16	+7V
U61	LM318	4	-15V	7	+15V		
U62	LM318	4	-15V	7	+15V		
U63	4013	7	GRD	14	+10V		
U64	LM311	4	-15V	8	+15V		
U65	LF356	4	-15V	7	+15V		
U66	LM301	4	-15V	7	+15V		
U67	LF356	4	-15V	7	+15V		
U68	AD536	3	-15V	9 - 10	GRD	14	+15V
U69	LF356	4	-15V	7	+15V		
U610	LM318	4	-15V	7	+15V		
U611	4025	7	-7V	14	+7V		
U612	4001	7	-7V	14	+7V		
U613	Custom RNET						
U614	LM310	4	-7V	7	+7V		
U615	Custom RNET						
U71	LF356	4	-15V	7	+15V		
U72	LF356	4	-15V	7	+15V		
U73	4053	7	-1.2V	8	GRD	16	+15V
U74	LF356	4	-15V	7	+15V		
U75	LF356	4	-15V	7	+15V		
U76	LM301	4	-15V	7	+15V		
U77	AD536	3	-15V	9 - 10	GRD	14	+15V
U78	LF356	4	-15V	7	+15V		
U79	4001	7	-7V	14	+7V		
U710	LF356	4	-7V	7	+7V		
U711	LM310	4	-7V	7	+7V		
U712	LF356	4	-7V	7	+7V		
U713	10K RNET						
U81	LM318	4	-15V	7	+15V		
U82	LM318	4	-15V	7	+15V		
U83	LF356	4	-15V	7	+15V		
U84	LF356	4	-15V	7	+15V		
U85	100K RNET						
U86	4066	7	-7V	14	+7V		
U87	4066	7	-7V	14	+7V		
U88	LF356	4	-7V	7	+7V		
U89	4053	7	-7V	8	-7V	16	+7V
U810	LM318	4	-7V	7	+7V		
U811	LM301	4	-7V	7	+7V		

INTEGRATED CIRCUIT POWER SUPPLY VOLTAGES

METER BOARD

Sheet 1 of 1

DEVICE	TYPE	PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
U11	4040	8	GRD	16	+10V		
U12	33KRNET						
U13	LM340 LAH-10	1	+15V	2	+10V	3	GRD
U14	LM301	4	GRD	7	+15V		
U21	4518	8	GRD	16	+10V		
U22	4081	7	GRD	14	+10V		
U23	4049	1	+10V	8	GRD		
U24	4011	7	GRD	14	+10V		
U25	4011	7	GRD	14	+10V		
U26	4070	7	GRD	14	+10V		
U27	LM301	4	−15V	7	+15V		
U28	LM301	4	−15V	7	+15V		
U29	LF356	4	−15V	7	+15V		
U210	LF356	4	−15V	7	+15V		
U211	LM311	4	−15V	8	+15V		
U31	4518	8	GRD	16	+10V		
U33	4013	7	GRD	14	+10V		
U34	4013	7	GRD	14	+10V		
U35	4013	7	GRD	14	+10V		
U36	75492	4	GRD via 1Ω	11	+10V		
U37	4019	8	GRD	16	+10V		
U38	4008	8	GRD	16	+10V		
U39	4025	7	GRD	14	+10V		
U310	LF356	4	−15V	7	+15V		
U311	4053	7	−5V	8	GRD	16	+10V
U312	LM318	4	−15V	7	+15V		
U312	LF356	4	−15V	7	+15V		
U314	LM325N	7	−15V	11	GRD	14	+15V
U315	AD536	3	−15V	9-10	GRD	14	+15V
U41	4027	8	GRD	16	+10V		
U42	4081	7	GRD	14	+10V		
U43	3082	5	GRD	15	+9V		
U44	470Ω RNET						
U45	47Ω RNET						
U46	75492	4	GRD via 1Ω	11	+10V		
U47	MK50395	1	+10V	22	GRD		
U48	LF356	4	−15V	7	+15V		
U49	LF356	4	−15V	7	+15V		
U410	LF356	4	−15V	7	+15V		
U411	LF356	4	−15V	7	+15V		

INTEGRATED CIRCUIT POWER SUPPLY VOLTAGES

GENERATOR BOARD

Sheet 1 of 2

DEVICE	TYPE	PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
U11	LM325N	7	-15V	11	GRD	14	+15V
U12	4011	7	GRD	14	+10V		
U13	4081	7	GRD	14	+10V		
U14	22K RNET						
U15	22K RNET						
U16	LF356	4	-7V	7	+7V		
U17	LM318	4	-15V	7	+15V		
U118	4066	7	-7V	14	+7V		
U21	4011	7	GRD	14	+10V		
U22	4081	7	GRD	14	+10V		
U23	22K RNET						
U24	3082	5	-7V	15	+7V		
U25	22K RNET						
U26	3082	5	-7V	15	+7V		
U27	4066	7	-7V	14	+7V		
U28	LF356	4	-15V	7	+15V		
U29	LF356	4	-15V	7	+15V		
U210	LF356	4	-15V	7	+15V		
U31	Custom RNET						
U32	4052	7	-7V	8	-7V	16	+7V
U33	4052	7	-7V	8	-7V	16	+7V
U34	4052	7	-7V	8	-7V	16	+7V
U35	Custom RNET						
U36	4011	7	GRD	14	+10V		
U37	4081	7	GRD	14	+10V		
U38	22K RNET						
U39	22K RNET						
U310	LM318	4	-15V	7	+15V		
U41	LM310	4	-7V	7	+7V		
U42	LM310	4	-7V	7	+7V		
U43	LM310	4	-7V	7	+7V		
U44	LM318	4	-7V	7	+7V		
U45	4040	8	GRD	16	+10V		
U46	4040	8	GRD	16	+10V		
U47	22K RNET						
U48	22K RNET						
U51	LM310	4	-7V	7	+7V		
U52	LM310	4	-7V	7	+7V		
U53	LM310	4	-7V	7	+7V		
U54	4052	7	-7V	8	-7V	16	+7V
U55	LM301	4	-7V	7	+7V		
U56	LF356	4	-7V	7	+7V		
U57	10K RNET						
U58	10K RNET						
U59	22K RNET						
U510	3082	5	-7V	15	+7V		
U61	LM318	4	-7V	7	+7V		
U62	LM318	4	-7V	7	+7V		
U63	10K RNET						
U64	4066	7	-7V	14	+7V		
U65	4029	8	-7V	16	+7V		
U66	4029	8	-7V	16	+7V		
U67	4040	8	-7V	16	+7V		
U68	22K RNET						
U69	220Ω RNET						
U71	LM318	4	-7V	7	+7V		
U72	10K RNET						

INTEGRATED CIRCUIT POWER SUPPLY VOLTAGES

GENERATOR BOARD

Sheet 2 of 2

DEVICE	TYPE	PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
U73	4066	7	-7V	14	+7V		
U74	4073	7	-7V	14	+7V		
U75	4049	1	+7V	8	-7V		
U76	4027	8	-7V	16	+7V		
U77	4070	7	-7V	14	+7V		
U78	10K RNET						
U79	4520	8	GRD	16	+10V		
U710	4027	8	GRD	16	+10V		
U711	4006	7	-7V	14	+7V		
U81	LM318	4	-7V	7	+7V		
U82	LF356	4	-15V	7	+15V		
U83	LM310	4	-15V	7	+15V		
U84	4001	7	-7V	14	+7V		
U85	100K RNET						
U86	4011	7	-7V	14	+7V		
U87	100K RNET						
U88	4011	7	-7V	14	+7V		
U89	4011	7	-7V	14	+7V		
U810	4013	7	-7V	14	+7V		
U811	4006	7	-7V	14	+7V		
U812	4013	7	-7V	14	+7V		
U813	4040	8	-7V	16	+7V		
U814	LF357	4	-15V	7	+15V		
U815	LF356	4	-15V	7	+15V		
U91	LM301	4	-7V	7	+7V		
U92	LM567	4	+7V*	7	GRD		

*+7Volt in Auto Start reproduce mode only.

PARTS LIST

ASSEMBLY	4400-700-06 TOTAL ASSEMBLY
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ AUG 78 — SHEET 1 OF 1

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
	4400-710-06	Receiver Sub Ass'y	AMBER	1
	4400-720-06	Meter Sub Ass'y	AMBER	1
	4400-730-06	Generator Sub Ass'y	AMBER	1
	4400-645-04	Plastic Front Panel	AMBER	1
	4400-610-05	Top Cover	AMBER	1
	4400-610-05	Bottom Cover	AMBER	1
	4400-622-03	Chassis	AMBER	1
	4400-625-04	Side Bracket	AMBER	2
	4400-630-08	Rear Panel	AMBER	1
	4400-640-06	Front Underlay	AMBER	1
	4400-653-02	Dress Strip	AMBER	4
	4400-655-01	Handle Ass'y	AMBER	2
	10 x F10	10 Position Switch Ass'y	SCHADOW	1
	14-024-108	Ribbon Cable	ARIES	1
	7211SYZG	3 Position ON-ON-ON TOGGLE	C&K	3
	4400-0100-03	Transformer	HAMMOND	1
	4400-635-01	Transformer Bracket	AMBER	1
	6J4	Power Filter, Connector	CORCOM	1
		Fuse	FUSETRON	1
	KC-79-131	BNC Receptacles	KINGS	9
	2201-2151	Housing 15 Position	MOLEX	1
		Housing 4 position	MOLEX	14
	0856-0110	Crimp Terminals, gold	MOLEX	71
	1504-9209	Crimp Terminals, round	MOLEX	7
		Harness Assembly	AMBER	1
	RB67-IB-SKML	Knob Bar Skirted	ROGAN	4
	RB67-ISK7-DML	Knob Concentric	ROGAN	4
	RB67-ODCML	Knob, Round	ROGAN	4
		Vinyl Feet & Ball Ass'y	BUCKEYE	1
	17250B	Power Cord	BELDEN	1
		Ground Lug No. 4	VARIOUS	1
		Ground Lug 3/8" I.D.	VARIOUS	9
		Nylon Washer No. 10	VARIOUS	2
	2668	Nylon Washer BNC	SMITH	9
	5614-18-31	Nylon Spacer BNC	SEASTROM	9
	4-40 x 3/16"	Spacer, threaded brass 1/2" AF	VARIOUS	2
Panel Hold Down	2-56 x 1/4"	Screw, Flat Head, Black	VARIOUS	1
Panel Hold Down	2-56 x 1/4"	Screw, Flat Head, Yellow Cad	VARIOUS	1
Frame Ass'y	4-40 x 1/4"	Screw, Flat Head, Yellow Cad	VARIOUS	32
Cover	4-40 x 3/8"	Screw, Flat Yellow Cad	VARIOUS	20
Flat Cable, Sw	4-40 x 1/4"	Screw, Pan Head, Yellow Cad	VARIOUS	7
Feet, Rear	4-40 x 3/8"	Screw, Pan Head, Yellow Cad	VARIOUS	4
PCB, XFRM Mount	6-32 x 5/16"	Screw, Pan Head, Yellow Cad	VARIOUS	15
PCB Mount	6-32 x 1/2"	Screw, Pan Head, Yellow Cad	VARIOUS	1
Feet Bottom	6-32 x 1/2"	Screw, Pan Yellow Cad	VARIOUS	6
Misc	No 4	Lock Washer, Int Tooth	VARIOUS	7
Misc	No 6	Lock Washer, Int Tooth	VARIOUS	16
Controls	1/4" I.D.	Lock Washer, Int Tooth	VARIOUS	8
Controls	3/8" I.D.	Lock Washer, Int Tooth	VARIOUS	2
	4-40 x 1/4" AF	Hex Nuts, Yellow Cad	VARIOUS	5
Controls	3/8 x 32 x 7/16" AF	Hex Nuts, Yellow Cad	VARIOUS	8
Controls	1/4" x 32 x 5/16 AF	Hex Nuts, Yellow Cad	VARIOUS	2

PARTS LIST

ASSEMBLY	RECEIVER BOARD (4400-710-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 1 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
U612,79	CD4001B	QUAD 2 IN NOR	VARIOUS	2
U16,510	CD4011B	QUAD 2 IN NAND	VARIOUS	2
U28 55	CD4012B	DUAL 4 IN NAND	VARIOUS	2
U18,24,27,45.63	CD4013B	DUAL D-FLIP-FLOP	VARIOUS	5
U57	CD4017B	DECADE COUNTER	VARIOUS	1
U21,22	CD4019B	QUAD AND/OR	VARIOUS	2
U611	CD4025B	TRI 3 IN NOR	VARIOUS	1
U42,43	CD4035B	4 BIT SHIFT REGISTER	VARIOUS	2
U58	CD4040B	BINARY COUNTER	VARIOUS	1
U25,56	CD4049B	HEX INVERTER	VARIOUS	2
U511 thru 514	CD4052B	MUX/DEMUX	VARIOUS	4
U26,41,59,73·89	CD4053B	MUX/DEMUX	VARIOUS	5
U11,12	CD4063B	4 BIT COMPARATOR	VARIOUS	2
U86,87,214	CD4066B	QUAD SWITCH	VARIOUS	3
U23	CD4068B	8-IN NAND	VARIOUS	1
U210	CD4081B	DUAL 4 IN AND	VARIOUS	1
U39,310	CD4086B	QUAD 2 IN AND/OR INVERT	VARIOUS	2
U44	CD4098B	DUAL 1-SHOT	VARIOUS	1
U14,15,17	CD4520B	DUAL UP COUNTER	VARIOUS	3
U52	MC3408	LIN 8 BIT D/A	VARIOUS	1
U68,77	AD536AJD	LIN RMS to DC CONV.	VARIOUS	2
U31 thru 38	2102	1K x 1 RAM	VARIOUS	8
U48,49,66,76,811	LM301N	LIN OP AMP	VARIOUS	5
U410 thru 413, 614, 711	LM310N	LIN OP AMP	VARIOUS	6
U64	LM311N	LIN VOLT COMP	VARIOUS	1
U313,314,61,62,610 81,82	LM318N	LIN OP AMP	VARIOUS	7
U110	LM325N	LIN ±5V REGULATOR	VARIOUS	1
U54	LM340TO5	LIN +5V REGULATOR	VARIOUS	1
U111,112,213,311, 312,51,65,67,69, 71,72,74,75,78,710 712,83,84,88,810	LF356N	LIN BIFET OP AMP	VARIOUS	20
U211,212	LF357N	LIN BIFET OP AMP	VARIOUS	2
U19	314A104	Resistor Network 100K	A-B	1
U53	314B202	Resistor Network 2K	A-B	1
U85	316A104	Resistor Network 100K	A-B	1
U13,29,46,47,713	316B103	Resistor Network 10K	A-B	5
U613,615	1000-4404/CBD788	Resistor Network Custom	A-B	2
		All resistors 1/4w ±5% unless otherwise stated. *indicates leads formed for vertical mounting, all others horizontal mounting.		
R15,20,21,22		2.2Ω	VARIOUS	4
R242		15Ω	VARIOUS	1
R88,245		51Ω	VARIOUS	2
R23,37,249,250,252		100Ω	VARIOUS	5
R177 thru 182		100Ω ±1%	A-B	6
R90,244		220Ω	VARIOUS	2
R100,110 218,219		270Ω	VARIOUS	4
RT1,RT2		330Ω positive temco thermistor,	TI	2
R170,171		360Ω	VARIOUS	2

PARTS LIST

ASSEMBLY	RECEIVER BOARD (4400-710-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 2 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		All resistors 1/4w ±5% unless otherwise stated. * indicates leads formed for vertical mounting, all others horizontal mounting.		
R16,17,18,19,112, 114,123,125		470Ω	VARIOUS	8
R246,247		560Ω	VARIOUS	2
R146*,147*		820Ω	VARIOUS	2
R221,225		976Ω ±1%	A-B	2
R1 31,36*,45,50*, 94,142,188,190,205, 228,238		1kΩ	VARIOUS	12
R62,63,67,68,69,70 71,72,73,74,98,104		3.9kΩ	VARIOUS	12
R30*,44*,162		4.7kΩ	VARIOUS	3
R35,49,75,78,82,83, 167 ,260		5.1kΩ	VARIOUS	8
R220,227		5.90kΩ ±1%	A-B	2
R91,95		8.2kΩ	VARIOUS	2
R2,3,4,6,7,8,9,14, 25,33*,34*,39,47*, 48*,51*,52*,53*,54*, 55* 56* 87,93,96,* 97* 99,102,107,108, 109*,113,116,118,106 119,120 124,127,129, 130,131,132,133 134, 135,143*,152,159,160 168,169,174,183 184, 185,192,200,202*, 207*.208,209,210, 211 212,213 214,215* 216*,230,231 234, 236,237,240,243,251* 259, ,262,263 264,		10kΩ	VARIOUS	79
R186,187,261		10.0kΩ ±1%	A-B	3
R233		10.2kΩ ±1%	A-B	1
R79,80,165		11k	VARIOUS	3
R115,117,126 128		12k	VARIOUS	4
R153		15k	VARIOUS	1
R57,58,103,111,157, 201,204		20k	VARIOUS	7
R86,173,203,239, 253,*		30k	VARIOUS	5
R223,226		34.0kΩ ±1%	A-B	2
R66 161,163,166,175		36k	VARIOUS	5
R199,206		43k	VARIOUS	2
R26,28*,40,42*		47k	VARIOUS	4
R61.64,65		49.9kΩ ±1%	A-B	3
R241,248		51kΩ	VARIOUS	2
R59,60		91kΩ	VARIOUS	2
R148		7.5KΩ	VARIOUS	1

PARTS LIST

ASSEMBLY	RECEIVER BOARD (4400-710-06)	
USED ON	4400 MULTIPURPOSE AUDIO TEST SET	
PREPARED	WJ JULY 78	SHEET 3 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		All resistors 1/4w ±5% unless otherwise stated, * indicates leads formed for vertical mounting, all others horizontal mounting.		
R5,10,11*,12*,13, 24,38,85*,89,136, 137,138,139,140,158, 172,176,217,256*, 258*,		100kΩ	VARIOUS	20
R144,145		100kΩ ±1%	A-B	2
R76,77,81,84		160kΩ	VARIOUS	4
R222,224		191kΩ ±1%	A-B	2
R121,122,164		200kΩ	VARIOUS	3
R149*,150*,151*,154* 155*,156*,257*		270KΩ	VARIOUS	7
R229		316kΩ ±1%	A-B	1
R189,191		330kΩ	VARIOUS	2
R141,254*		430kΩ	VARIOUS	2
R27*,29*,32,41*,43*, 46,101,105,235,		1MΩ	VARIOUS	9
R193 194,195,196, 197,198		1.00MΩ ±1%	A-B	6
RV1,2,4,5,8,9,10, 11,12,13,14,16,	E2A103	10K Trim Pot	A-B	12
RV3,6,7,15	E2A503	50K Trim Pot	A-B	4
C 16,17,18,19, 23,30,38,39,42 thru 45 56,57,67,68,69 70 thru 73,88,90,91, 103 106,107,108,112, 113,115,117,119,127		0.1 Ceramic Disc	Various	34
C6,7,31,34 62,135		4.7/35V Tantalum	VARIOUS	6
C4,5,10 thru 15, 63,99 thru 102 129,130,50,51,131, 132,133,134		10/35V Tantalum	VARIOUS	22
C52,53,104 105,8,9		22/35 Tantalum	VARIOUS	6
C61		100/25 Electrolytic	VARIOUS	1
C20,37,46, thru 49, 116		3.3pF Ceramic Disc	VARIOUS	7
C109,110,111		10pF Ceramic Disc	VARIOUS	3
C21,22,40,41,122		30pF Ceramic Disc	VARIOUS	5
C55,58		47pF Ceramic Disc	VARIOUS	2
C64,65,66,74,75, 125,128		100pF Ceramic Disc	VARIOUS	7
C94		150pF Ceramic Disc	VARIOUS	1
C25,26,28,29,93,126		0.01µF Ceramic Disc	VARIOUS	6
C123,124	CM06FD821G03	820pF 2% Dipped Mica	VARIOUS	2
C92,120,121	CM06FD332G03	3300pF 2% Dipped Mica	VARIOUS	3
C89,54		0.001Film	VARIOUS	2
C59		0.0022 Film	WIMA	1
C60		0.0047 Film	WIMA	1
C3		0.01 Film	WIMA	1

PARTS LIST

ASSEMBLY	RECEIVER BOARD (4400-710-06)	
USED ON	4400 MULTIPURPOSE AUDIO TEST SET	
PREPARED	WJ JULY 78	SHEET 4 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
C78,81,84,87		0.022 Film	WIMA	4
C35,36		0.047 Film	WIMA	2
C1,32,33,76,79,82, 85,96,98		0.1 Film	WIMA	9
C77,80,83,86		0.15 Film	WIMA	4
C95,97		0.47 Film	WIMA	2
C2		0.68 Film	WIMA	1
CV1		7-25pF Trimming Capacitor	ERIE	1
CR1 thru CR54 CR61 thru CR68, CR70 thru CR73	1N4148	Diode GEN PURPOSE	VARIOUS	66
CR55 thru CR60 69	MV5054	LED TI-3/4 Red Diffused	VARIOUS	7
Q2,10,12,13,15 thru 21,23 24	2N4401	NPN GEN PURPOSE	VARIOUS	13
Q3,9,11,14,22	2N4403	PNP GEN PURPOSE	VARIOUS	5
Q4,5,6,25	2N6474	NPN 16w/120v	VARIOUS	4
Q1	2N6476	PNP 16w/120v	VARIOUS	1
Q7,8	2N4861	FET N-CHANNEL	VARIOUS	2
S2 thru S4		Custom Switch Assy 3 x F type	SCHADOW	1
S7 thru S20		Custom Switch Assy 14 x F type	SCHADOW	1
S1, RV17	4400-0792	Pot Switch Combination	A-B	1
S22,RV20	4400-0793	Pot Switch Combination	A-B	1
S5,6,RV18,19	4400-0794	Pot Switch Combination	A-B	1
RV21 thru 24	4400-0795	Quad Pot Combination	A-B	1
S21	71BF30-1-1-11-N	Switch Rotary 11 Position	GRAYHILL	1
	76B05	5 Position Rocker Dip Switch	GRAYHILL	1
	6030B	Heatsink	THERMALLOY	1
J1,2	609-2602-MR/	Connector 26 Pin	ANSLEY/3M	2
J3,4,5,7,8,9,10, 11	2227-2041	Connector 4 Pin Header, Locking	MOLEX	8
		I.C. Socket 8 Pin	VARIOUS	33
		I.C. Socket 14 Pin	VARIOUS	22
		I.C. Socket 16 Pin	VARIOUS	36
		Machine Socket 14 Pin	AUGAT	1
	6-32 x 3/8 Pan HD	Screw	VARIOUS	1
	6-32	Hex Nut	VARIOUS	1
	4400-410-06	Printed Circuit Board	AMBER	1

PARTS LIST

ASSEMBLY	METER BOARD (4400-720-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 1 OF 3

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
U38	CD4008B	4 BIT FULL ADDER	VARIOUS	1
U24, 25	CD4011B	QUAD 2 In NAND	VARIOUS	2
U33,34,35	CD4013B	DUAL D FLIP-FLOP	VARIOUS	3
U37	CD4019B	QUAD AND-OR	VARIOUS	1
U39	CD4025B	TRI 3-IN NOR	VARIOUS	1
U32,41	CD4027B	DUAL J-K FLIP FLOP	VARIOUS	2
U26	CD4030/CD4070 B	QUAD EXCL-OR	VARIOUS	1
U11	CD4040B	UP COUNTER	VARIOUS	1
U23	CD4049B	HEX INVERTER	VARIOUS	1
U311	CD4053B	TRI 2-CH MUX/DEMUX	VARIOUS	1
U22,42	CD4081B	DUAL 4-in AND	VARIOUS	2
U21,31	CD4518B	DUAL DECADE UP COUNTER	VARIOUS	2
U43	CA3082	LIN NPN XSTR ARRAY	VARIOUS	1
U315	AD536AJD	RMS to DC CONVERTER	Analog Device	1
U47	MK50395	Six digit decade Counter	VARIOUS	1
U36,46	SN75492	LIN MOS to VLED DRIVER	VARIOUS	2
U14, 27, 28	LM301AN	LIN OP AMP	VARIOUS	3
U211	LM311N	LIN COMPARATOR	VARIOUS	1
U312	LM318N	LIN PRECISION OP AMP	VARIOUS	1
U314	LM325N	LIN ±15V REGULATOR	VARIOUS	1
U29, 210,310,313, 48,49,410,411	LF356N	LIN BIFET OP AMP	VARIOUS	8
U13	LH0070/LM340-10	LIN +10V Precision Reference	VARIOUS	1
U45	314B470	47Ω Resistor Network	A-B	1
U44	314B471	470Ω Resistor Network	A-B	1
U12	314B333	33K Resistor Network	A-B	1
U51	MAN6650	LED 1-1/2 digit common cathode	MONSANTO	1
U52,53	MAN6640	LED 2 digit common cathode	MONSANTO	2
		All Resistors 1/4W ±5% unless otherwise stated.		
R4		33Ω 1/2w	VARIOUS	1
R1,2		0.51Ω 2w	VARIOUS	2
R54,55		1Ω 1/2w	VARIOUS	2
R49		2.2Ω 2w	VARIOUS	1
R20,21		2.2Ω	VARIOUS	2
R29		100Ω	VARIOUS	1
R18,57,58,61		180Ω	VARIOUS	4
R5		220Ω	VARIOUS	1
R52 53		330Ω	VARIOUS	2
R60		470Ω	VARIOUS	1
R26,27,30,31 40,51,63		1K	VARIOUS	7
R56		1.8K	VARIOUS	1
R25		2K	VARIOUS	1
R28,34		5.1K	VARIOUS	2
R3,6,8,9,16 19,22,24,35,50,59 62,64,65,73,78,79, 80,81		10K	VARIOUS	19
R75,76,77		10K ±1%	A-B	3
R36		7.5K	VARIOUS	1
R72		16K	VARIOUS	1
R42,47		24K	VARIOUS	2

PARTS LIST

ASSEMBLY	METER BOARD (4400-720-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 2 OF 3

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		All resistors 1/4w ±5% unless otherwise stated.		
R17,67,68		33K	VARIOUS	3
R46,66,69,71,74		47K	VARIOUS	5
R11,12,13,23,48		100K	VARIOUS	5
R32,33		160K	VARIOUS	2
R7, 15		390K	VARIOUS	2
R14,		430K	VARIOUS	1
R10		620K	VARIOUS	1
R41		1M	VARIOUS	1
R43,44,45		10M	VARIOUS	3
RV2	E2A-104	100K Trim Pot	A-B	1
RV3,5,11	E2A-103	10K TRIM POT	A-B	3
RV1, 4,6,7,10	E2A-503	50K TRIM POT	A-B	5
RV12	4400-0791	5K LOG POT	A-B	1
		Capacitors. All values in µF unless otherwise stated.		
C18		47/16V Electrolytic	VARIOUS	1
C3,15,16		100/25V Electrolytic	VARIOUS	3
C5,6		220/63V Electrolytic	VARIOUS	2
C9,10		1000/40V Electrolytic	VARIOUS	2
C1,4		2200/25V Electrolytic	VARIOUS	2
C11,32,33,45,46, 53,56,57,58,59,54		10/35V Tant	VARIOUS	11
C36,37,48,50,51		4.7/35V Tantalum	VARIOUS	5
C7,8,14,17,19,21 22,27,29,31,42,43, 44,47,60,61,68,71, 72		0.1 Ceramic Disc	VARIOUS	19
C67		150pf Film	WIMA	1
C65		0.001 Film	WIMA	1
C66		0.0033 Film	WIMA	1
C25		0.022 Film	WIMA	1
C24,39,55,70		0.1 Film	WIMA	4
C26		0.15 Film	WIMA	1
C69		0.47 Film	WIMA	1
C40,41,62,63		3.3pF Ceramic Disc	VARIOUS	4
C38,64		10pF Ceramic Disc	VARIOUS	2
C49		30pF Ceramic Disc	VARIOUS	1
C12,20,23,30,34, 52		100pF Ceramic Disc	VARIOUS	6
C13,C35		0.01µF Ceramic Disc	VARIOUS	2
C28		0.015 NPO TEMPCO	VARIOUS	1

PARTS LIST

ASSEMBLY	METER BOARD (4400-720-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 3 OF 3

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
CR13 thru 18	1N4148	Diode, Gen Purpose	VARIOUS	6
CR1 thru 12	1N5404	Rectifier Diode 3A/400V	VARIOUS	12
CR19 thru 22	MV5054	LED TI-3/4 Red Diff.	VARIOUS	4
Q4,7,8,9	2N4401	NPN Gen, Purpose	VARIOUS	4
Q5,6	2N4403	PNP Gen, Purpose	VARIOUS	2
Q1, 2,3,	2N6474	NPN 16w/120V	VARIOUS	3
S1-14	16 x F12.5FA201	Switch Assembly	SCHADOW	1
M1	ME-DUA-500	Meter 500 uA, Custom Scale	MODUTEC	1
	6030B	Heat Sink	THERMALLOY	1
		Heat Sink Washer		1
J1,2,3	609-2603	Connector 26 PIN	ANSLEY	3
J5 6,7,8,9	4180-4AG	Connector 4 PIN HEADER	MOLEX	5
J4	4180-15AG	Connector 15 PIN HEADER	MOLEX	1
		Socket 8 PIN DUAL in line	VARIOUS	13
		Socket 14 PIN DUAL in line	VARIOUS	13
		Socket 16 PIN DUAL in line	VARIOUS	10
		Socket 40 PIN DUAL in line	VARIOUS	1
J11		Socket 16 PIN DIL Machined contact		1
	501-18-CLR	Socket 18 PIN Right Angle	GARRY	3
	6-32 x 5/16	Screw, Pan Head	VARIOUS	1
	6-32	Hexnut	VARIOUS	1
	4400-420-06	Printed Circuit Board	AMBER	1
	171-26	Flat Cable	ANSLEY	3
	609-2600M	Connector 26 PIN socket	ANSLEY	4
	609-255	Connector 25 PIN	ANSLEY	2

PARTS LIST

ASSEMBLY	GENERATOR BOARD (4400-730-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 1 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
U84	CD4001B	IC, CMOS, QUAD 2 in NOR	VARIOUS	1
U711,811	CD4006B	IC, CMOS 18 STAGE S-R	VARIOUS	2
U12,21 36 86,88, 89	CD4011B	IC, CMOS QUAD 2 in NAND	VARIOUS	6
U810,812	CD4013B	IC,CMOS DUAL D FLIP FLOP	VARIOUS	2
U76,710	CD4027B	IC, CMOS DUAL J-K FLIP FLOP	VARIOUS	2
U65,66	CD4029B	IC, CMOS UP/DOWN COUNTER	VARIOUS	2
U77	CD4030B	IC CMOS QUAD EXCL-OR	VARIOUS	1
U45,46,67,813	CD4040B	IC, CMOS BINARY COUNTER	VARIOUS	4
U75	CD4049B	IC, CMOS HEX INVERTER	VARIOUS	1
U32,33,34,54	CD4052B	IC, CMOS MUX, DEMUX	VARIOUS	4
U18,27 64,73	CD4066B	IC, CMOS QUAD SWITCH	VARIOUS	4
U74	CD4073B	IC, CMOS TRI 3 in AND	VARIOUS	1
U13,22,37	CD4081B	IC, CMOS DUAL 4in AND	VARIOUS	3
U79	CD4520B	IC, CMOS DUAL UP COUNTER	VARIOUS	1
U24,26,510	CA3082	IC, LIN XSTR ARRAY	VARIOUS	3
U55 91	LM301N	IC, LIN OP AMP	VARIOUS	2
U41,42,43,51,52, 53,83	LM310N	IC, LIN OP AMP	VARIOUS	7
U17,310,44, 81	LM318N	IC, LIN PRECISION OP AMP	VARIOUS	4
U11	LM325N	IC, LIN ±15V REGULATOR	VARIOUS	1
U16,28,29,210,56, 82,815,61,62,71	LF356N	IC LIN BIFET OP AMP	VARIOUS	10
U814	LF357N	IC LIN BIFET OP AMP	VARIOUS	1
U92	NE567N	LIN TONE DECODER	VARIOUS	1
U69	314B221	Resistor Network 220Ω	A-B	1
U57,58	314A103	Resistor Network 10kΩ	A-B	2
U68,72	314B103	Resistor Network 10KΩ	A-B	2
U78	316B103	Resistor Network 10kΩ	A-B	1
U14,15,23,25,28 39,47,48,59,68	316B223	Resistor Network 22kΩ	A-B	10
U85	314A104	Resistor Network 100kΩ	A-B	1
U87	316B104	Resistor Network 100kΩ	A-B	1
U31,35	1000-4404/CBD788	Resistor Network CUSTOM	A-B	2
		All resistors 1/4w ±5% Unless otherwise stated * indicates leads formed for vertical mounting, all others horizontal mounting.		
R1,2,3,8,74,79		2.2Ω	VARIOUS	6
R72		49.9Ω ±1% 2W	A-B	1
R54,55,56		49.9Ω ±1%	A-B	3
R57		54.9Ω ±1%	A-B	1
R52,123,155,172, 173		100Ω	VARIOUS	5
R73,78		220Ω	VARIOUS	2
R159,166,167,168		270Ω	VARIOUS	4
R7-1 thru R7-10 R10-1 thru R10-10 R4,5,6,76,118, 124,169		470Ω	VARIOUS	27

PARTS LIST

ASSEMBLY	GENERATOR BOARD (4400-730-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 2 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		All resistors 1/4w ±5% unless otherwise stated. * indicates leads formed for vertical mounting all others horizontal mounting.		
R69		499Ω ±1%	A-B	1
R137,138		560Ω	VARIOUS	2
R86		680Ω	VARIOUS	1
R131*		750Ω	VARIOUS	1
R98,102		976Ω ±1%	A-B	2
R16,94,112,119,139*, 140*,144*,147*,152* 177, 178,		1kΩ	VARIOUS	11
R163		1.5KΩ	VARIOUS	1
R70,71,		1.6KΩ 2w	VARIOUS	2
R75,39		2kΩ	VARIOUS	2
R88		2.4kΩ	VARIOUS	1
R17,87,127*,153		2.7kΩ	VARIOUS	4
R93,110,128		3.3kΩ	VARIOUS	3
R30,35,37 38		3.9k	VARIOUS	4
R146*,148,149,151 164,165,174		4.7kΩ	VARIOUS	7
R68		4.99 kΩ ±1%	A-B	1
R18,29		5.1kΩ	VARIOUS	2
R95,100		5.90kΩ ±1%	A-B	2
R89,145*		6.8kΩ	VARIOUS	2
R32, 109,154		7.5kΩ	VARIOUS	3
R9*,11*,12*,13*, R14-1 thru R14-10, R15,19,25,33,41, 47,48,49,50,51,53, 58,59,60,61,77, 97, 104,106 107,108, 111,113*,114*,115*, 117,121,122,129*, 156,158,160,161,170* 171*,175,176		10kΩ	VARIOUS	51
R31		11kΩ	VARIOUS	1
R132*		15kΩ	VARIOUS	1
R126		16kΩ	VARIOUS	1
R91,92		20kΩ	VARIOUS	2
R42		22kΩ	VARIOUS	1
R85,90		24.3kΩ ±1%	A-B	2
R20		27kΩ	VARIOUS	1
R34,36,130*,133*		33k	VARIOUS	4
R99,101		34KΩ ±1%	A-B	2
R24,82		39kΩ	VARIOUS	2
R67		49.9kΩ ±1%	A-B	1
R21,44,45		51kΩ	VARIOUS	3
R125		82kΩ	VARIOUS	1
R22,26,62,63,64,65, 120,136*,142*,150 157*		100kΩ	VARIOUS	11
R80,81		100kΩ ±1%	A-B	2
R27,28,135*		160kΩ	VARIOUS	3

PARTS LIST

ASSEMBLY	GENERATOR BOARD (4400-730-06)
USED ON	4400 MULTIPURPOSE AUDIO TEST SET
PREPARED	WJ JULY 78 — SHEET 3 OF 4

DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		All resistors 1/4w ±5% unless otherwise stated. *indicates leads formed for vertical mounting, all others horizontal mounting.		
R96 103		191kΩ ±1%	A-B	2
R43,46, 134*		220kΩ	VARIOUS	3
R116*		270kΩ	VARIOUS	1
R141		330kΩ	VARIOUS	1
R66		499kΩ ±1%	A-B	1
R23, 105		1MΩ	VARIOUS	2
RV13-1 thru RV13-10 RV1,2,3,4,5,7,8	E2A103	10K TRIM POTS	A-B	17
RV6	E2A503	50K TRIM POT		1
		Capacitors. All values in μF unless otherwise stated.		
C3-10, C5-10		150pF Film	WIMA	2
C3-9, C5-9, 31, 54		330pF Film	WIMA	4
C1-10, C2-10, C3-8 C5-8, C11		680pF Film	WIMA	5
C1-9, C5-7		0.001 Film	WIMA	2
C2-9, C3-7 C4-10, 12		0.0015 Film	WIMA	4
C1-8, C5-6		0.0022 Film	WIMA	2
C2-8, C3-6, C4-9, 13 48		0.003 Film	WIMA	5
C1-7, C4-8, C5-5		0.0047 Film	WIMA	3
C2-7, C3-5, 14		0.0068 Film	WIMA	3
C1-6, C2-6, C3-4, C4-7, C5-4, C30, 78 82		0.01 Film	WIMA	8
C15		0.015 Film	WIMA	1
C1-5, C2-5, C3-3, C4-6, C5-3, 49, 68		0.022 Film	WIMA	7
C1-4, C5-2, 16		0.033 Film	WIMA	3
C2-4, C3-2, C4-5,		0.047 Film	WIMA	3
C1-3, C5-1, C17, 69, 52		0.068 Film	WIMA	5
C2-3, C3-1, C4-4, C46, 76		0.1 Film	WIMA	5
C1-2, C4-3		0.15 Film	WIMA	2
C2-2, C71, 72, 77		0.22 Film	WIMA	4
C1-1, C2-1, C4-2 65		0.33 Film	WIMA	4
C75 88, 89		0.47 Film	WIMA	3
C4-1, C70, 80		0.68 Film	WIMA	3
C22, 23, 33, 34, 98, 99		3.3pF Ceramic Disc	VARIOUS	6
C32, 37, 38, 45, 74, 95, 101		10pF Ceramic Disc	VARIOUS	7
C26		30pF Ceramic Disc	VARIOUS	1
C100		47pF Ceramic Disc	VARIOUS	1
C39, 47, 64, 81, 93		100pF Ceramic Disc	VARIOUS	5
C73, 104		150pF Ceramic Disc	VARIOUS	2
C29		470pF Ceramic Disc	VARIOUS	1
C79, 92		0.01 Ceramic Disc	VARIOUS	2

PARTS LIST

ASSEMBLY	GENERATOR BOARD (4400-730-06)	
USED ON	4400 MULTIPURPOSE AUDIO TEST SET	
PREPARED	WJ JULY 78	SHEET 4 OF 4

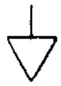
DESIGNATION	PART NUMBER	DESCRIPTION	MFGR	QTY
		Capacitors. All values in μF unless otherwise stated.		
C60,62	CM06FD821G03	820pF 2% Dipped Mica	VARIOUS	2
C61,63	CM06FD332G03	3300pF 2% Dipped Mica	VARIOUS	2
C20, 21 24,25,27, 28,35,36 40 thru 44,50 53,55,56,57 58,59, 83 thru 87		0.1 Ceramic Disc	VARIOUS	25
C7,8,51,90,91		4.7/35V Tantalum	VARIOUS	5
C6,9 10,18,19,94 96,97,102,103		10/35V Tantalum	VARIOUS	6
C66,67		22/35V Tantalum	VARIOUS	2
CR46	1N750	Zener 4.7V 400mV	VARIOUS	1
CR92	1N821	Zener 6.2V	VARIOUS	1
CR1 thru 45, CR47 thru 50, CR55 thru 84,90,91,93	1N4148	Diode General Purpose	VARIOUS	82
CR53,54	1N4745	Zener 16V 1W	VARIOUS	2
CR85 thru 89	MV5054	LED TI-3/4 red diffused	VARIOUS	5
Q25	2N2243	NPN HI-VOLTAGE		1
Q27	2N4031	PNP HI-VOLTAGE		1
Q4 7,8,10,13 15, 16,17,19,21,22,23, 24 28	2N4401	NPN GEN PURPOSE	VARIOUS	14
Q5,9,11,14,18,20, 26,32	2N4403	PNP GEN PURPOSE	VARIOUS	8
Q12	2N4861	FET N-CHANNEL	VARIOUS	1
Q1,2,6,31	2N6474	NPN 16w/120V	RCA	4
Q3,29	2N6476	PNP 16w/120V	RCA	2
Q30	T1P29A	NPN Power	TI	1
X1		3.072 MHz Crystal	AMBER	1
RL1 thru RL7	925A12C1A	Relay 12V, 1A Contact	CP CLARE	7
S2,15,16	71BF30-1-1-11-N	Switch Rotary 11 pos.	GRAYHILL	3
S3 thru S14		Custom Switch Assy 12 x F type	SCHADOW	1
RV14/S1	4400-0792	Pot/Switch Combination	A-B Custom	1
RV15/RV16/S17	4400-0796	Dual Pot/Switch Combination	A-B Custom	1
RV9/RV10/RV11 RV12	4400-0795	Quad Pot Combination	A-B Custom	1
	4400-A625	Heatsink	AMBER	1
J1,2	609-2602-MR/	Connector 26 PIN	ANSLEY/3M	2
J3,4,5	4108-4AG	Connector 4 PIN Header	MOLEX	3
		8 PIN I.C. Socket	VARIOUS	25
		14 PIN I.C. Socket	VARIOUS	21
		16 PIN I.C. Socket	VARIOUS	16
	6-32 x 3/8 Pan Head	Screw	VARIOUS	3
	6-32	Hex Nut	VARIOUS	3
		Heat Sink Washer	VARIOUS	3
		Nylon Washer	VARIOUS	3
	4400-430-06	PCB	AMBER	1

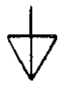
SCHEMATIC GENERAL NOTES

1. COMPONENT VALUES ARE AS FOLLOWS UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
   ALL DIODES ARE 1N4148

2. 

DC POWER SUPPLY VOLTAGE

3. 
GROUND

4. 
POWER AMPLIFIER OUTPUT GROUND

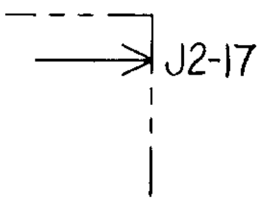
5. 

CONNECTED TO LOCATION ON SAME DRAWING SPECIFIED BY SCHEMATIC COORDINATES A5.

6. 

CONNECTED TO LOCATION ON SAME SUB-ASSEMBLY (i.e. RECEIVER, METER, GENERATOR) SPECIFIED BY SCHEMATIC COORDINATES A5 ON DRAWING 6.

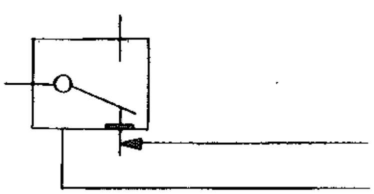
7. 
PRINTED CIRCUIT SUB-ASSEMBLY

8. 

MULTI PIN FLAT CABLE OR MOLEX CONNECTOR PIN OUT

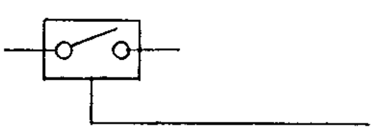
9. 

INTEGRATED CIRCUIT LOCATED AT ROW 6 COLUMN 4

10. 
<u>CMOS ANALOG SWITCH</u> (4053)

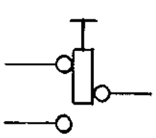
CONNECTION MADE WHEN CONTROL LINE IS HIGH.

CONTROL LINE

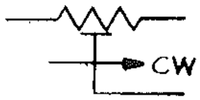
11. 
<u>CMOS ANALOG SWITCH</u> (4066)

SWITCH CLOSED WHEN CONTROL LINE IS HIGH.

CONTROL LINE

12. 
<u>PUSH BUTTON SWITCH</u>

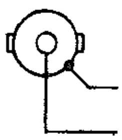
SHOWN IN "OUT" POSITION

13. 

SCREWDRIVER ADJUST TRIM CONTROL

14. 

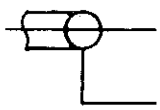
FRONT PANEL POTENTIOMETER

15. 

BNC CONNECTOR

SHIELD CONNECTION

CENTER CONNECTION

16. 

SHIELDED CABLE

CENTER CONNECTION

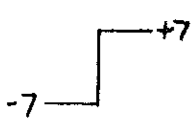
SHIELD CONNECTION

17. FILTER TYPES

LOW PASS FILTER

BAND PASS FILTER

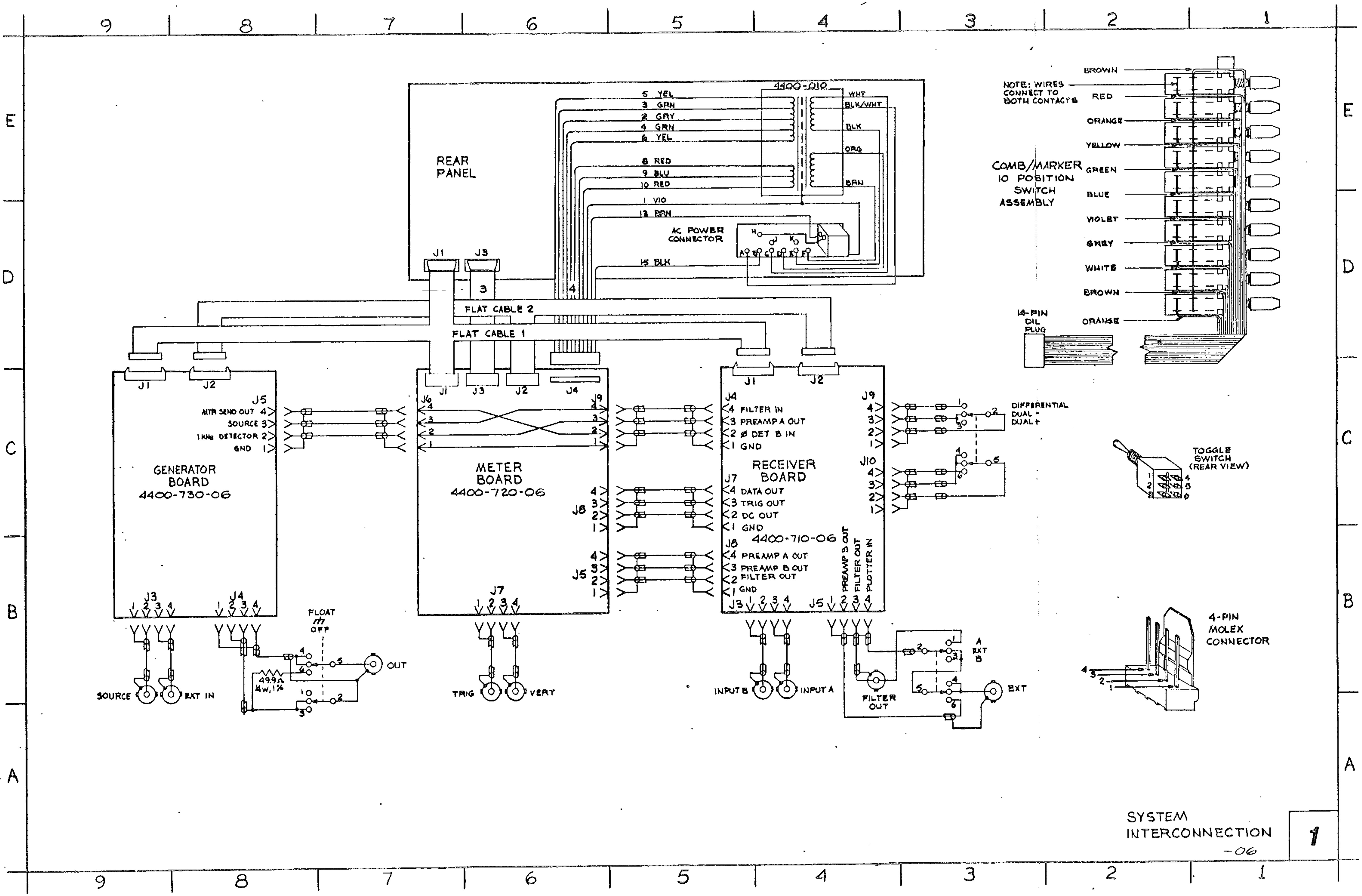
HIGH PASS FILTER

18. 

CONTROL LINE VOLTAGE LEVELS

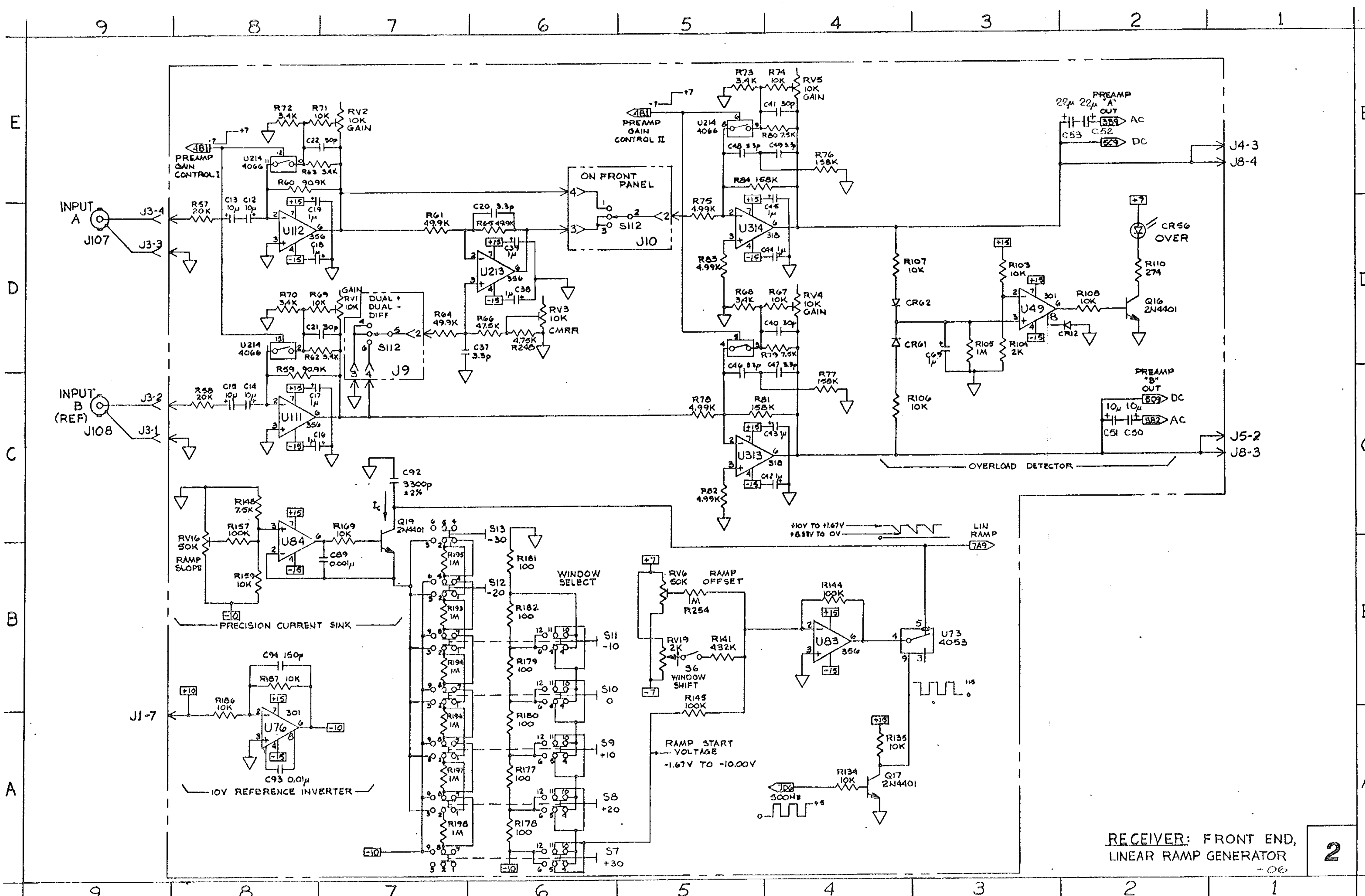
19. LEVEL AND GAIN NOTATION

(+13dB) / (-17dB)	HIGHEST GAIN OR LOSS / LOWEST GAIN OR LOSS
+7 V / +220mV	HIGHEST VOLTAGE LEVEL / LOWEST VOLTAGE LEVEL
+20 dBm / -40 dBm	HIGHEST ABSOLUTE LEVEL / LOWEST ABSOLUTE LEVEL



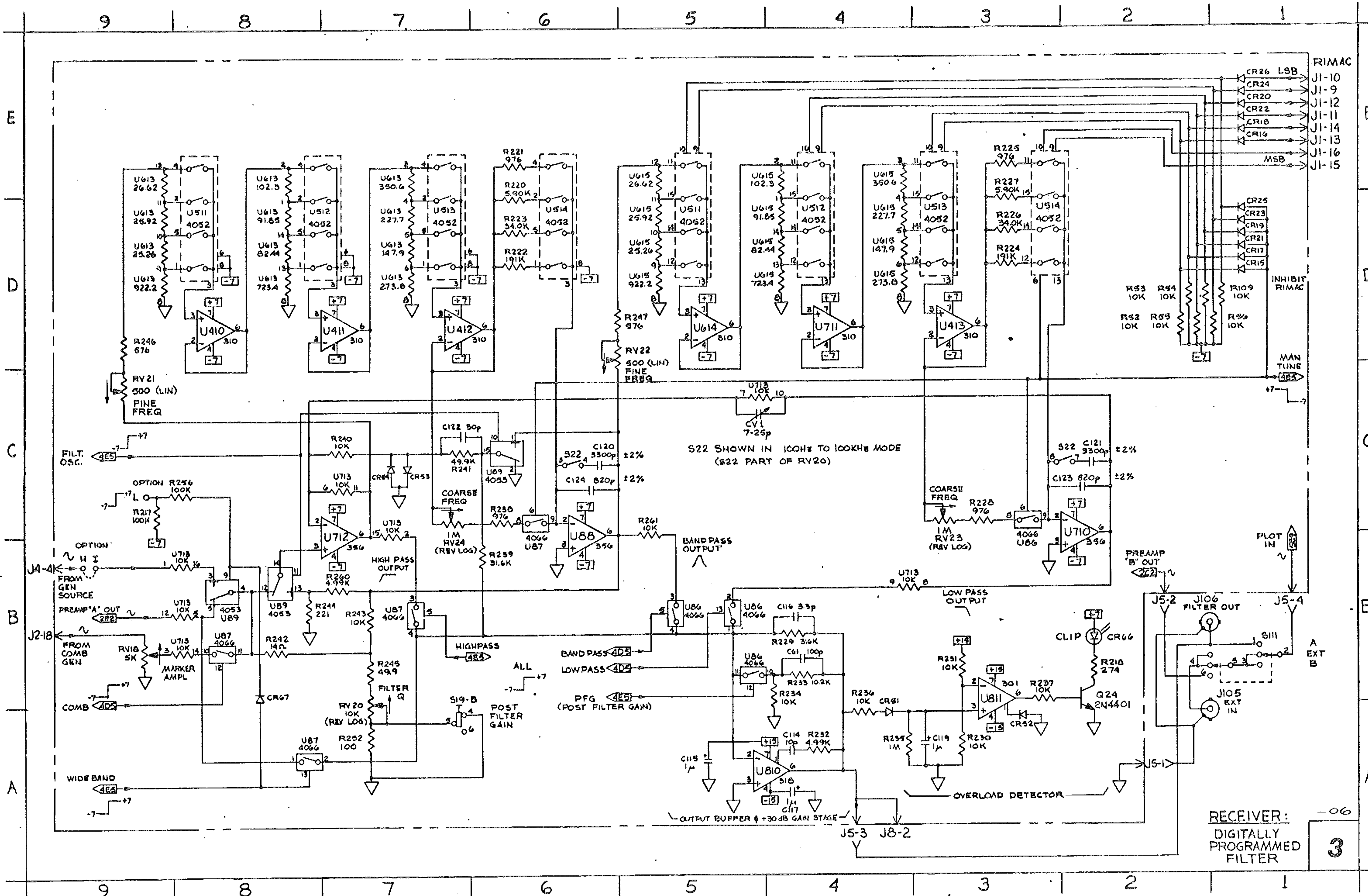
SYSTEM INTERCONNECTION -06

1



RECEIVER: FRONT END, LINEAR RAMP GENERATOR

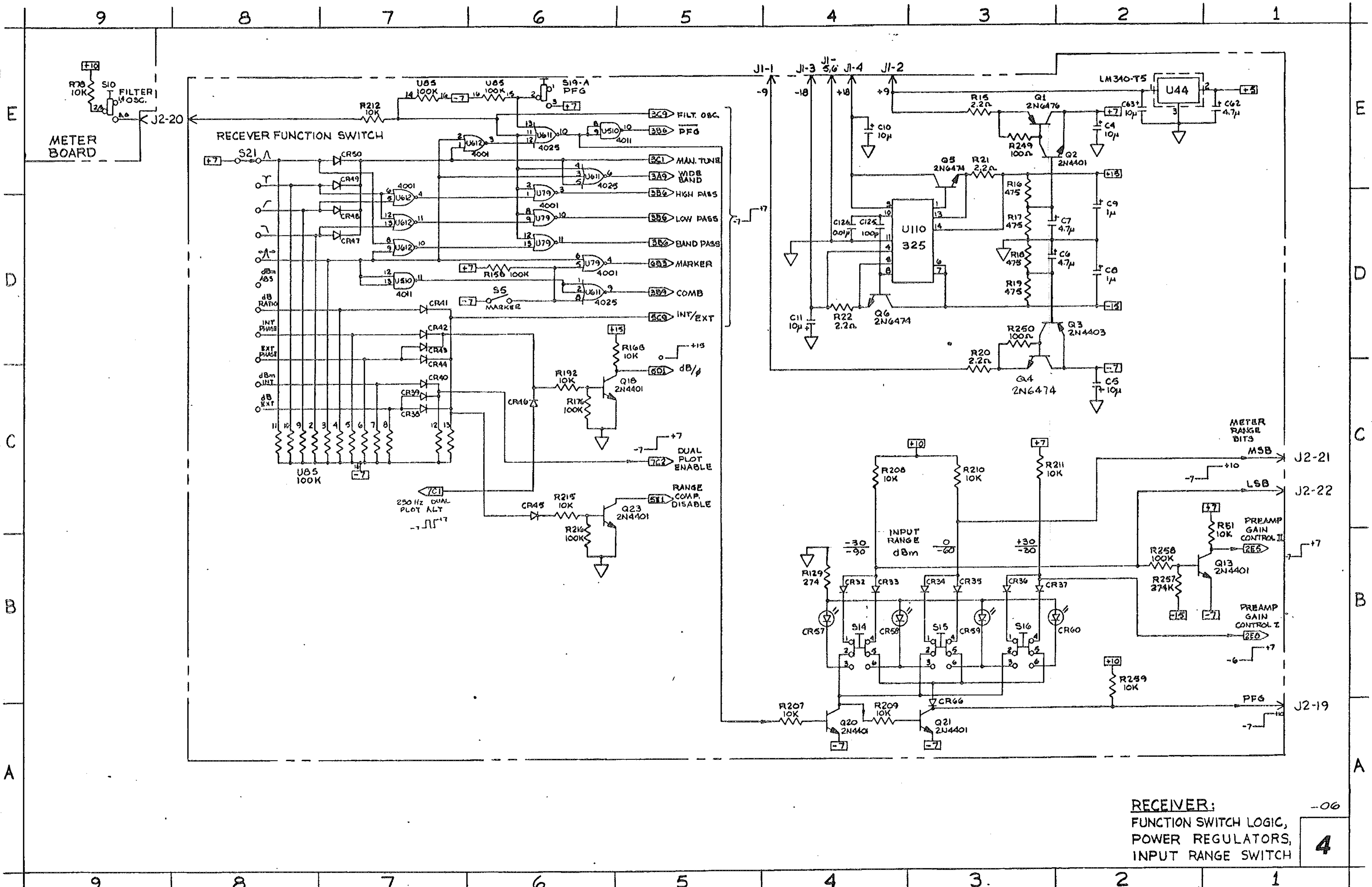
2



RECEIVER:
DIGITALLY PROGRAMMED FILTER

-06

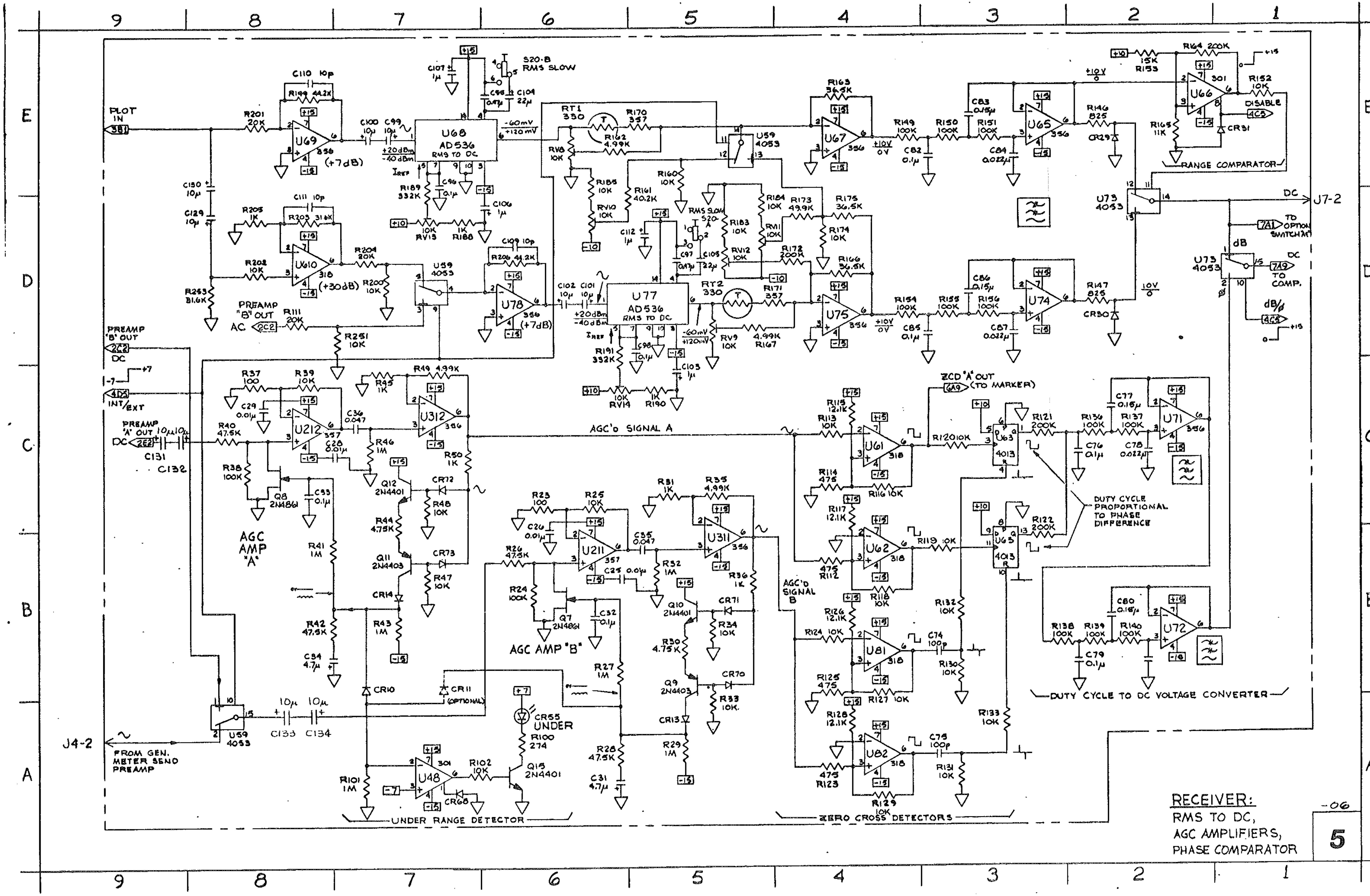
3



RECEIVER:
FUNCTION SWITCH LOGIC,
POWER REGULATORS,
INPUT RANGE SWITCH

-06

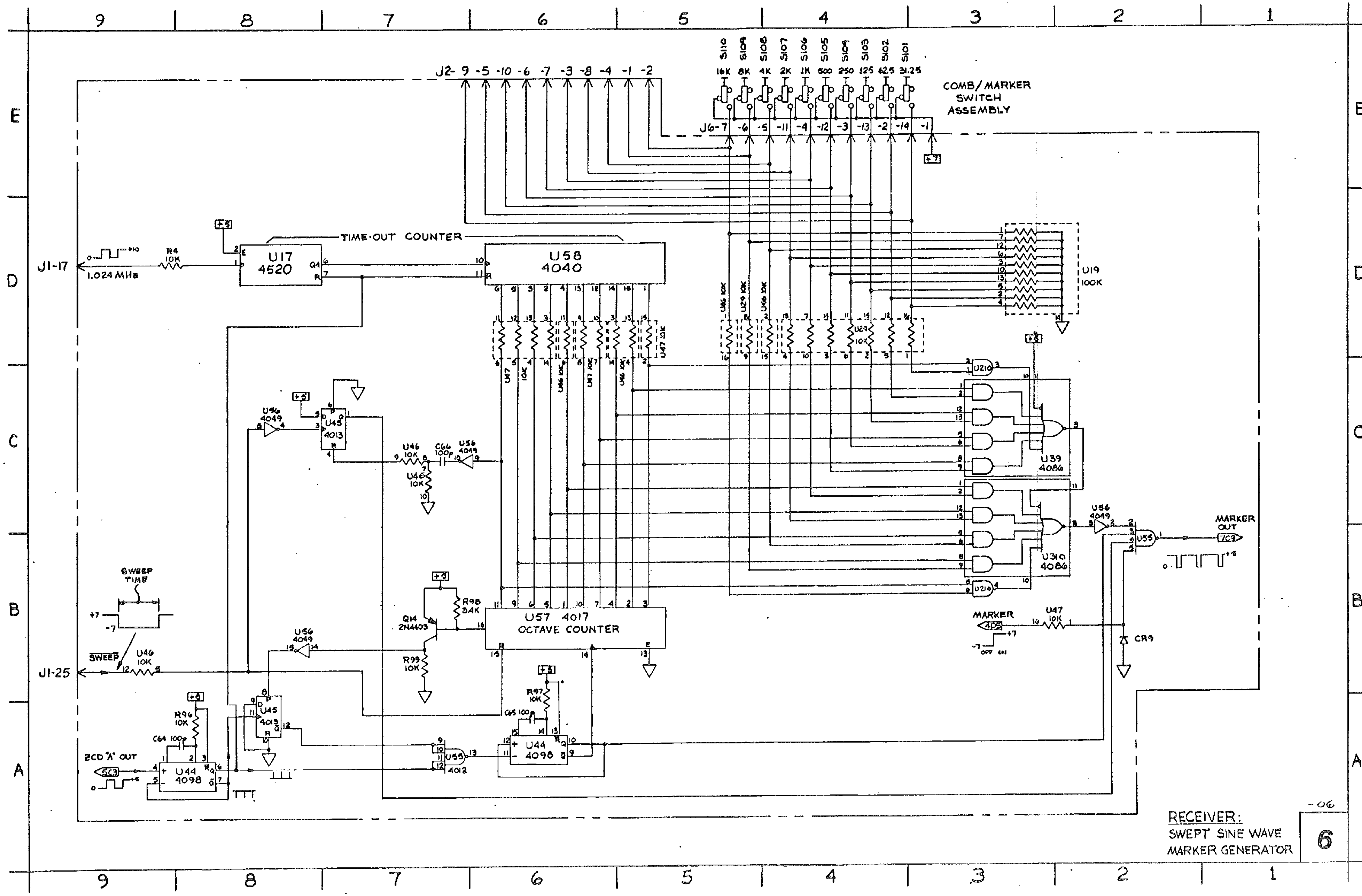
4



RECEIVER:
RMS TO DC,
AGC AMPLIFIERS,
PHASE COMPARATOR

-06

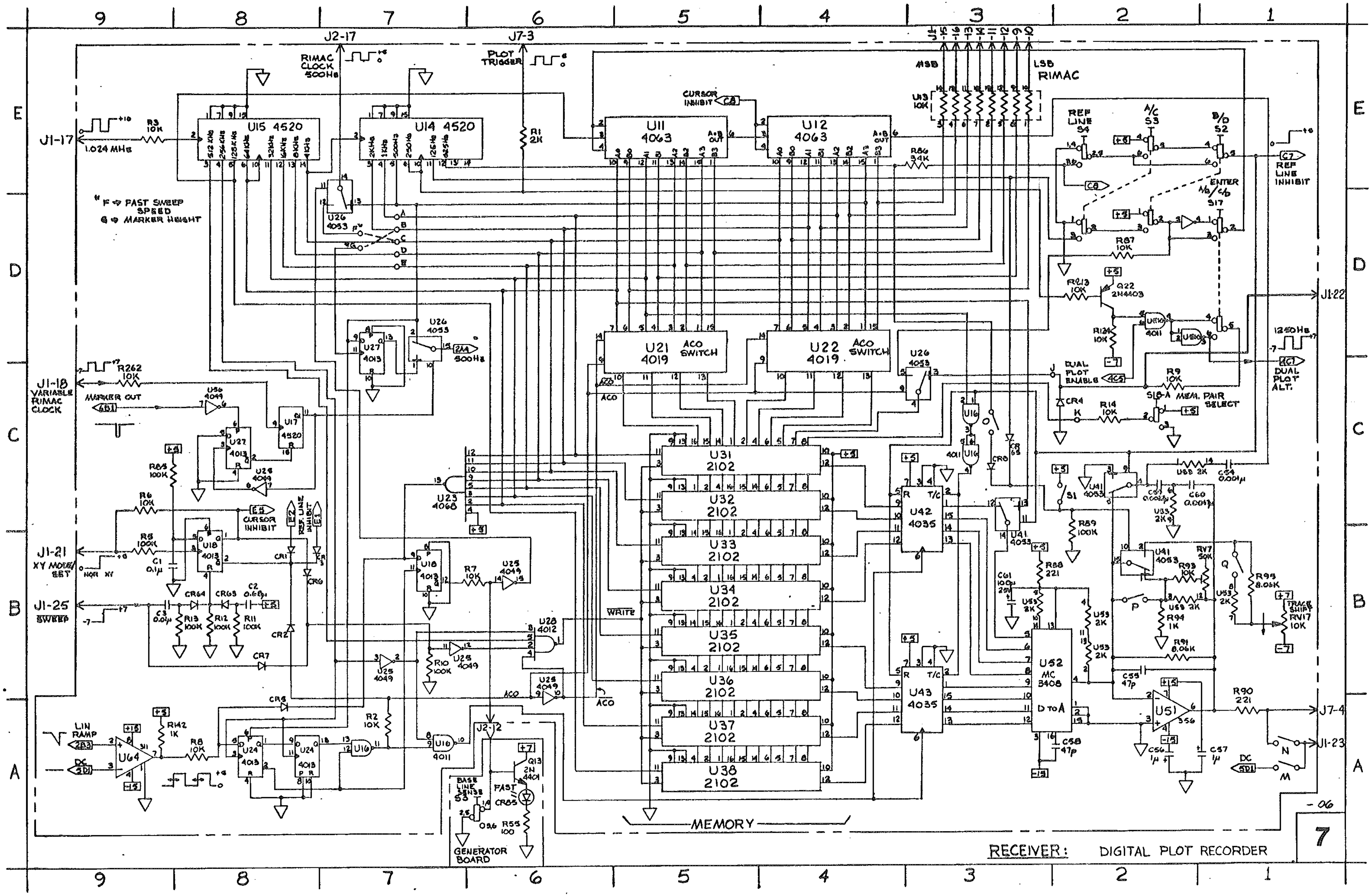
5



RECEIVER:
SWEPT SINE WAVE
MARKER GENERATOR

-06

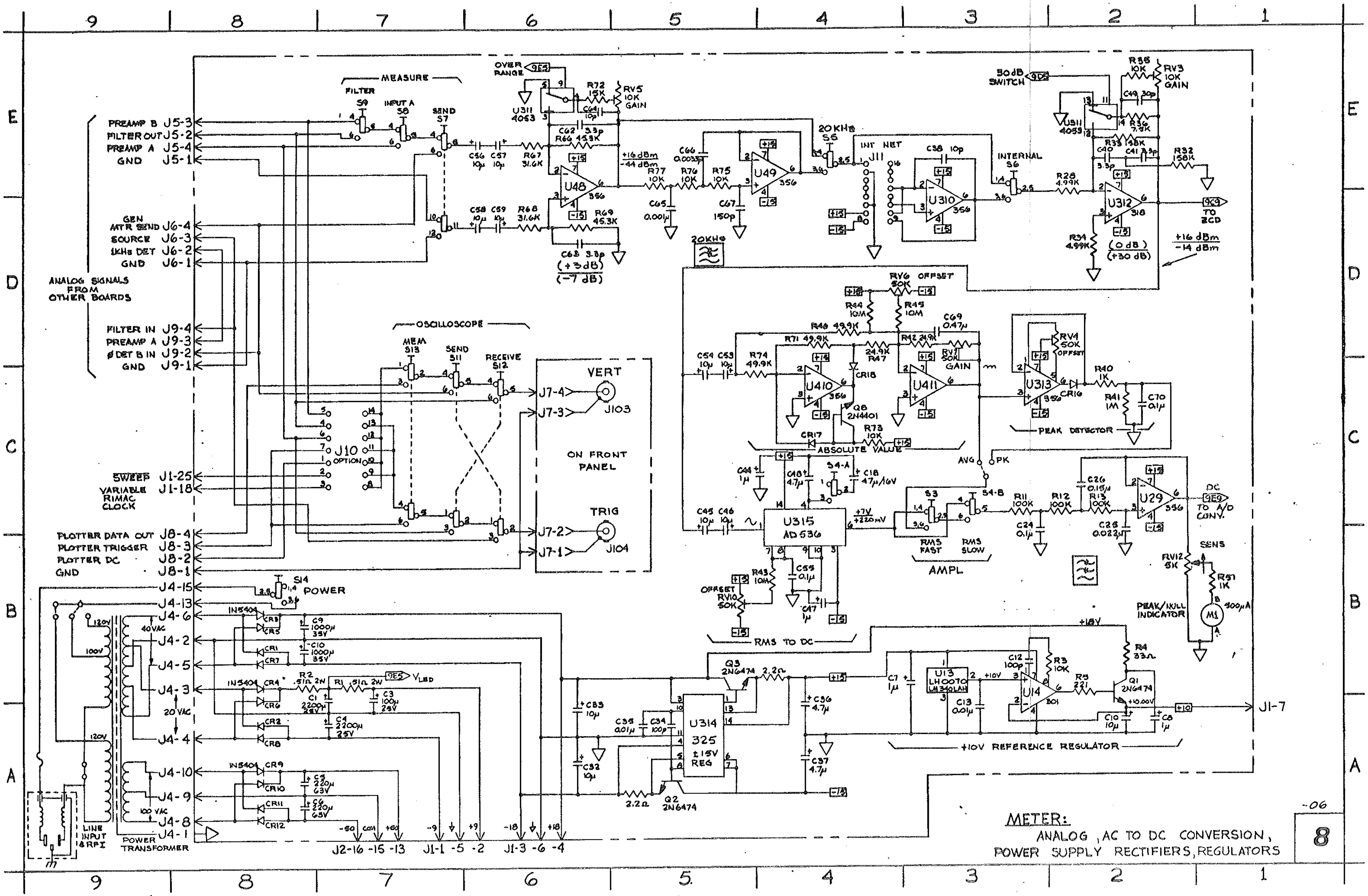
6



-06

7

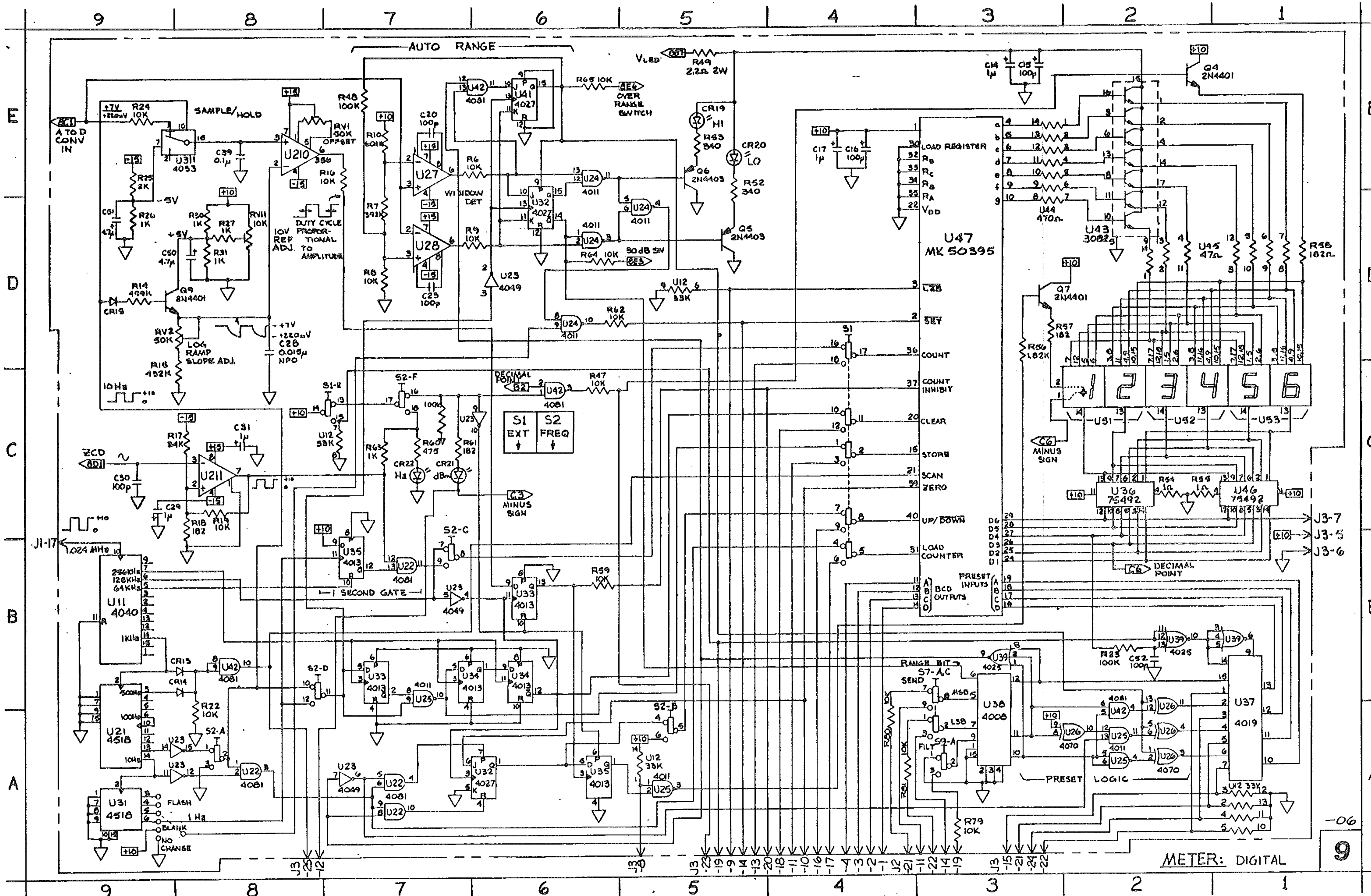
RECEIVER: DIGITAL PLOT RECORDER



METER:
ANALOG, AC TO DC CONVERSION,
POWER SUPPLY RECTIFIERS, REGULATORS

-06

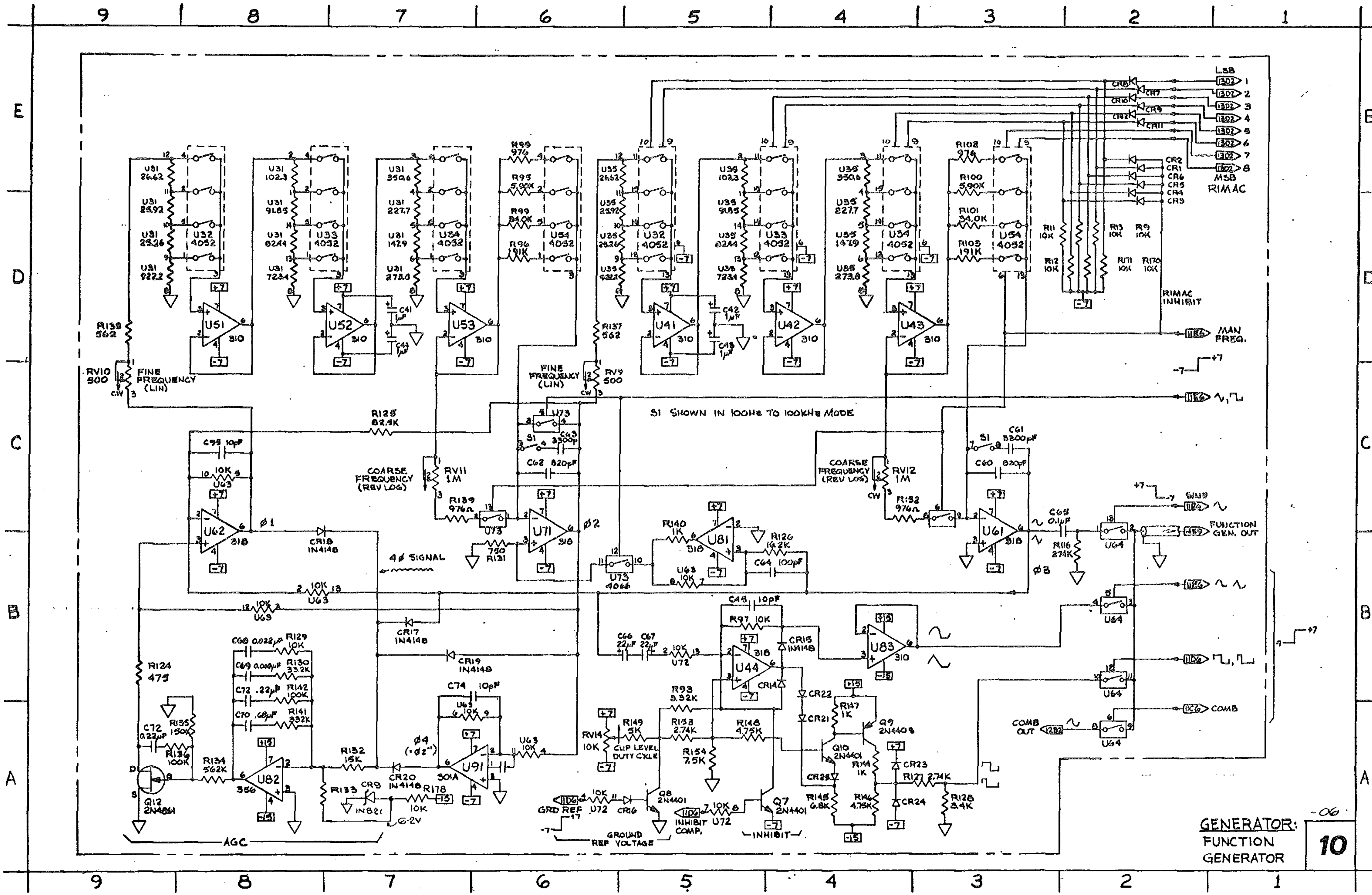
8



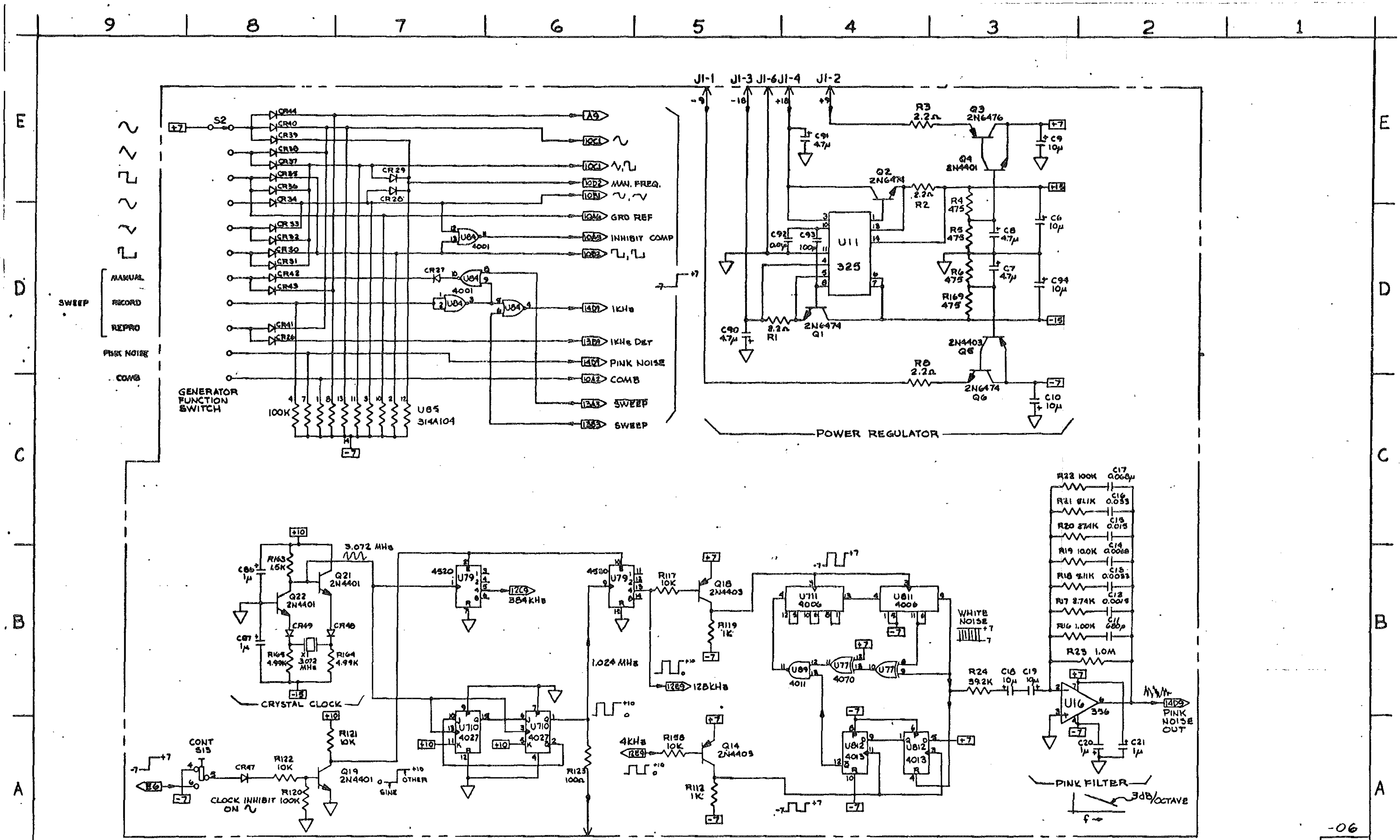
METER: DIGITAL

-06

9

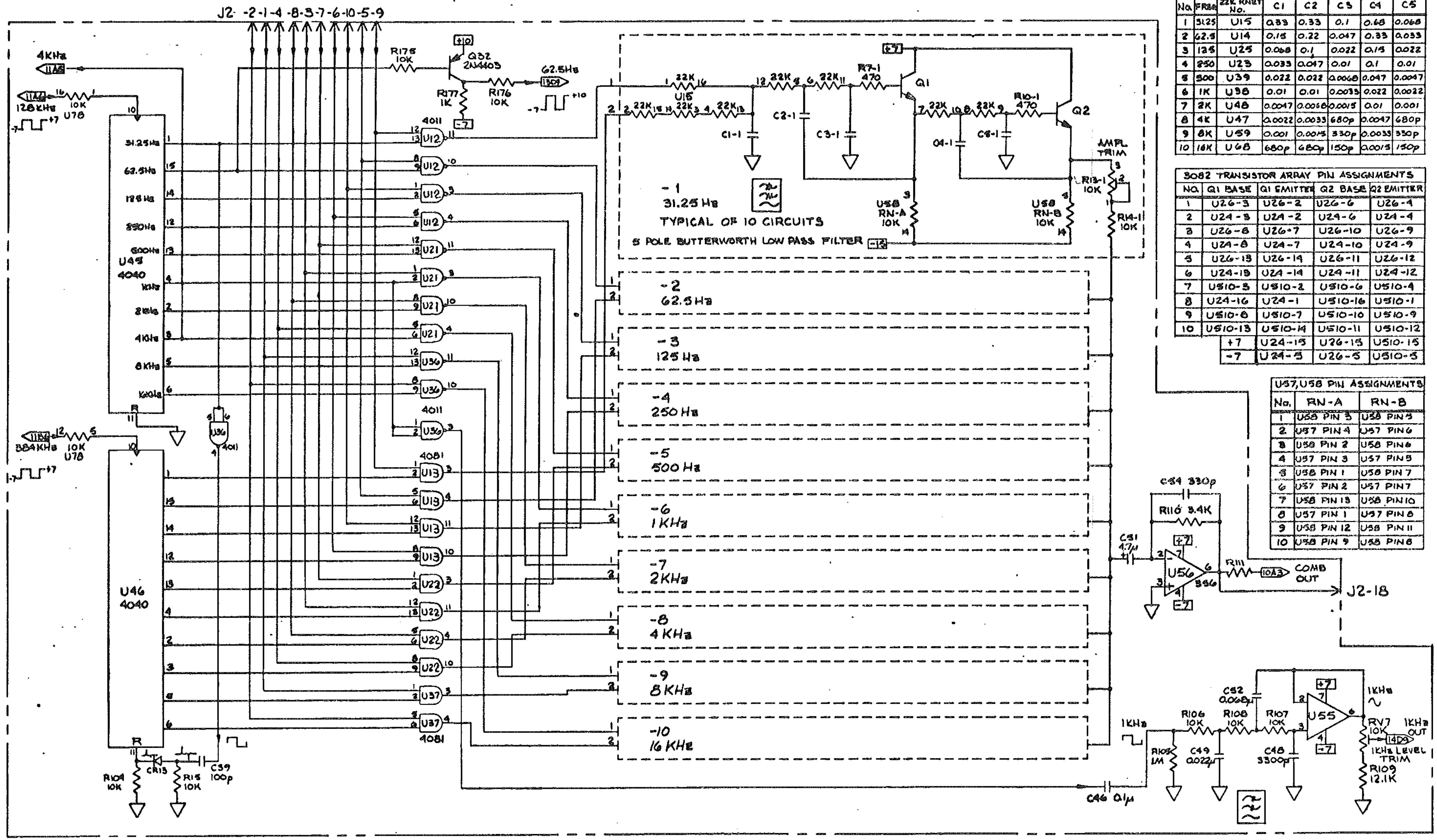


GENERATOR: FUNCTION GENERATOR
10



-06

GENERATOR: FUNCTION SWITCH, POWER REGULATOR
MASTER CRYSTAL CLOCK, PSEUDO RANDOM NOISE GENERATOR



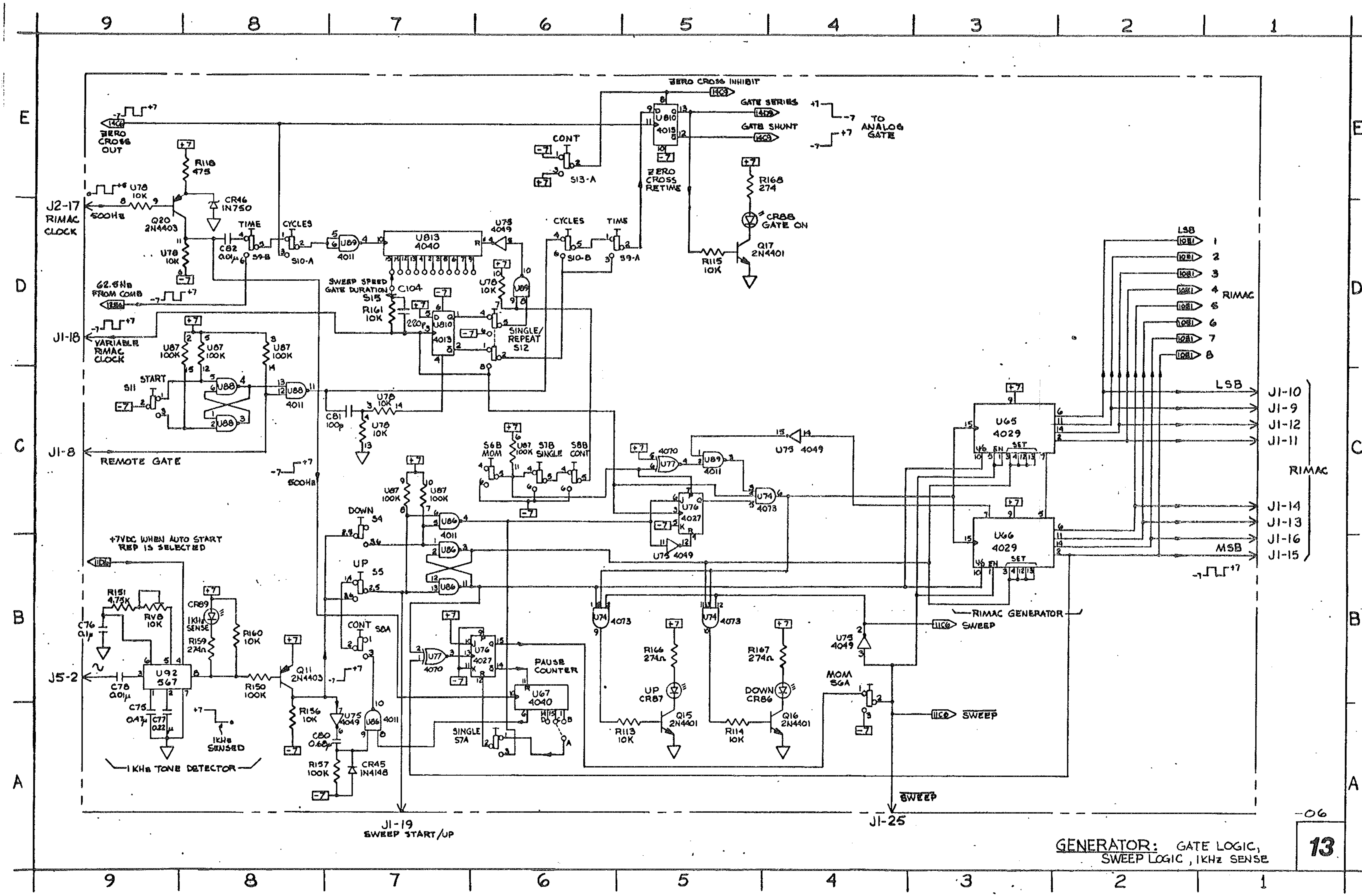
COMPONENT TABLE FOR LOW PASS FILTERS							
No.	FREQ	22K RNET No.	C1	C2	C3	C4	C5
1	31.25	U15	0.33	0.33	0.1	0.68	0.068
2	62.5	U14	0.15	0.22	0.047	0.33	0.033
3	125	U25	0.068	0.1	0.022	0.15	0.022
4	250	U23	0.033	0.047	0.01	0.1	0.01
5	500	U39	0.022	0.022	0.0068	0.047	0.0047
6	1K	U38	0.01	0.01	0.0035	0.022	0.0022
7	2K	U48	0.0047	0.0068	0.0015	0.01	0.001
8	4K	U47	0.0022	0.0033	680p	0.0047	680p
9	8K	U59	0.001	0.0015	330p	0.0033	330p
10	16K	U68	680p	680p	150p	0.0015	150p

3082 TRANSISTOR ARRAY PIN ASSIGNMENTS				
NO.	Q1 BASE	Q1 EMITTER	Q2 BASE	Q2 EMITTER
1	U26-3	U26-2	U26-6	U26-4
2	U24-3	U24-2	U24-6	U24-4
3	U26-8	U26-7	U26-10	U26-9
4	U24-8	U24-7	U24-10	U24-9
5	U26-13	U26-14	U26-11	U26-12
6	U24-13	U24-14	U24-11	U24-12
7	U510-3	U510-2	U510-6	U510-4
8	U24-16	U24-1	U510-16	U510-1
9	U510-8	U510-7	U510-10	U510-9
10	U510-13	U510-14	U510-11	U510-12
	+7	U24-15	U26-15	U510-15
	-7	U24-5	U26-5	U510-5

U57,U58 PIN ASSIGNMENTS		
No.	RN-A	RN-B
1	U58 PIN 3	U58 PIN 5
2	U57 PIN 4	U57 PIN 6
3	U58 PIN 2	U58 PIN 6
4	U57 PIN 3	U57 PIN 5
5	U58 PIN 1	U58 PIN 7
6	U57 PIN 2	U57 PIN 7
7	U58 PIN 13	U58 PIN 10
8	U57 PIN 1	U57 PIN 8
9	U58 PIN 12	U58 PIN 11
10	U58 PIN 9	U58 PIN 8

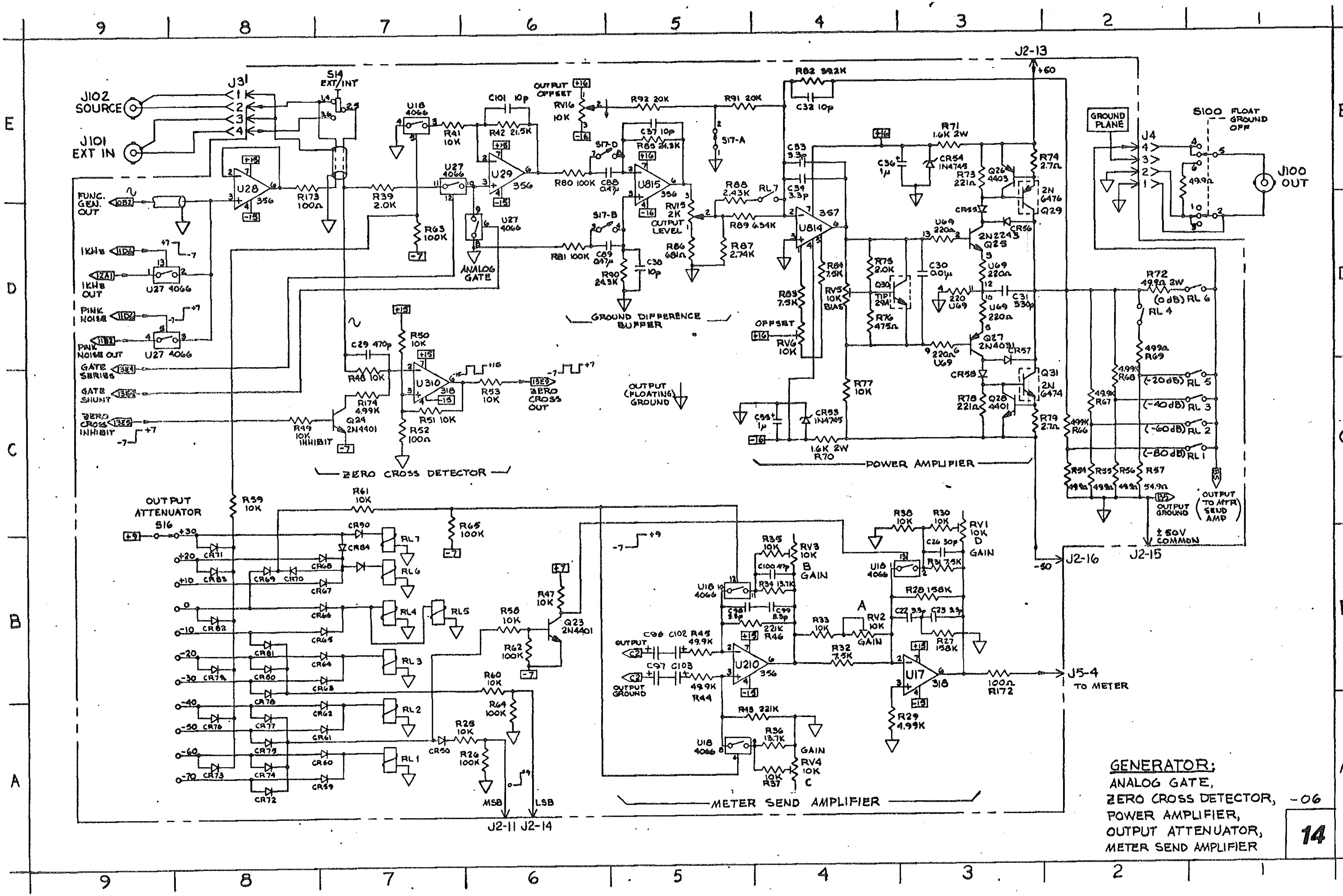
-06

GENERATOR:
COMB GENERATOR



GENERATOR: GATE LOGIC, SWEEP LOGIC, 1KHz SENSE

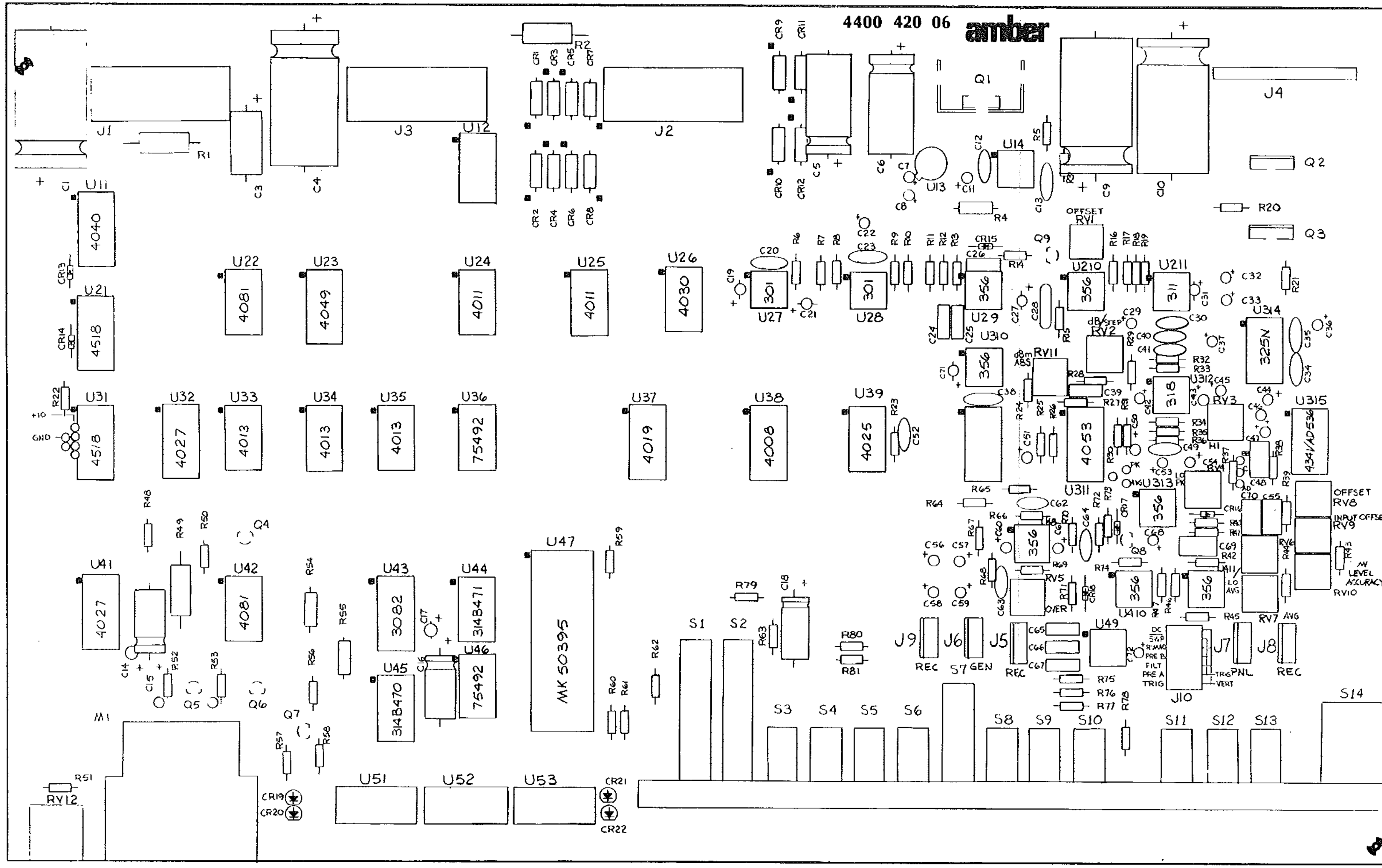
-06



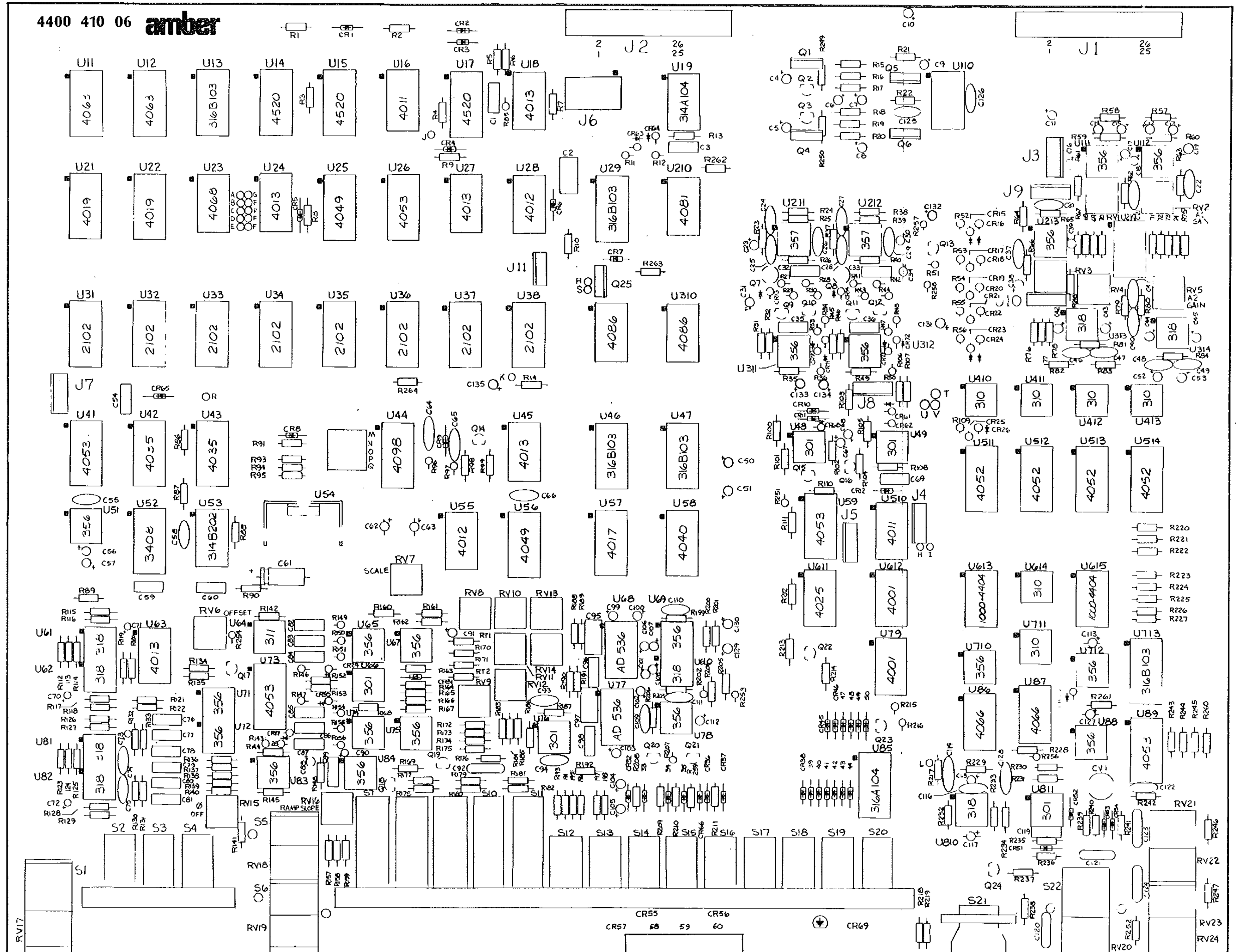
GENERATOR:
ANALOG GATE,
ZERO CROSS DETECTOR,
POWER AMPLIFIER,
OUTPUT ATTENUATOR,
METER SEND AMPLIFIER

-06

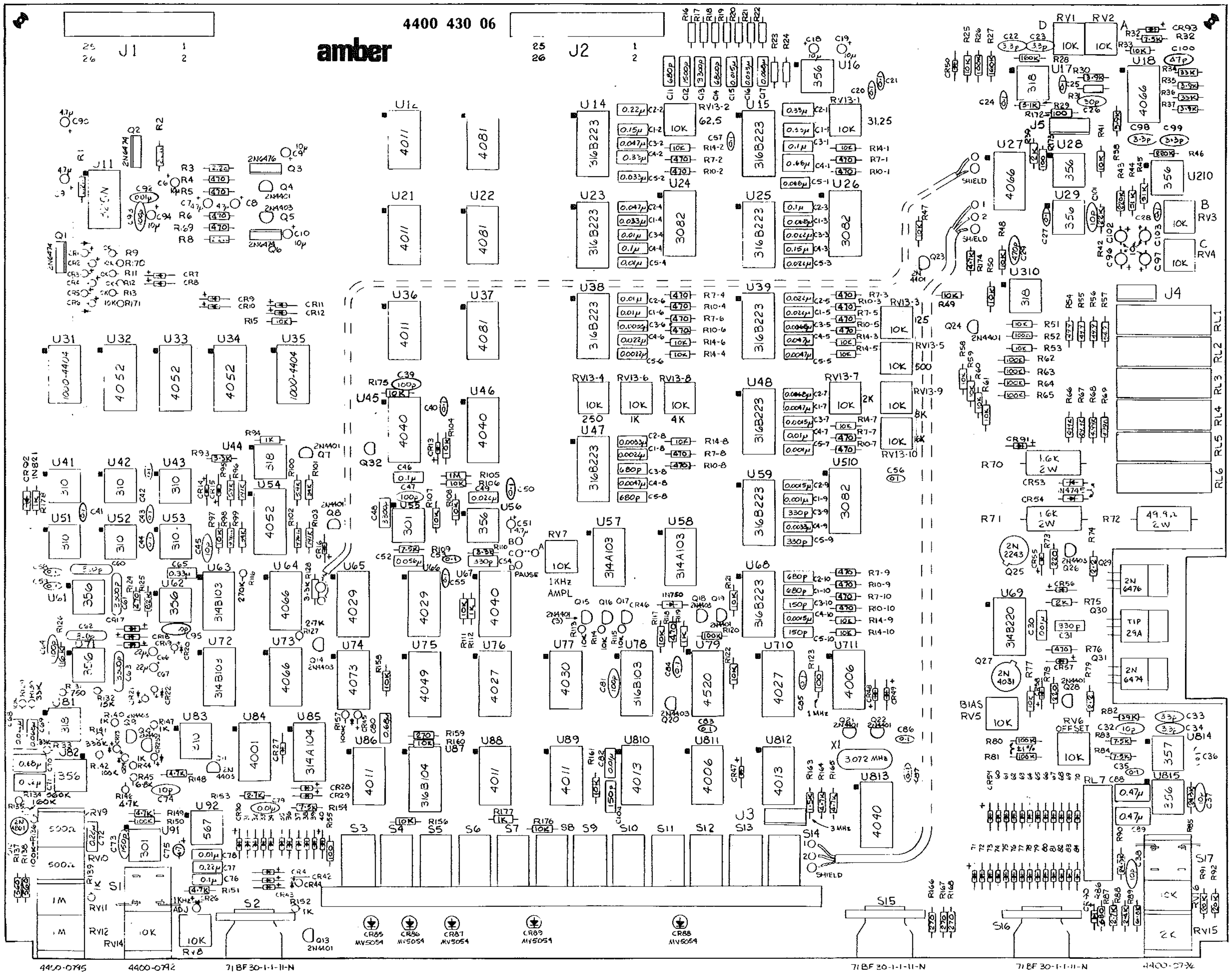
14



4400-720-06 METER BOARD



4400-710-06 RECEIVER BOARD



4400-730-06 GENERATOR BOARD