potential DSP uses 12.288 MHz clock
div 32 gives 384kHz PWM clock
oscilator freq should be set +20% to +30%, Set to 480kHz
R1 = , c1 = c2 = 2.2nF, R1 = 186 ohms, Rfb = 68k

Each output pin has a nominal common-mode dc level of 1.5 V
and swings ±1.27 V for a 0 dBFS digital input signal.

Therefore we want a gain of 26 to achive clipping with 64V supply

Syncronise devices with extenal clock - AD modulation so rember to invert - side of bridge

On Carrier board:
1) input capacitors
2) opto isolated switch for CSD shorting
3) external clock
4) SMPS for +12V from VBUS
5) supply rail shorting diodes at output
6) output filter
7) Bulk decoupling

Single supply clocked bridged IR4301 alu board (thermal substrate)

2k4 bias resistors for floating supply
Vbus = 30V = 4mA
Vbus = 80V = 12mA

VBUS
R12 2k4, 5%, 500mW
D3 LED Red
VAA
C12 10V, X5R, 20%
Connect floating grounds of bridged chips together (avoids DC offset)
GNDA
C13 10V, X5R, 20%
VAA = floating analog input supply
Zenner clamped aprox 10V (VAA-VSS)
VSS
D4 LED Green
R13 2k4, 5%, 500mW
GND

EXT_CLK
384kHz, 5V clock signal to sync amplifiers
R1 22k, 1%, 63mW
C1 100pF, 100V, CG0
SPK_OUT
R5 68k, 0.1%, 100V, 125mW
IN-
R2 2k61, 0.1%, 100mW
Audio-
C2 2n2, 50V, X7R, 5%
C4 2n2, 50V, X7R, 5%
COMP
R6 180R, 1%, 63mW
C5 1nF, 50V, C0G, 5%
GNDA

R3 2k61, 0.1%, 100mW
Audio+
R4 68k, 0.1%, 100V, 125mW
GNDA
IN+
2n2, 50V, X7R, 5%
C3
Improves HF THD
R7 180R, 1%, 63mW
GNDA

VBUS
D1 1N4148WQ-7-F
+12V
R10 4R7, 5%, 125mW
D2 1N4148WQ-7-F
VBUS
R11 33k, 1%, 125mW
Precharge resistor (stops pops)
C10 22uF, 16V, X5R, 20%
SPK_OUT

U1 IR4301
VAA 1
GNDA 2
IN- 4
IN+ 3
COMP 5
VSS 7
CSD 6
CSH 14
VB 13
VP 12
VCC 8
VS 11
VIN 10
COM 9
R8 4R7, 5%, 125mW
+12V
SPK_OUT
C7 10uF, 25V, X5R, 20%
GND

Short CSD with opto switch to disable amp
Turn on @ aprox 6.7V = 0.67s
Charge/Discharge = 100uA
C6 10uF, 25V, X5R, 20%
VSS

Connection info:
VBUS => 30V - 80V (recomended max 68V),
Estimated supply current requriment Pout = 578W (bridged 4 ohm),
I=6A (per chip), 12A (bridge channel).
Assuming 6dB crest factor 3A required per bridge channel.

12V => assume around 15mA current

SPK_OUT => speaker output (connect filter)

CSD => Pull to VSS to disable chip

VSS => negative analog supply voltage

Audio+/Audio-=> diffirential audio input (ac couple)

EXT_CLK=>5Vpp 384kHz clock signal

AGND => common analog ground to connect between ICs

GND => 0V power rail

VBUS
DC bus decoupling
C8 100nF, 100V, X7R, 10%
C9 100nF, 100V, X7R, 10%
C11 100nF, 100V, X7R, 10%
R9 1R, 1%, 125mW
GND

VBUS
K23 EDGE_PAD_1mm
K24 EDGE_PAD_1mm
K25 EDGE_PAD_1mm
K26 EDGE_PAD_1mm
K27 EDGE_PAD_1mm

K28 EDGE_PAD_1mm
K29 EDGE_PAD_1mm
GNDA

H1 M3
H2 M3
H3 M3
H4 M3
Mounting holes
Remember to include in carrier

solder connection points for module
K18 EDGE_PAD_1mm
K21 EDGE_PAD_1mm
K22 EDGE_PAD_1mm
K19 EDGE_PAD_1mm
SPK_OUT
K20 EDGE_PAD_1mm
K15 EDGE_PAD_1mm
K16 EDGE_PAD_1mm
K17 EDGE_PAD_1mm
K12 EDGE_PAD_1mm
K13 EDGE_PAD_1mm
K14 EDGE_PAD_1mm
GND
VBUS

K1 EDGE_PAD_1mm
EXT_CLK
K2 EDGE_PAD_1mm
VSS
K3 EDGE_PAD_1mm
CSD
K4 EDGE_PAD_1mm
+12V
SPK_OUT
Audio-
Audio+
K11 EDGE_PAD_1mm
VBUS
GND
GNDA

Produce on single sided Alu board

VBus abs max = 80V, minimum = 30V, recomended 80V

James Lawson

Sheet: /
File: Aluboard.sch

Title: Aluboard for IR4301

Size: A3	Date: 2020-12-30	**Rev: 1**
KiCad E.D.A. kicad (5.1.9)-1		Id: 1/1