An Alternative Feedback Network for the Single Ended F5

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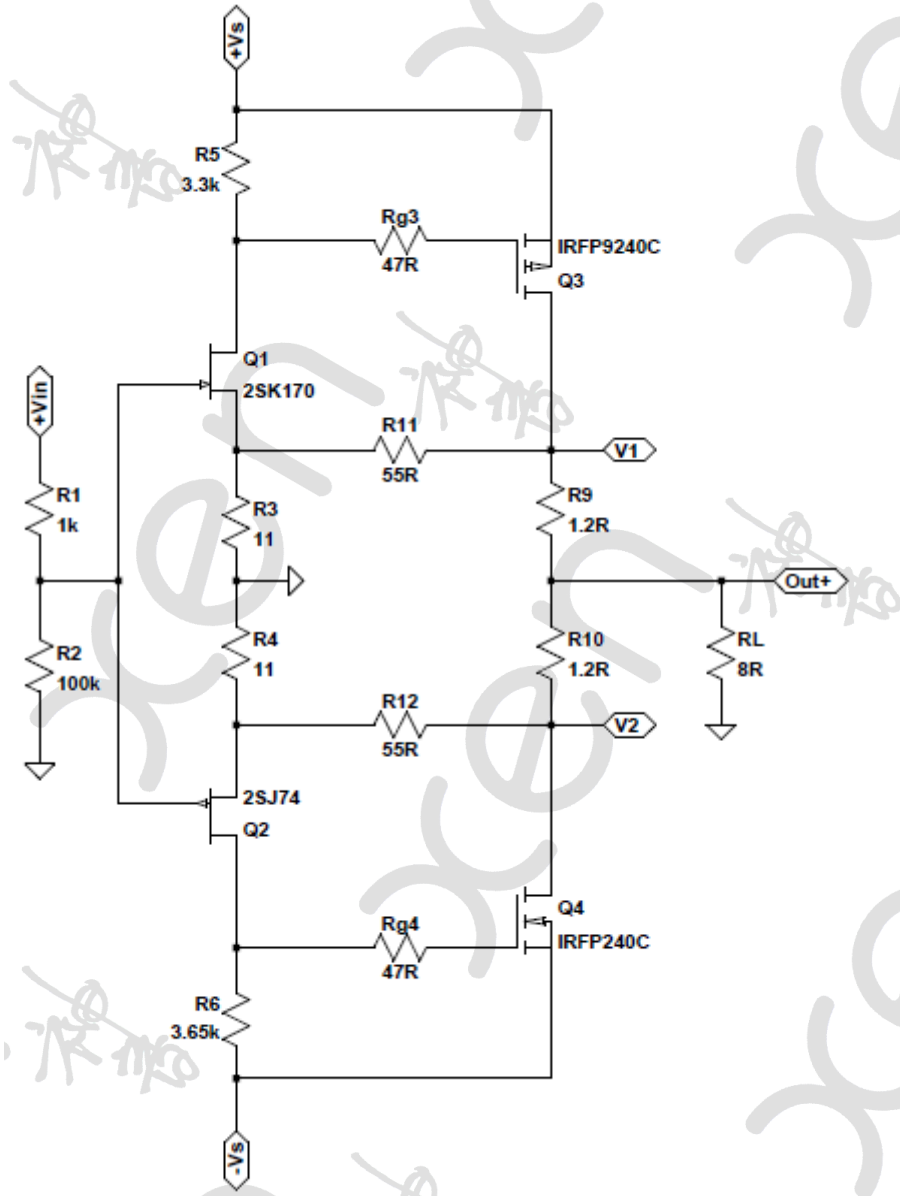
Earlier, Lynn Quam posted an alternative feedback circuit for the standard F5 power amplifier [1], which I thought was really clever. But he asserted that all he wanted was to achieve bias stabilisation, so that he could get rid of the MOSFET source resistors.

Let's see if that goal is achievable first. We all know that Spice is not 100% reality. It does give you a lot of information and is a very useful tool, for investigations of this type.



We set up a Spice model of his circuit and just look at DC operating point first. After setting the MOSFET bias to about 1.27A, we deliberately add an additional current of 100mA in parallel across Q3, to simulate the MOSFET heating up with a positive tempco. In the original circuit, without the Quam resistors (R9,10) one can see that the bias of Q4 will increase by 50mA, and the DC offset goes up by 11mV. With the Quam circuit, both DC offset and bias remains largely unchanged. So it works as intended. Good news.

How does it actually work, in DC ?

R9,10 sense the respective drain current of Q3,4, and fed that back to the front end via the NFB network. An increase in bias current of Q3, for example, will lift the DC voltage at the Source of Q1, and hence reduce its current. This, in turn, reduces the voltage across the drain resistor R5, which then reduces the bias of Q3. It therefore forms a feedback loop to regulated the bias current. The degree of regulation depends of course on this loop gain. The higher the value of R9, the better the bias stability.

So why not use a much larger value for R9,10 ? Well, R9,10 to the output is outside the feedback loop of the amplifier. A large value for them will not only increase the output impedance, but also reduce gain, as seen by the external load RL.

In addition to that, R9,10 also have other effects. Since we are talking about a Class A amplifier, there is a constant bias of say >1A. Even with no signal, the constant bias will generate a DC voltage at the source of the input JFETs (Q1,2), resulting in significant reduction in bias of the front end. The drain resistors will have to be increased to compensate for that, and the balance of the gain structure between first and second stage will change as a result. It does not have to be a bad thing, as loop gain is likely to increase as a whole.

So Lynn should be happy that he gets his bias control without source resistor.

How about in AC ?

Those sensing resistor not only work in DC, but also in AC. One can argue that they can be each paralleled with a 22,000 µF electrolytics to let AC through. But if we don't, as shown in his circuit, then they also have an impact on the AC performance of the amplifier.

As already mentioned, the inclusion of R9,10 changes the frontend bias as well as the overall loop gain. This of course applies equally to AC and DC. But what else happens in the presence of an AC signal ?

Let's assume that the top and the bottom halves of the F5 is completely symmetrical, i.e. the "push" current of one half is exactly equal and opposite to the "pull" current of the other half. Or, the amplifier has no even harmonic distortion into a perfectly linear load impedance. In that case, the total voltage across R9,10 will remain constant, but swings relative to Gnd with the output voltage. They behave as if they do not exist for AC feedback, other than the above-mentioned DC shift for the front end and the increased effective RL. If, however, the two halves are not perfectly symmetrical, and there is some even order harmonics, then the voltage across R9,10 will not remain constant, as can be seen in the simulation. This variation is actually a measure of those distortions, which are now being fed back to the frontend through the normal NFB network. And as you can see, when compared with the standard F5, the second harmonics is being reduced by some 6dB. Not bad for just 2 extra resistors.

Simulated FFT for Standard F5, 1kHz 1W into 8R

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	4.078e+00	1.000e+00	-0.03°	0.00°
2	2.000e+03	7.232e-05	1.773e-05	63.87°	63.90°
3	3.000e+03	2.946e-05	7.223e-06	23.51°	23.54°

4	4.000e+03	1.248e-06	3.061e-07	-94.55°	-94.52°
5	5.000e+03	1.239e-06	3.039e-07	-76.42°	-76.39°
6	6.000e+03	1.116e-06	2.737e-07	-65.96°	-65.93°
7	7.000e+03	1.106e-06	2.711e-07	-61.56°	-61.53°
8	8.000e+03	1.118e-06	2.742e-07	-59.40°	-59.37°
9	9.000e+03	1.158e-06	2.839e-07	-55.46°	-55.43°

Total Harmonic Distortion: 0.001916%(0.015579%)

Simulated FFT for F5 LQ, 1kHz 1W into 8R

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	4.072e+00	1.000e+00	-0.04°	0.00°
2	2.000e+03	3.578e-05	8.786e-06	18.25°	18.29°
3	3.000e+03	2.628e-05	6.453e-06	53.73°	53.77°
4	4.000e+03	1.149e-06	2.823e-07	-104.07°	-104.03°
5	5.000e+03	1.407e-06	3.455e-07	-78.71°	-78.67°
6	6.000e+03	1.117e-06	2.742e-07	-65.58°	-65.54°
7	7.000e+03	1.106e-06	2.715e-07	-61.79°	-61.75°
8	8.000e+03	1.148e-06	2.820e-07	-58.43°	-58.40°
9	9.000e+03	1.174e-06	2.882e-07	-56.13°	-56.09°

Total Harmonic Distortion: 0.001092%(0.015499%)

Why does it not cancel the second harmonics by some 20dB, like in a F5X ? The value of R9,10 in parallel is only a fraction of the load impedance. So the distortion sensing is already attenuated by that ratio. On top of that, the reduced bias of the frontend will also lower its transconductance and hence increase the first stage distortion. There is a sweet spot somewhere, which is, unfortunately, load dependent.

Whether you like to keep those H2 deliberately as sweetener is a fully separate discussion.

Reference

1. https://www.diyaudio.com/forums/pass-labs/376445-update-pas-f5-post6797286.html