AKD4413-SA

AK4413 Sound Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD4413-SA is an evaluation board for AK4413, 24bit 4ch DAC, supporting DVD-Audio. The AKD4413-SA has digital audio interfaces, enabling to interface to digital audio systems via optical or coaxial connector.

■ Ordering Guide

AKD4413-SA	---	AK4413 Evaluation Board (Control software is attached)

FUNCTION

- **Three digital audio interfaces**
  - **Coaxial Input**
  - **Optical Input**
  - **10pin Header for serial control mode**
- **USB control port**
- **On-board Analog output buffer circuit**

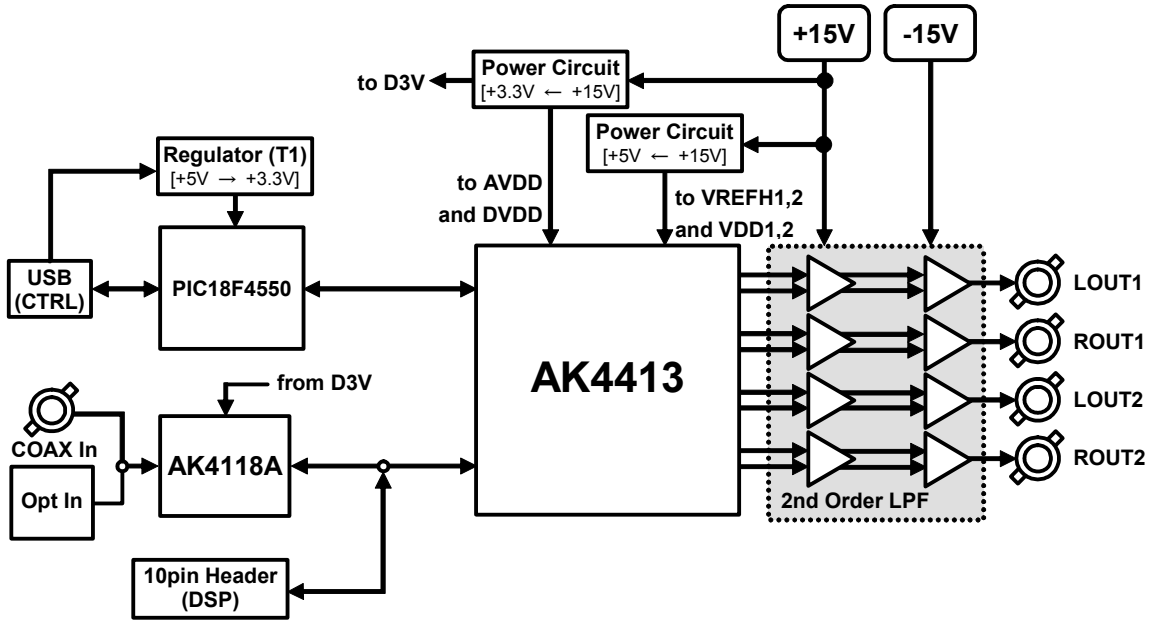


Figure 1. AKD4413-SA Block Diagram (Note 1)

Note 1. Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation Sequence

1) Setup the power supply lines.

2) Setup the evaluation mode.

2-1) Evaluation of D/A using AK4118A (DIR) (Coaxial connector) <default>
2-2) Evaluation of D/A using AK4118A (DIR) (Optical connector)
2-3) All interface signals including master clock are fed externally (PORT2)

3) Jumper pins and Switch setting. (See the followings.)

3-1) Jumper pin setting
3-2) DIP switch setting

4) Power on.

1) Setup the power supply lines.

Name	Color	Voltage	Breakdown	Note
+15V	Red	+12~+15V	Regulator Input/Output Buffer (OP Amp.)	Must be connected.
-15V	Blue	-12~-15V	Input/Output Buffer (OP Amp.)	Must be connected.
GND	Black	0V	Ground	Must be connected.

Table 1. Power Supply Lines (Note 2)

Note 2. Each supply line should be distributed separately from the power supply unit

2) Evaluation Mode

2-1) D/A Evaluation using the AK4118A (DIR) (Coaxial connectior) < default >

The AK4118A generates MCLK, BICK, LRCK, SDATA1 and SDATA2 from the data from the BNC connector (J1). Evalutations using a test CD and etc. are available (Note 3).

Setting: R46 = “open”, R48 = “short (0Ω)”

Note 3. Coaxial connection is recommended when evaluating the sound quality.

2-2) D/A Evaluation using the AK4118 (DIR) (Optical connectior)

The AK4118A generates MCLK, BICK. LRCK, SDATA1 and SDATA2 from the data from the optical connector (PORT1). Evalutations using a test CD and etc. are available.

Setting: R46 = “short (0Ω)”, R48 = “open”

2-3) All interface signals including the master clock are supplied externally (PORT2)

Setting: R30, R32, R34, R36, R38 = “open”, R29, R31, R33, R35, R37 = “short (0Ω)”

3) Jumper Pins and Switch Setting

3-1) Jumper Pin Settings

[JP1 (DZF1)]: Selects connection to the DIF1/DZF1 pin
OPEN : Serial Control Mode
SHORT : Parallel Control Mode < Default >

[JP2 (DZF2)]: Selects connection to the ACKS/DZF2 pin.
OPEN : Serial Control Mode
SHORT : Parallel Control Mode < Default >

[JP3 (DSDR1)]: Not for Use
Fixed to “SHORT”.

[JP4 (PIC)]: Not for Use
Fixed to “Open”. Do not connect anything.

3-2). SW Settings

Switch Up: “ON (H)”. Switch Down: “OFF (L)”.

[SW3] (SW DIP-2): AK4118A Setting

No.	Name	ON (“H”)	OFF (“L”)	Default
1	OCKS1	Master Clock setting for AK4118A Refer to Table 5		ON
2	OCKS0			OFF

Table 2. AK4118A Mode Setting

[SW4] (SW DIP-6): AK4413 Setting 1

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SMUTE	SMUTE ON	SMUTE OFF	OFF
2	TDM1	Audio I/F Format for AK4413 Refer to Table 6		OFF
3	TDM0			OFF
4	DEM1	De-emphasis Control Refer to Table 7		OFF
5	DEM0			ON
6	PSN	Parallel Control Mode	Serial Control Mode	ON

Table 3. AK4413-1 Mode Setting

[SW5] (SW DIP-6): AK4413 Setting 2

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SLOW	Digital Filter Setting Refer to Table 8		OFF
2	ACKS	Auto Setting Mode	Manual Setting Mode	ON
3	DIF2	Audio I/F Format for AK4413 Refer to Table 6		OFF
4	DIF1			ON
5	DIF0 /CAD1			OFF
		CAD1pin=”H”	CAD1pin=”L”	
6	SD /CAD0	Digital Filter Setting Refer to Table 8		ON
		CAD0pin=”H”	CAD0pin=”L”	

Table 4. AK4413-2 Mode Setting

OCKS1	OCKS0	MCKO1	
L	L	256fs	
H	L	512fs	<Default>
H	H	128fs	

Table 5. AK4118A Master Clock Setting

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK	
Normal	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs	
	1			0	0	1	20-bit LSB justified	H/L	≥40fs	
	2			0	1	0	24-bit MSB justified	H/L	≥48fs	<Default>
	3			0	1	1	24-bit I^2S compatible	L/H	≥48fs	
	4			1	X	X	24-bit LSB justified	H/L	≥48fs	
TDM256		0	1	0	0	0	N/A			
				0	0	1	N/A			
	8			0	1	0	24-bit MSB justified	↑	256fs	
	9			0	1	1	24-bit I^2S compatible	↓	256fs	
	10			1	X	X	24-bit LSB justified	↑	256fs	
TDM128		1	1	0	0	0	N/A			
				0	0	1	N/A			
	14			0	1	0	24-bit MSB justified	↑	128fs	
	15			0	1	1	24-bit I^2S compatible	↓	128fs	
	16			1	X	X	24-bit LSB justified	↑	128fs	

Table 6. AK4413 Audio I/F Format

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	< Default >
1	0	48kHz	
1	1	32kHz	

Table 7. De-emphasis Control

SD	SLOW	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll-off	< Default >
1	1	Short delay slow roll-off	

Table 8. Digital Filter Setting

4) Power ON

Switch Up: “ON (H)”, Switch Down: “OFF (L)”.

Power-down reset by SW1(PDN) and SW2(DIR-PDN) must be made once after power up the evaluation board. Put the SW1 and SW2 to “L” for power-down reset of the AK4413 and AK4118A, and the return them to “H” to release the power-down state.

[SW1] (PDN): Resets the AK4413 (Keep “H” during normal operation.)
This switch must be set to “L” once upon power up the evaluation board to reset the AK4413.

[SW2] (DIR-PDN): Resets the AK4118A (Keep “H” during normal operation.)
This switch must be set to “L” once upon power up the evaluation board to reset the AK4118A. When not using the AK4118A, keep this switch to “L”.

■ Board Control

The AKD4413-SA can be controlled via a USB port with a PC. Connect J2 (USB) connector to a PC with USB cable. The control software is included in the AKD4413-SA package. Refer to the "Control Software Manual" paragraph for operational sequence of the control software.

■ External Analog Filter

The AKD4413 has a differential output circuit that outputs differential outputs of the AK4413 via a non-inverting buffer (second order LPF, fs=106.4k, Q=0.698, G=+3.9dB) and a LPF (first order LPF, fs=284k, G=-0.84dB). A low-noise and high-voltage operatinal amplifier the LME49710NA is used on the AKD4413. The output signal from the BNC connector is about 2.8Vrms (Typ@VREF=5.0V).

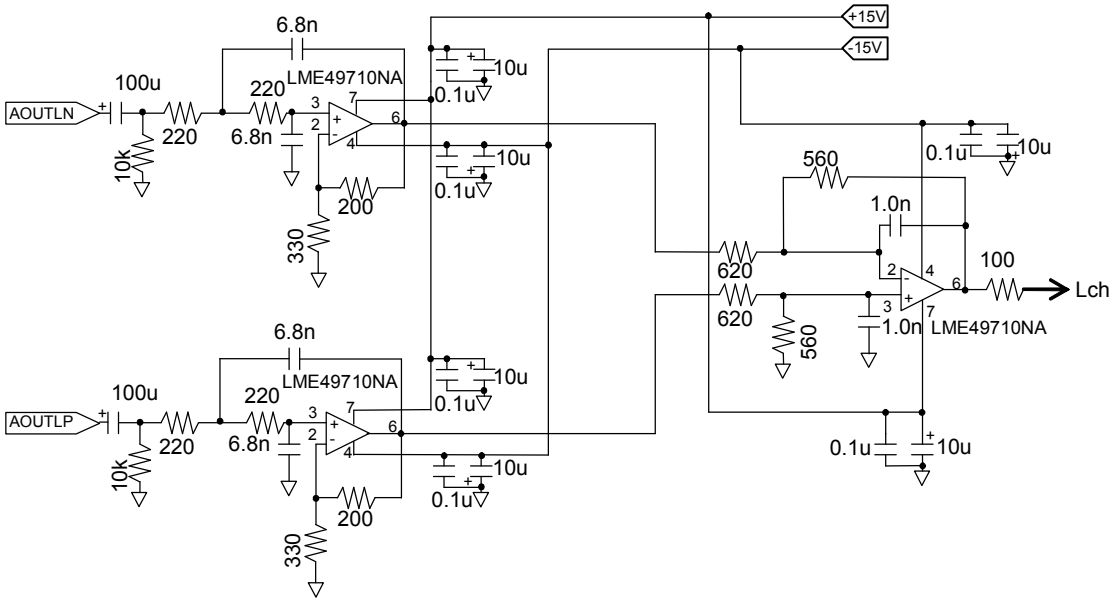


Figure 2. External Analog Filter

AKD4413-SA Filter	40kHz (Double)	80kHz (Quad)
Internal Filter	-0.3dB	-1dB
External LPF	-0.12dB	-1.3dB
Total	-0.42dB	-2.3dB

This table indicates typical values.

Table 9. Frequency Responses

■ Capacitor between VREFH and VREFL pins

Low-frequency distortion can be improved by connecting a large capacitance capacitor between the VREFH pin and the VREFL pin (Figure 3). Capacitors between the VREFH pin and the VREFL pin are shown as C159 and C160 in the circuit diagram.

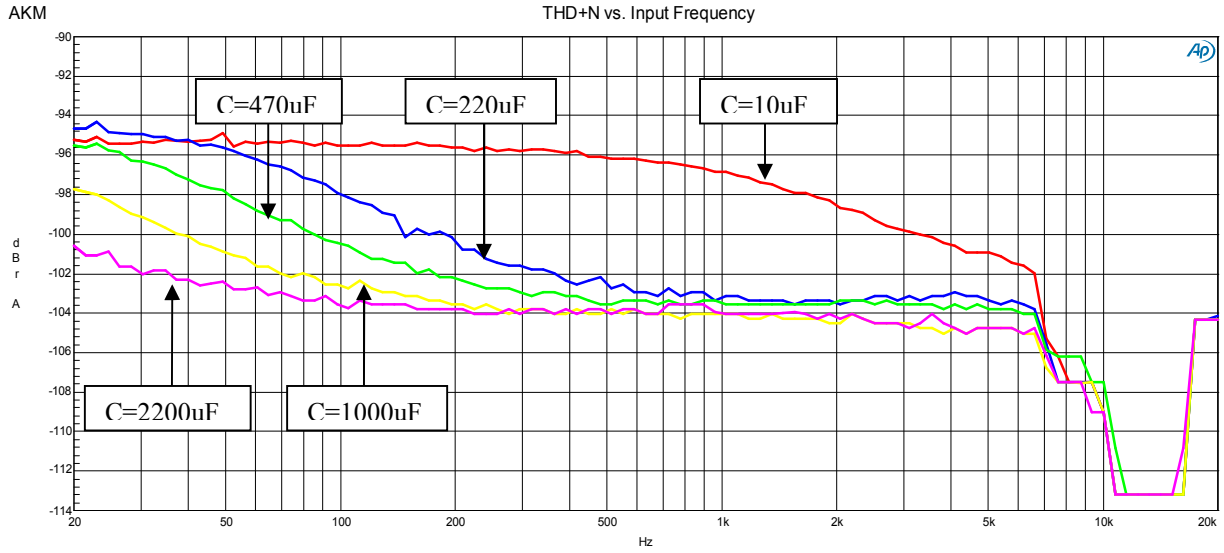


Figure 3. THD+N vs. Input Frequency

CONTROL SOFTWARE MANUAL

■ Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed. According to the previous terms.
2. Connect the evaluation board and a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please disconnect the evaluation board once and reconnect it to the PC.
4. Insert the CD-ROM labeled “AKD4413 Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “akd4413-sa.exe” to open the control program.
6. Begin evaluation by following the procedure below.

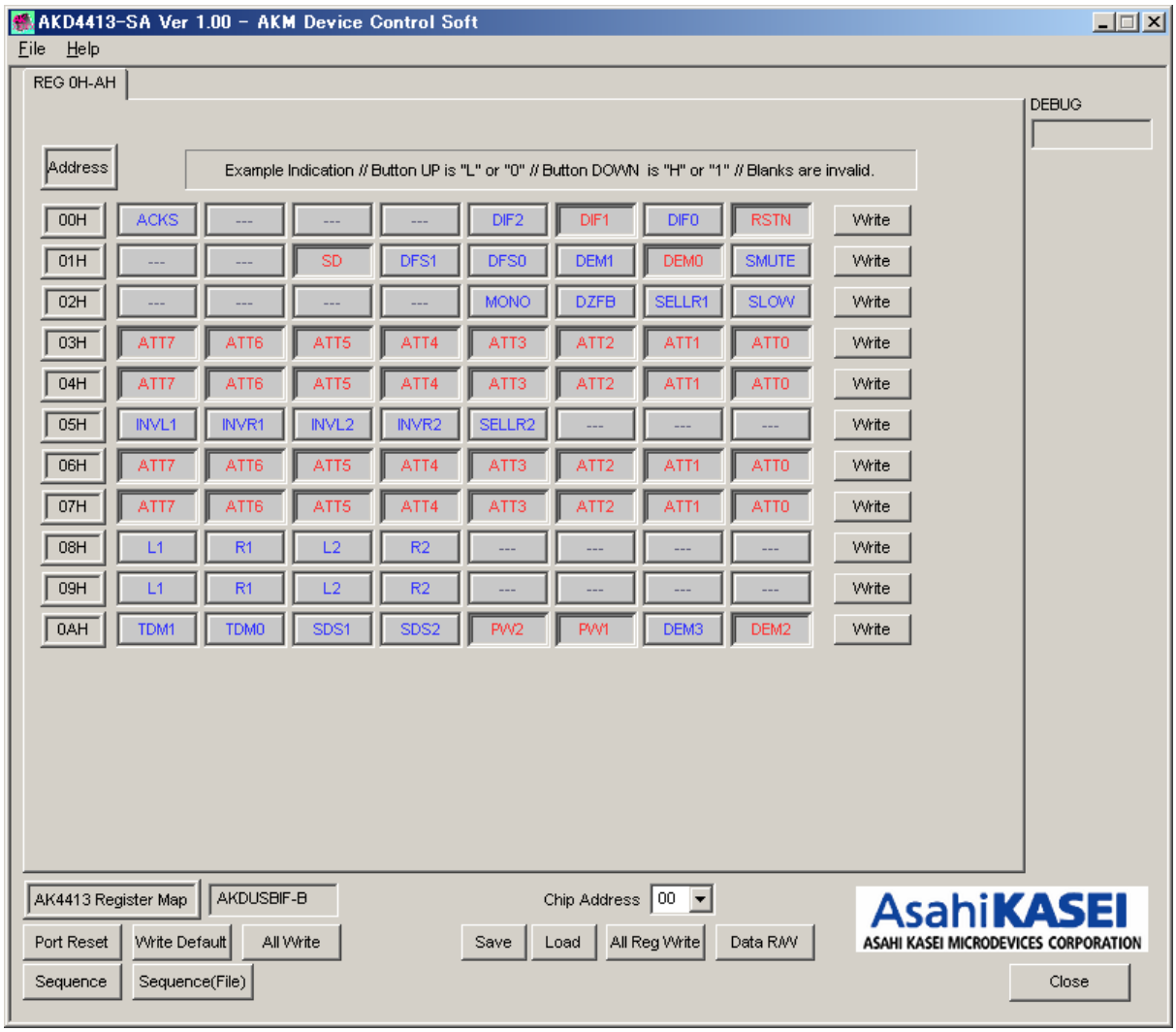


Figure 4. Control Software Window

■ Operation Overview

Register map is controlled by this control software.

Frequently used buttons such as the register initializing button “Write Default”, are located outside of the tab window. Refer to the “■ Dialog Boxes” section for details of each dialog box setting.

1. [Port Reset]: Resets the USB port of the main board.
   Click this button after the control software starts up when a PC is connected to J2 (USB) port of the AKD4413.

2. [Write Default]: Initializes register values.
   Use this button to initialize the registers after the device is reset by hardware reset.

3. [All Write]: Executes all write commands of displayed registers.

4. [Save]: Saves current register settings as a file.

5. [Load]: Executes data write from a saved file.

6. [All Reg Write]: “All Reg Write” dialog box pops up.

7. [Data R/W]: “Data R/W” dialog box pops up.

8. [Sequence]: “Sequence” dialog box pops up.

9. [Sequence(File)]: “Sequence(File)” dialog box pops up.

■ Tab Descriptions

1. [REG]: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.
Button Down indicates “1” and the bit name is shown in red (when read-only, the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only, the name is shown in gray)

Grayed out registers are Read-only registers. They can not be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

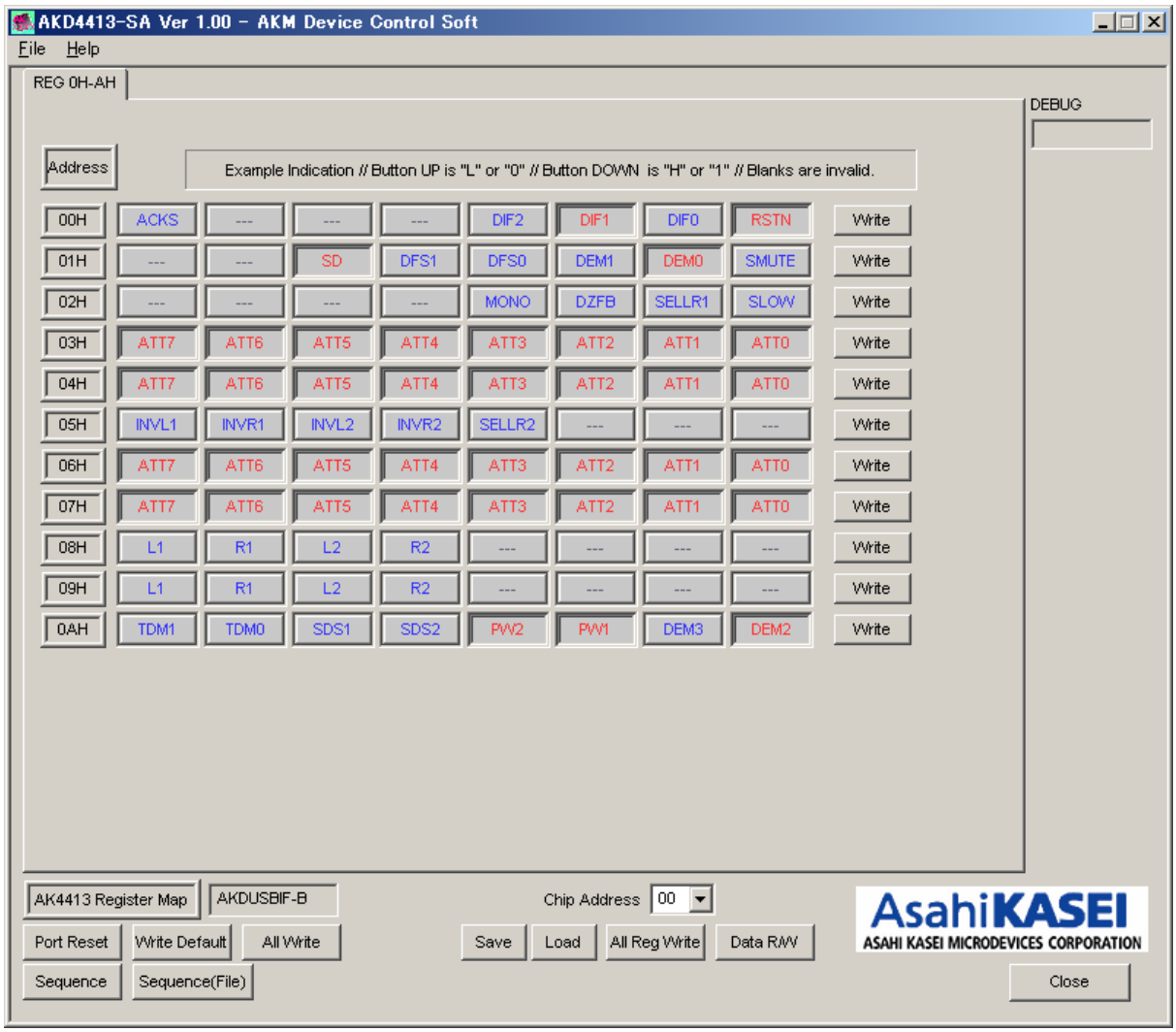


Figure 5. REG Window

[Write]: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register name is checked, the data will become "1". When the checkbox is not checked, the data will become "0". Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

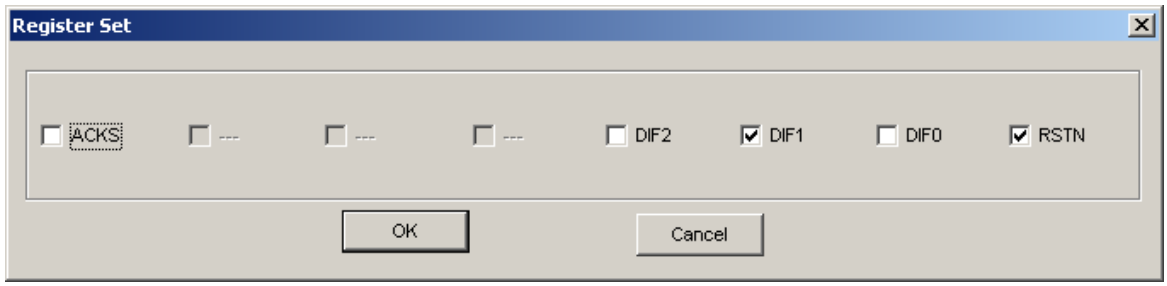


Figure 6. Register Set Window

■ Dialog Boxes

1.[All Req Write]

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

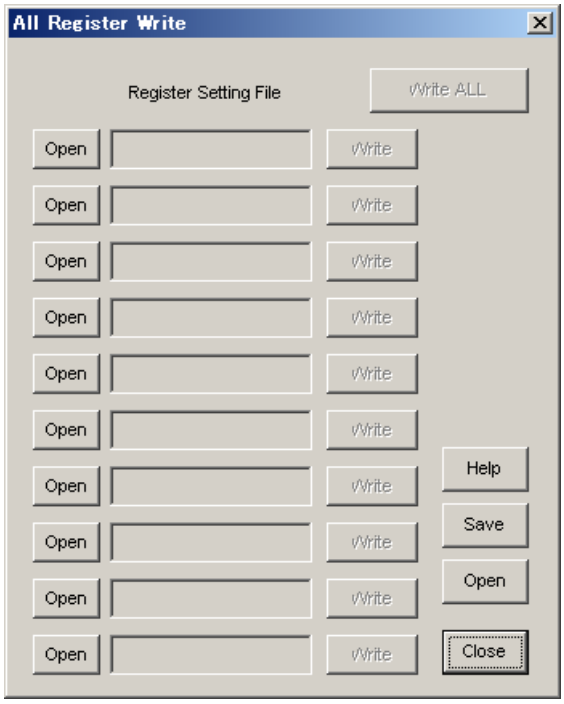


Figure 7. All Reg Write Window

[Open (left)] : Open a register setting file (*.akr).
[Write] : Executes register writing.
[Write All] : Executes all register writings.
Writings are executed in descending order.
[Help] : A help window pops up.
[Save] : Saves register setting file assignment. The file name is "*.mar".
[Open (right)] : Open a register setting assignment file that is saved as "*. mar".
[Close] : Closes the dialog box and finishes this process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2.[Data R/W]

Click the [Data R/W] button in the main window to open the data read/write dialog box shown below.
A data write is executed to specified address.

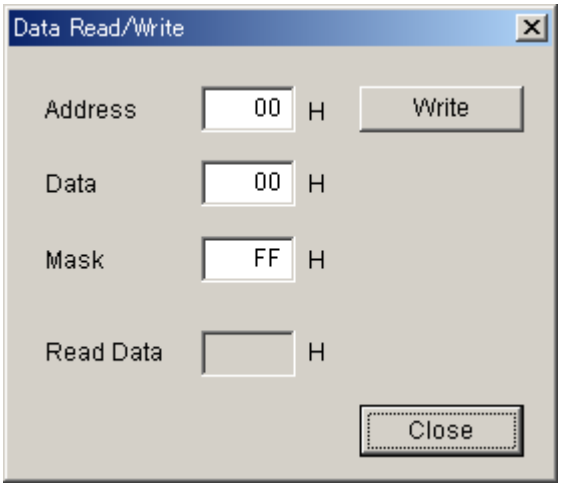


Figure 8. Data R/W Window

[Address] Box: Input write data address in hexadecimal numbers for data writing.
[Data] Box: Input start data in hexadecimal numbers.
[Mask] Box: Input mask data in hexadecimal numbers.
This value "ANDed" with the write data becomes the input data.

[Write] Button: Writes data to the address specified in "Address" box (Note 4).
[Close] Button: Closes the dialog box.
Data write can be cancelled by this button instead of [Write] button.

Note 4. The register map will be updated after executing the [Write] command.

3.[Sequence]

Click the [Sequence] button to open register sequence setting dialog box shown below.
Register sequence can be set in this dialog box.

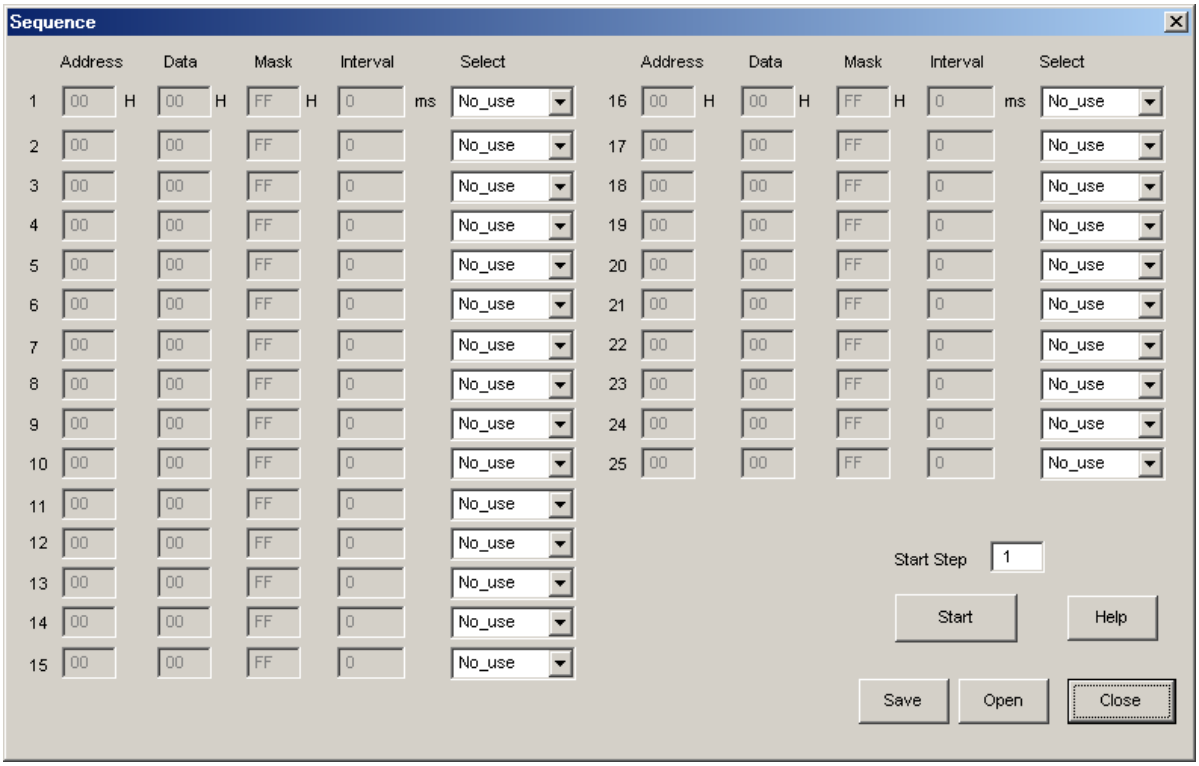


Figure 9. Sequence Window

Sequence Setting

Set register sequence according to the following process bellow.

(1) Select a command

Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >
- No_use : Not using this address
- Register : Register write
- Reg(Mask) : Register write (Masked)
- Interval : Takes an interval
- Stop : Pauses the sequence
- End : Ends the sequence

(2) Input sequence

[Address] : Data address
[Data] : Write data
[Mask] : Mask
The value in the [Data] box is ANDed with the value in the [Mask] box. This data becomes the actual input data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval] : Interval time

Valid boxes for each process command are shown bellow.

· No_use : None
· Register : [Address], [Data], [Interval]
· Reg(Mask) : [Address], [Data], [Mask], [Interval]
· Interval : [Interval]
· Stop : None
· End : None

Control Buttons

Functions of Control Buttons are shown bellow.

[Start] Button: Executes the sequence
[Help] Button: A help window pops up.
[Save] Button: Saves sequence settings as a file. The file name is "*.aks".
[Open] Button: Open a sequence setting file "*.aks".
[Close] Button: Closes the dialog box and finish the process.

Stop of the sequence

When "Stop" is selected in the sequence, the process is paused. It starts again when the [Start] button is clicked. Restart step number is shown in the "Start Step" box. When executing the process until the end of sequence, the "Start Step" value will return to "1".

The sequence can be started from any step by writing a step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4.[Sequence(File)]

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.
Files saved in the "Sequence setting dialog" can be applied in this dialog.

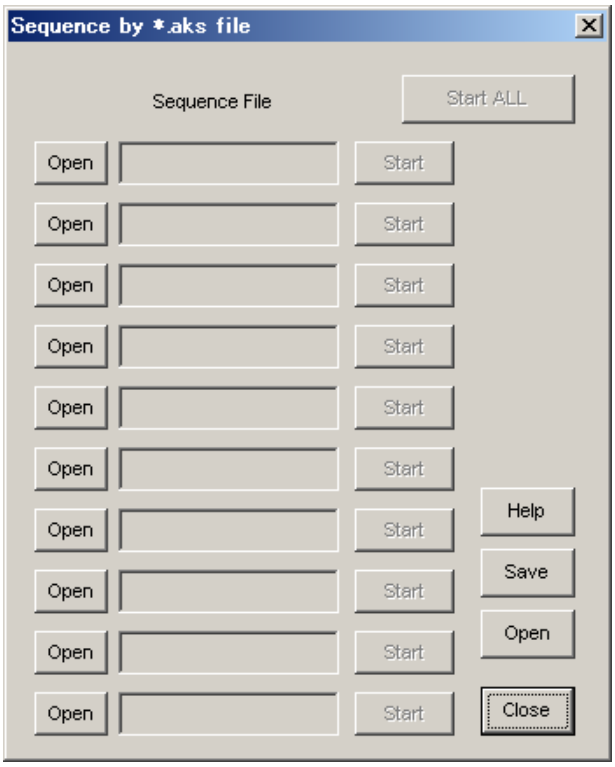


Figure 10. Sequence(File) Window

[Open (left)] : Open a sequence setting file (*.aks).
[Start] : Executes the sequence setting.
[Start All] : Executes all sequence settings.
Sequences are executed in descending order.
[Help] : A help window pops up.
[Save] : Saves a sequence setting file assignment. The file name is "*.mas".
[Open(right)] : Open a saved sequence setting file assignment "*. mas".
[Close] : Closes the dialog box and finish the process.

Operating Suggestions

(1) Files saved by the [Save] button and opened by the [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
(2) When "Stop" is selected in the sequence the process will be paused and the message box shown below pops up. Click "OK" to continue the process.

Figure 11. Sequence Pause Window

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (44.1kHz), 256fs (96kHz), 128fs (192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD= DVDD=3.3V, VDD1, 2=VREFH1, 2=5V
- Interface : Internal DIR (44.1kHz, 96kHz, 192kHz)
- Temperature : Room
- Operational Amplifiers : LME49710NA

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results			
			LOUT1 / ROUT1		LOUT2 / ROUT2	
S/(N+D)	1kHz, 0dB	20kHz SPCL LPF	103.6	104.8	105.6	103.7
DR	1kHz, -60dB		117.5	117.5	117.4	117.8
		A-weighted	120.1	120.1	120.0	120.2
S/N	"0" data	20kHz SPCL LPF	117.6	117.4	117.5	117.6
		A-weighted	120.0	120.0	120.1	120.2

fs=96kHz

Parameter	Input signal	Measurement filter	Results			
			LOUT1 / ROUT1		LOUT2 / ROUT2	
S/(N+D)	1kHz, 0dB	40kHz LPF	102.5	103.9	102.7	102.7
DR	1kHz, -60dB		114.7	114.8	114.7	114.7
		A-weighted	120.1	119.8	119.9	120.0
S/N	"0" data	40kHz LPF	114.9	114.7	114.8	114.8
		A-weighted	120.3	120.0	120.0	120.0

fs=192kHz

Parameter	Input signal	Measurement filter	Results			
			LOUT1 / ROUT1		LOUT2 / ROUT2	
S/(N+D)	1kHz, 0dB	40kHz LPF	101.0	102.9	101.8	103.5
DR	1kHz, -60dB		114.3	112.1	113.3	111.9
		A-weighted	119.2	116.1	117.3	116.0
S/N	"0" data	40kHz LPF	114.8	114.8	114.8	114.8
		A-weighted	120.1	120.0	120.0	120.0

Plots

fs=44.1kHz

・FFT1 (fin=1kHz, Input Level=0dBFS)

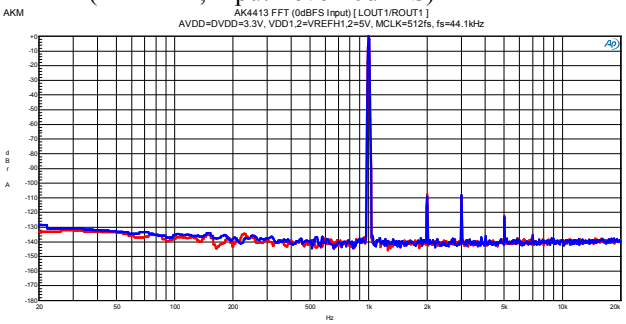


Figure 12. LOUT1/ROUT1

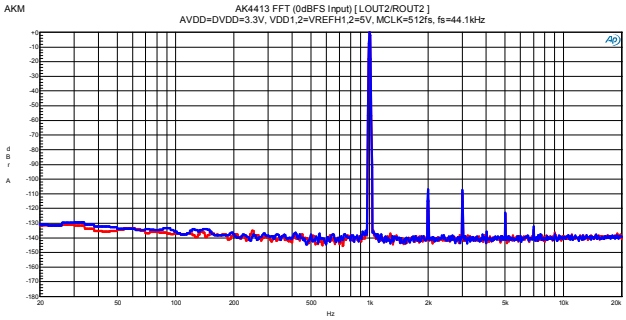


Figure 13. LOUT2/ROUT2

・FFT2 (fin=1kHz, Input Level=-60dBFS)

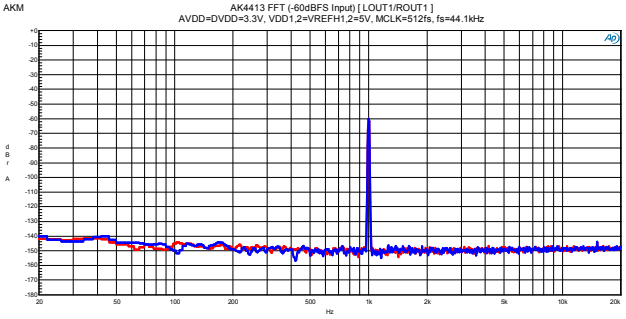


Figure 14. LOUT1/ROUT1

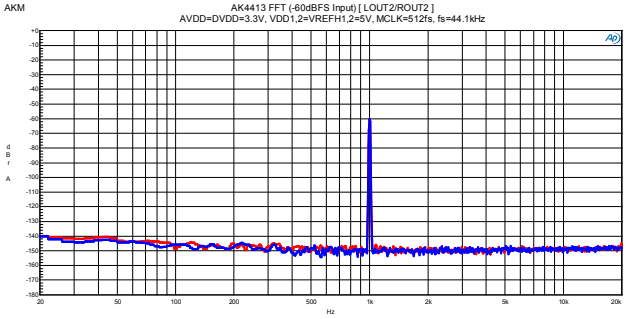


Figure 15. LOUT2/ROUT2

・FFT3 (Noise Floor)

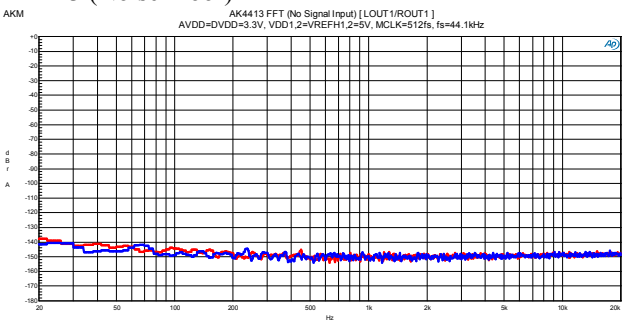


Figure 16. LOUT1/ROUT1

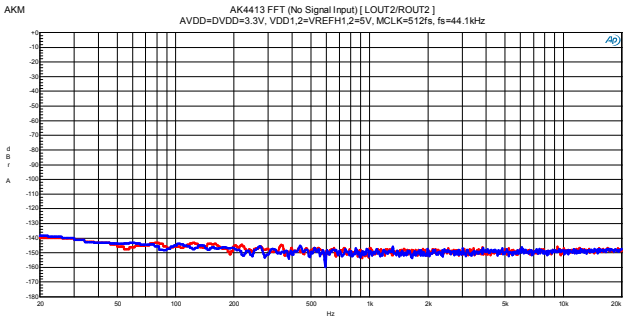


Figure 17. LOUT2/ROUT2

▪ FFT4 (Out of Band Noise)

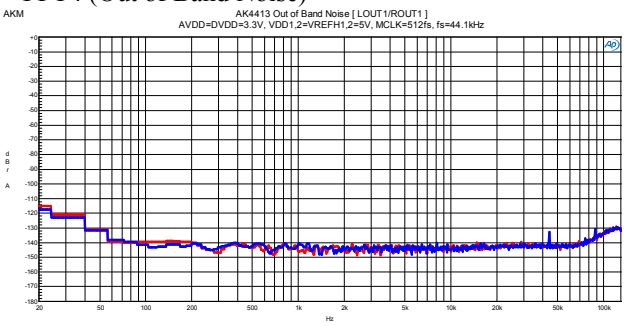


Figure 18. LOUT1/ROUT1

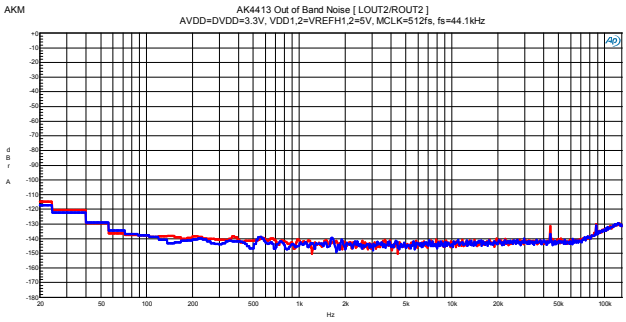


Figure 19. LOUT2/ROUT2

▪ THD+N vs. Input Level

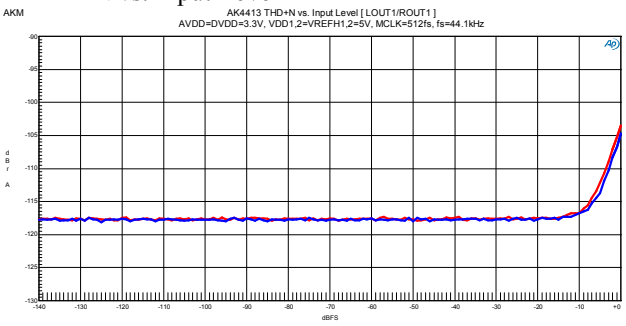


Figure 20. LOUT1/ROUT1

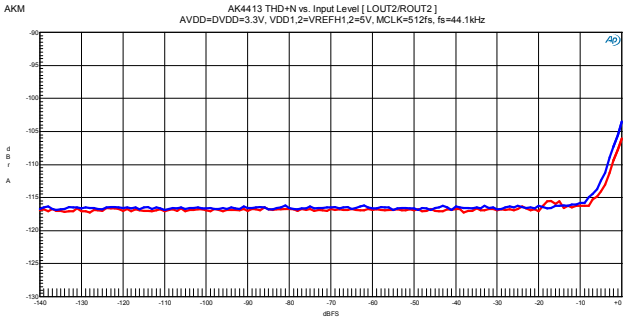


Figure 21. LOUT2/ROUT2

▪ THD+N vs. Input Frequency

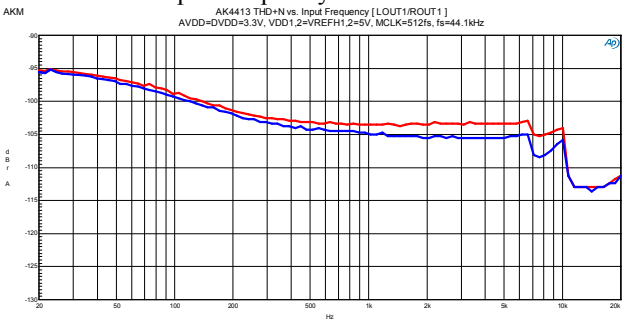


Figure 22. LOUT1/ROUT1

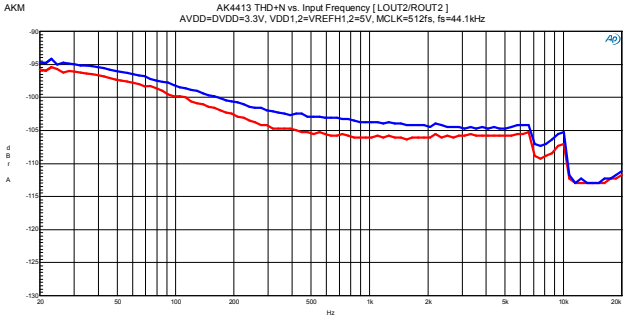


Figure 23. LOUT2/ROUT2

・Linearity

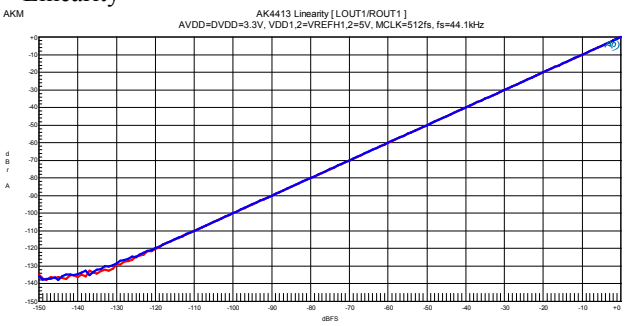


Figure 24. LOUT1/ROUT1

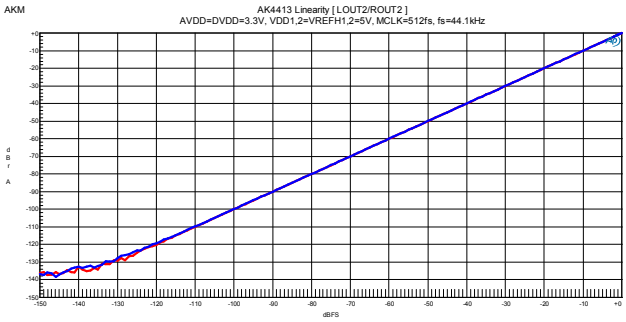


Figure 25. LOUT2/ROUT2

・Frequency Response

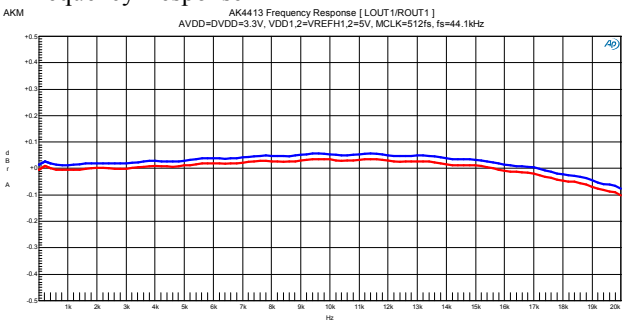


Figure 26. LOUT1/ROUT1

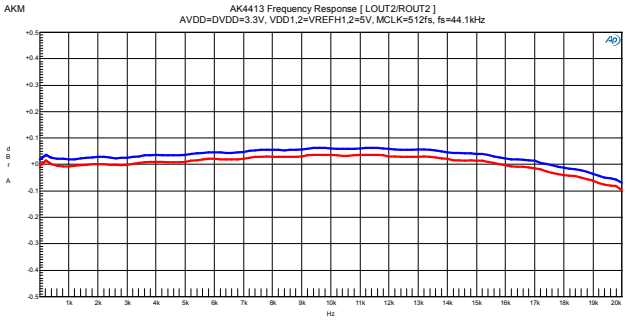


Figure 27. LOUT2/ROUT2

・Crosstalk

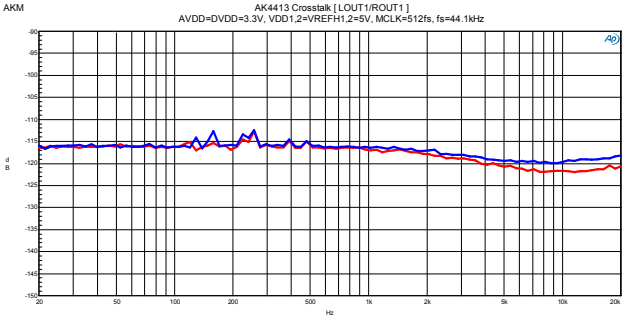


Figure 28. LOUT1/ROUT1

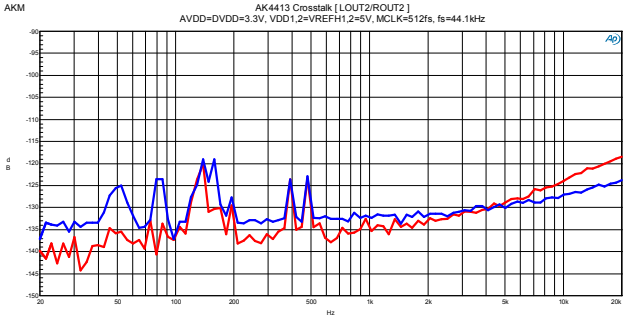


Figure 29. LOUT2/ROUT2

fs=96kHz

・FFT1 (fin=1kHz, Input Level=0dBFS)

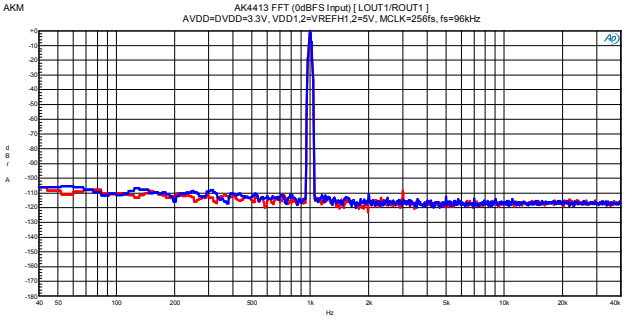


Figure 30. LOUT1/ROUT1

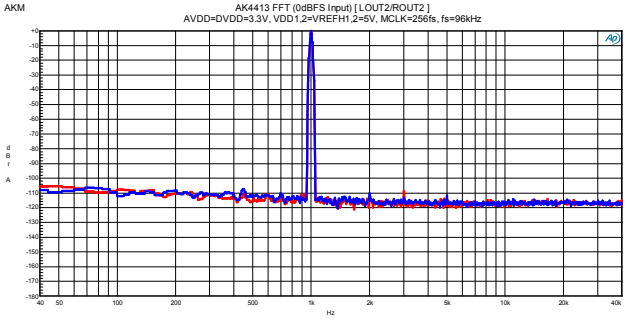


Figure 31. LOUT2/ROUT2

・FFT2 (fin=1kHz, Input Level=0dBFS, Notch)

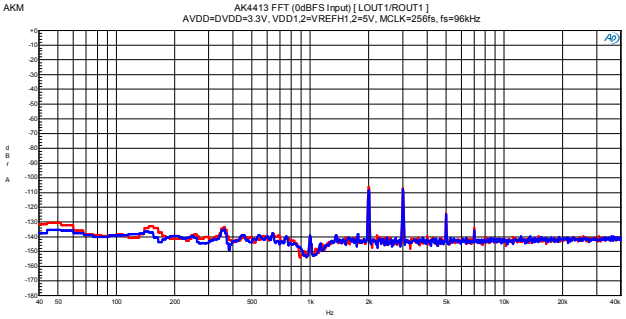


Figure 32. LOUT1/ROUT1

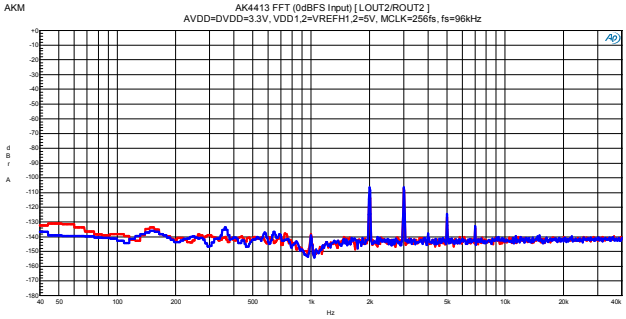


Figure 33. LOUT2/ROUT2

・FFT3 (fin=1kHz, Input Level=-60dBFS)

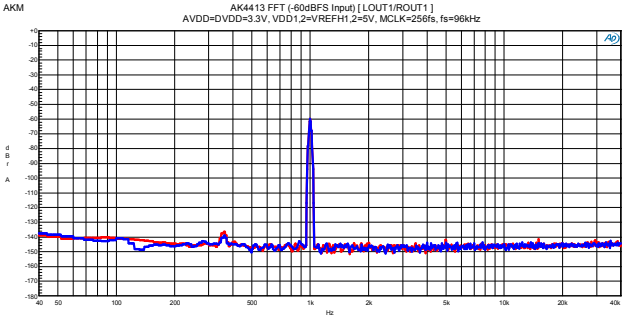


Figure 34. LOUT1/ROUT1

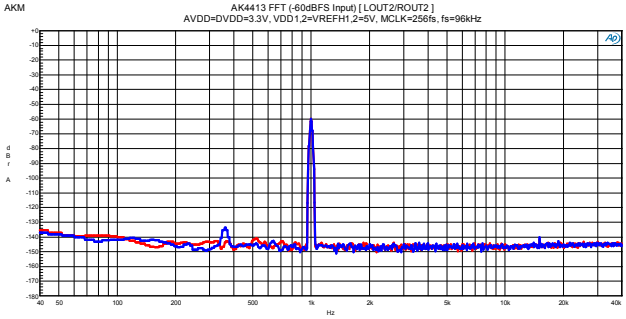


Figure 35. LOUT2/ROUT2

・FFT4 (Noise Floor)

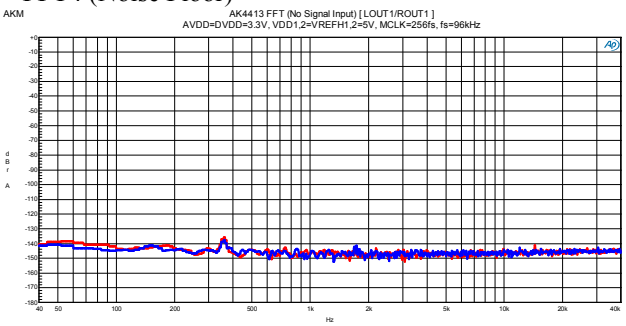


Figure 36. LOUT1/ROUT1

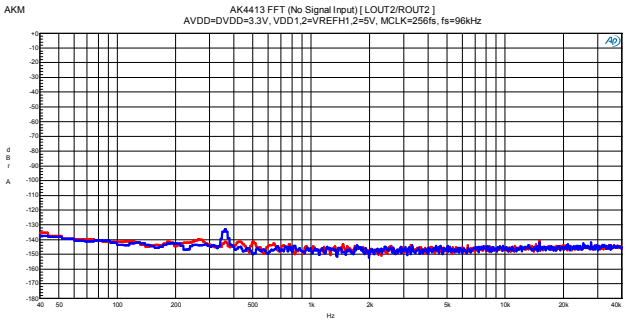


Figure 37. LOUT2/ROUT2

・THD+N vs. Input Level

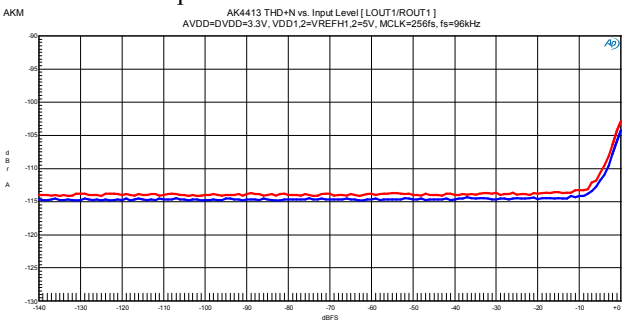


Figure 38. LOUT1/ROUT1

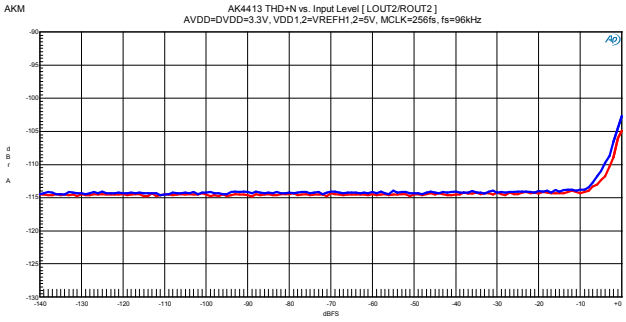


Figure 39. LOUT2/ROUT2

・THD+N vs. Input Frequency

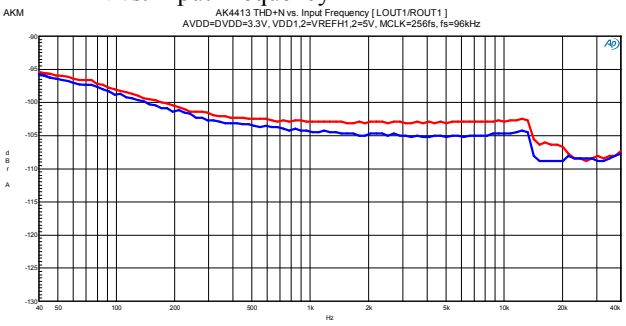


Figure 40. LOUT1/ROUT1

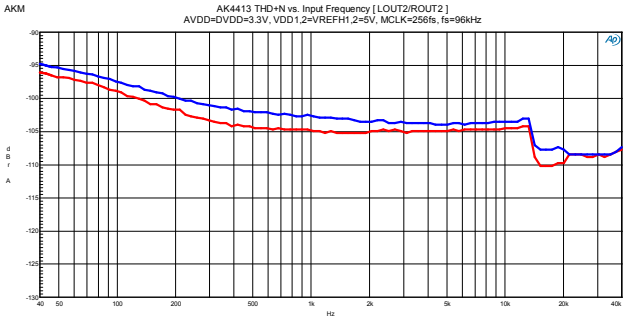


Figure 41. LOUT2/ROUT2

・Linearity

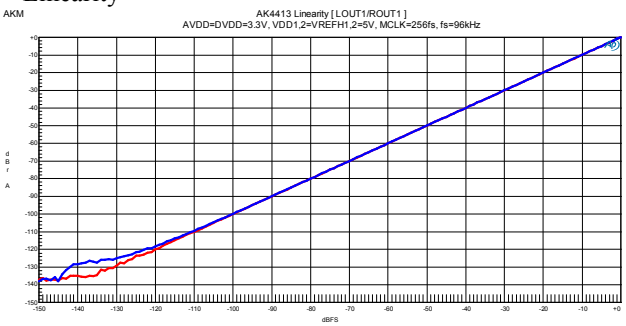


Figure 42. LOUT1/ROUT1

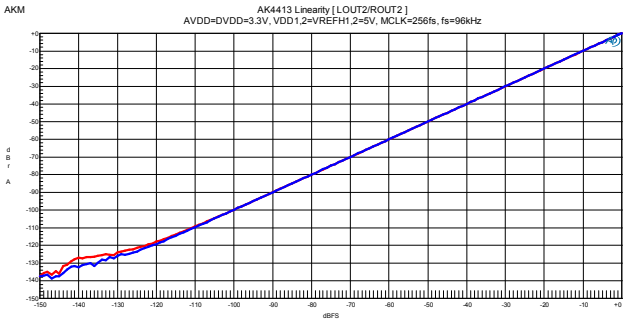


Figure 43. LOUT2/ROUT2

・Frequency Response

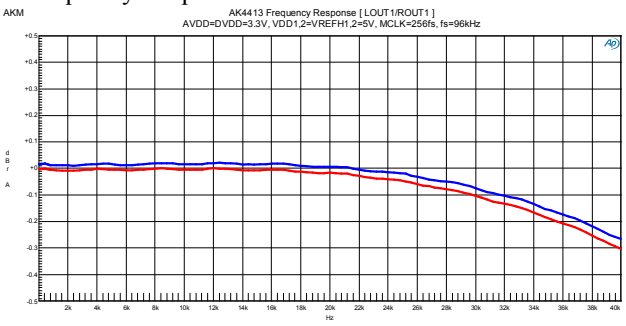


Figure 44. LOUT1/ROUT1

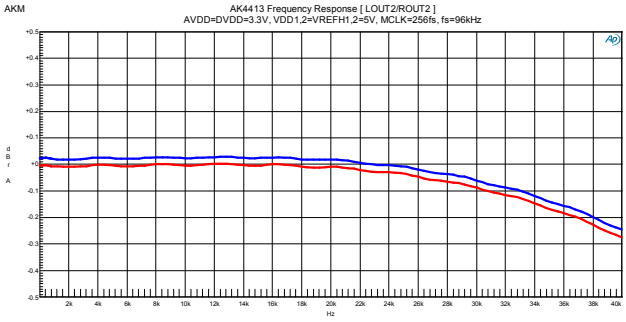


Figure 45. LOUT2/ROUT2

・Crosstalk

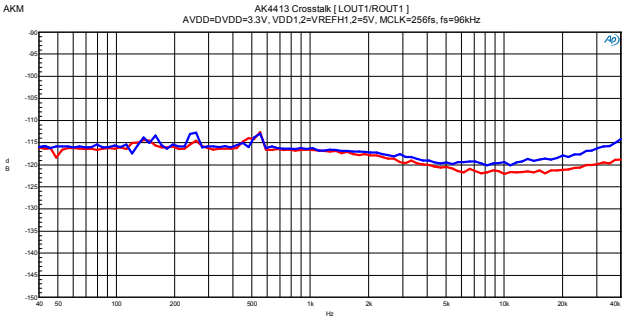


Figure 46. LOUT1/ROUT1

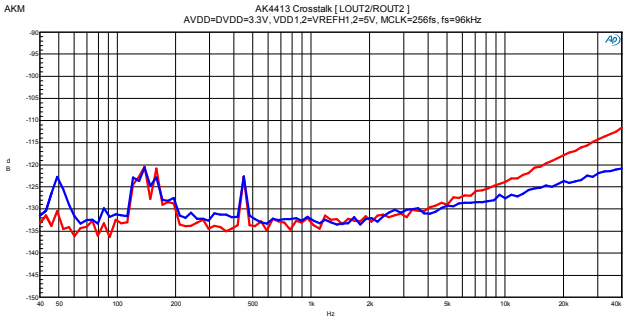


Figure 47. LOUT2/ROUT2

fs=192kHz

・FFT1 (fin=1kHz, Input Level=0dBFS)

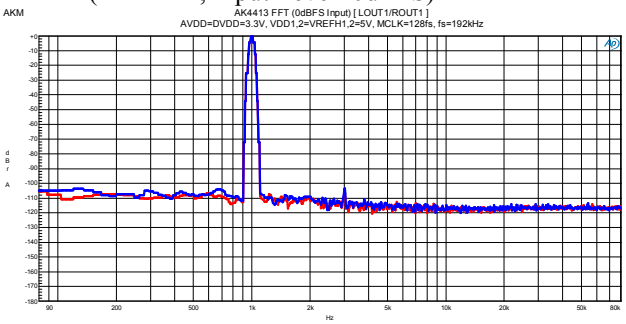


Figure 48. LOUT1/ROUT1

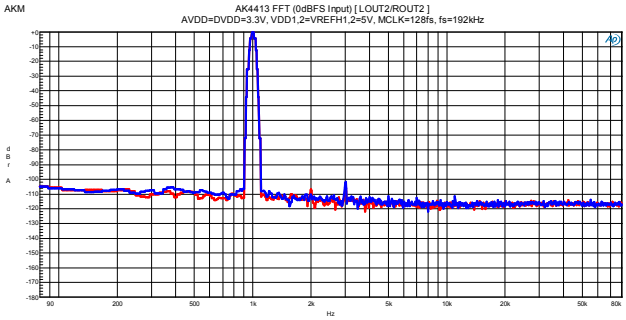


Figure 49. LOUT2/ROUT2

・FFT2 (fin=1kHz, Input Level=0dBFS, Notch)

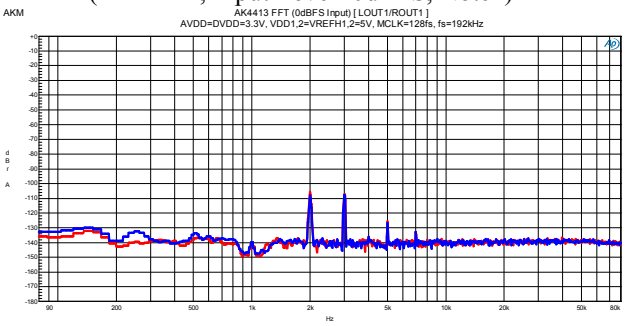


Figure 50. LOUT1/ROUT1

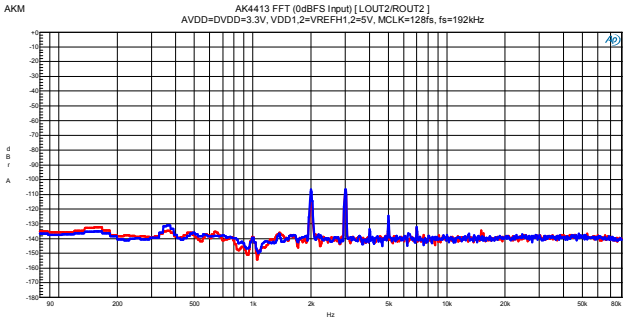


Figure 51. LOUT2/ROUT2

・FFT3 (fin=1kHz, Input Level=-60dBFS)

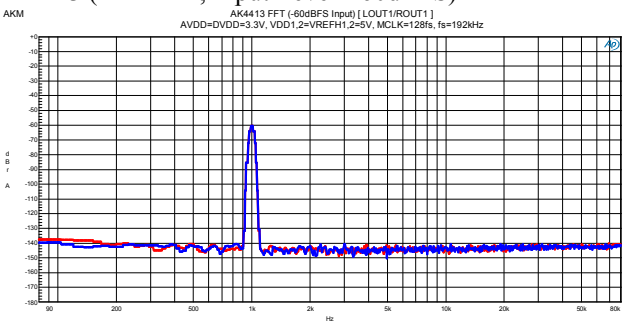


Figure 52. LOUT1/ROUT1

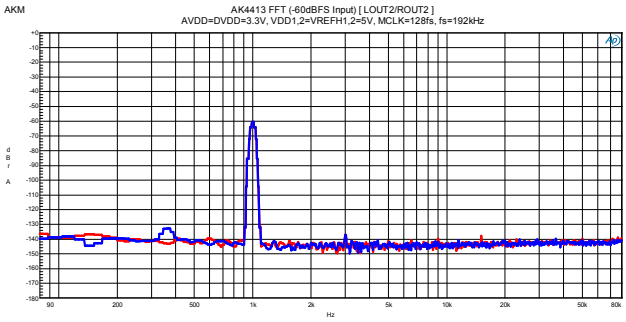


Figure 53. LOUT2/ROUT2

・FFT4 (Noise Floor)

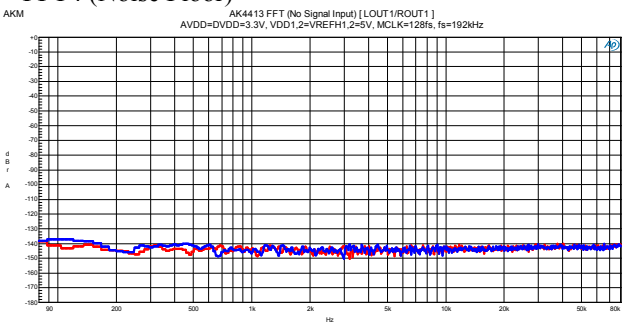


Figure 54. LOUT1/ROUT1

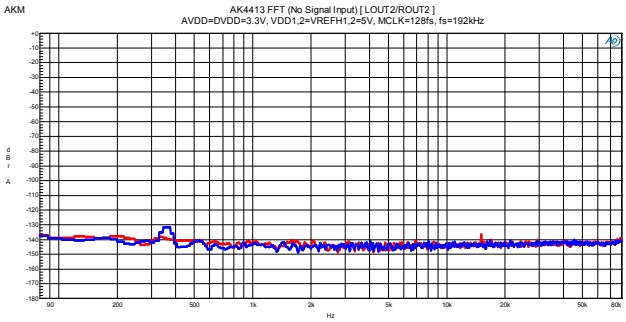


Figure 55. LOUT2/ROUT2

・THD+N vs. Input Level

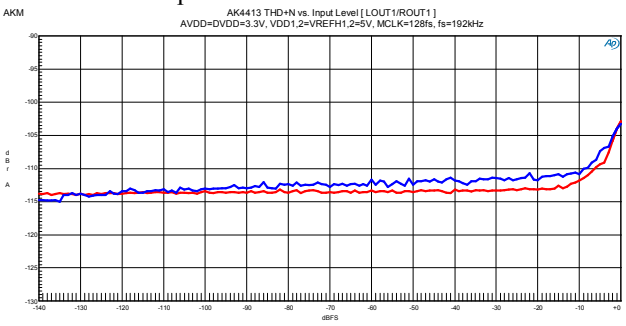


Figure 56. LOUT1/ROUT1

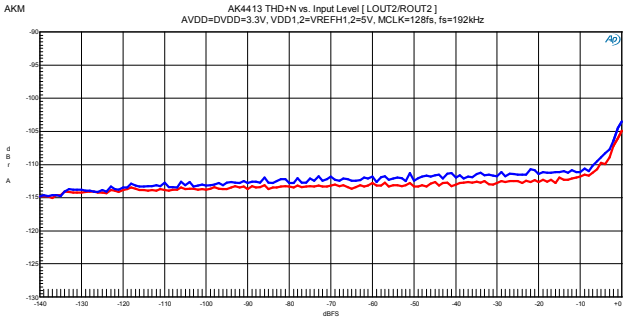


Figure 57. LOUT2/ROUT2

・THD+N vs. Input Frequency

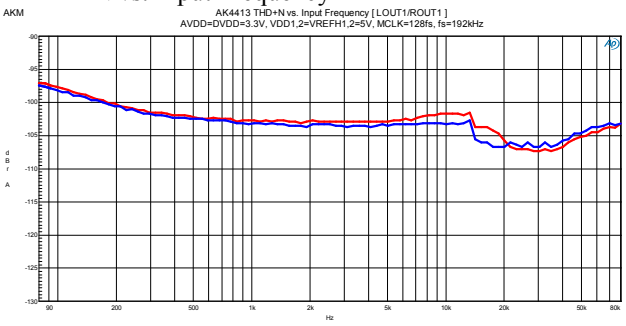


Figure 58. LOUT1/ROUT1

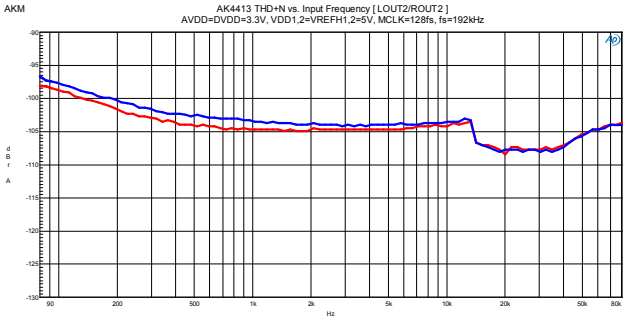


Figure 59. LOUT2/ROUT2

・Linearity

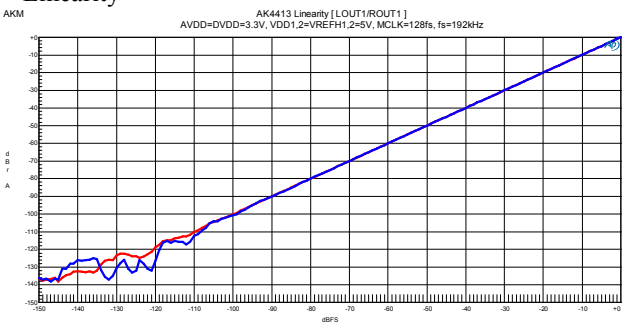


Figure 60. LOUT1/ROUT1

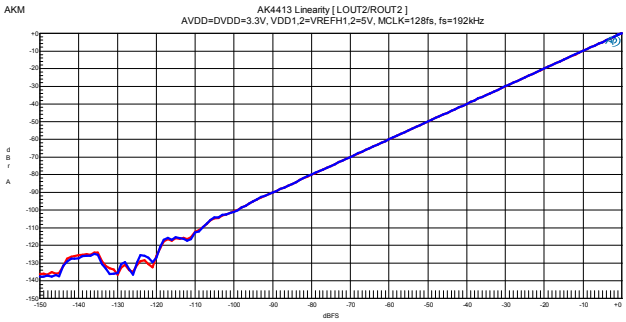


Figure 61. LOUT2/ROUT2

・Frequency Response

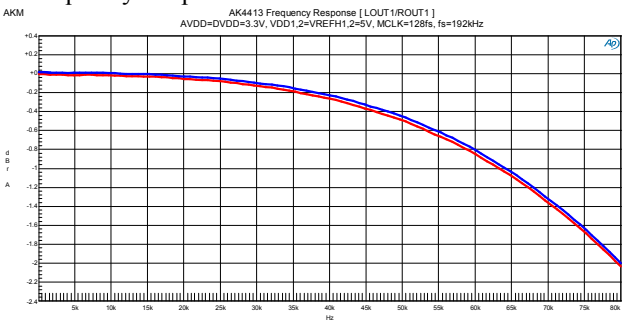


Figure 62. LOUT1/ROUT1

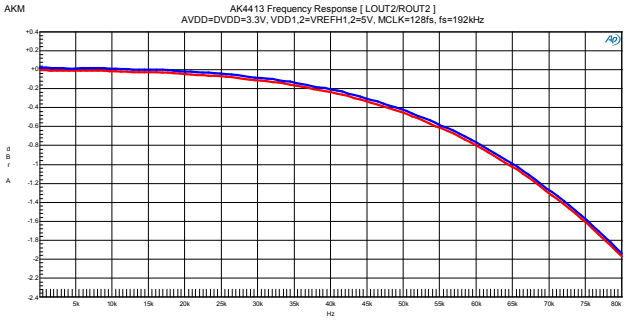


Figure 63. LOUT2/ROUT2

・Crosstalk

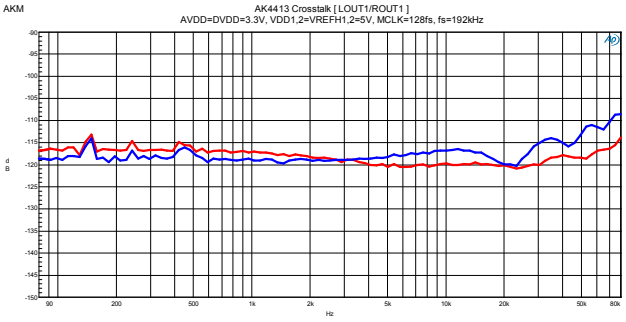


Figure 64. LOUT1/ROUT1

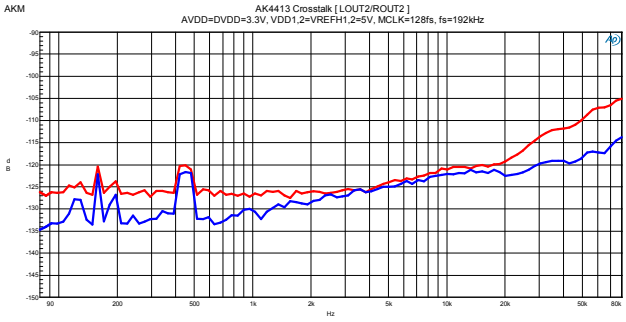
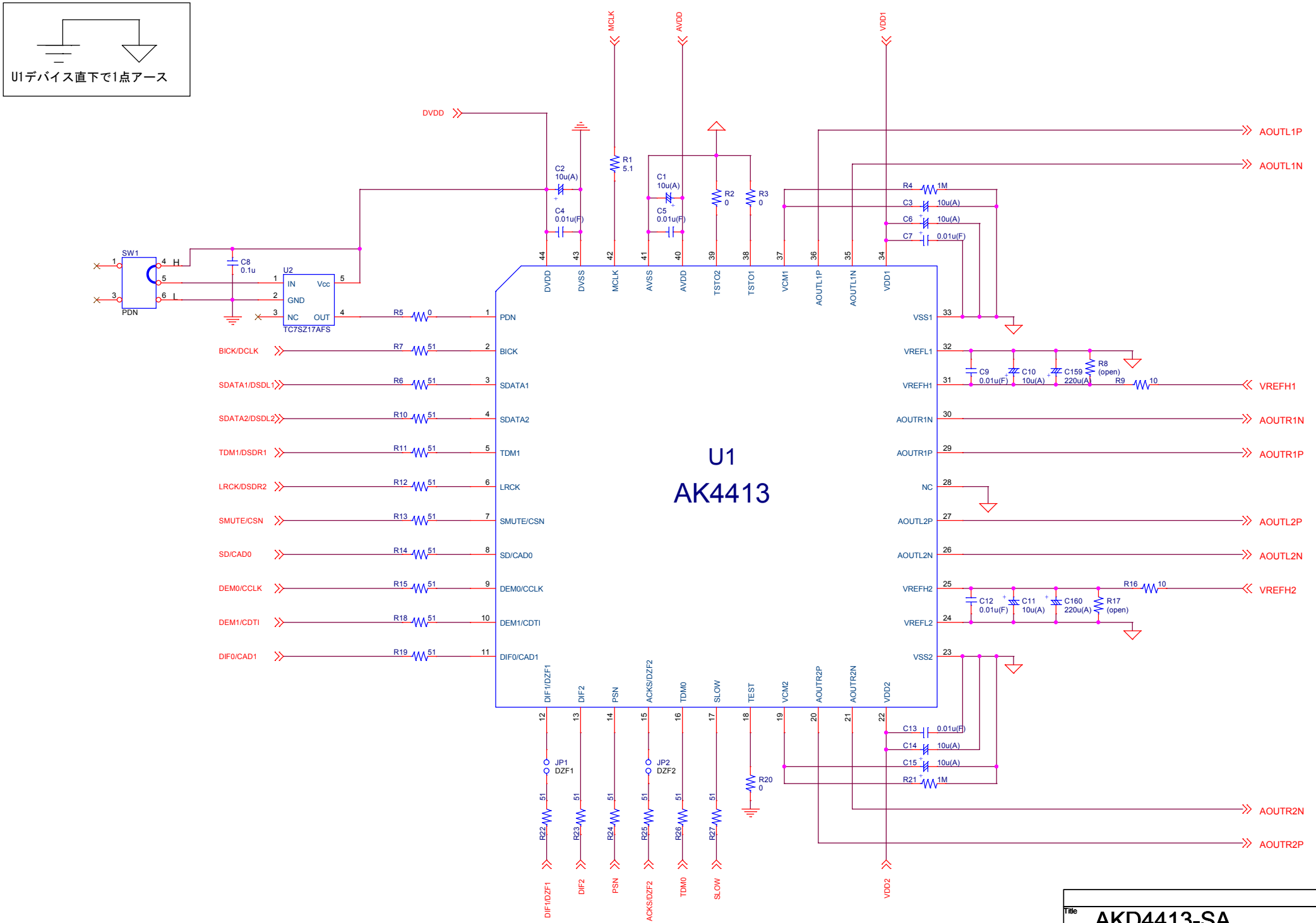


Figure 65. LOUT2/ROUT2

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
12/06/27	KM111500	0	First edition	-	
12/10/03	KM111501	0	Change	8	Figure 3 was changed.



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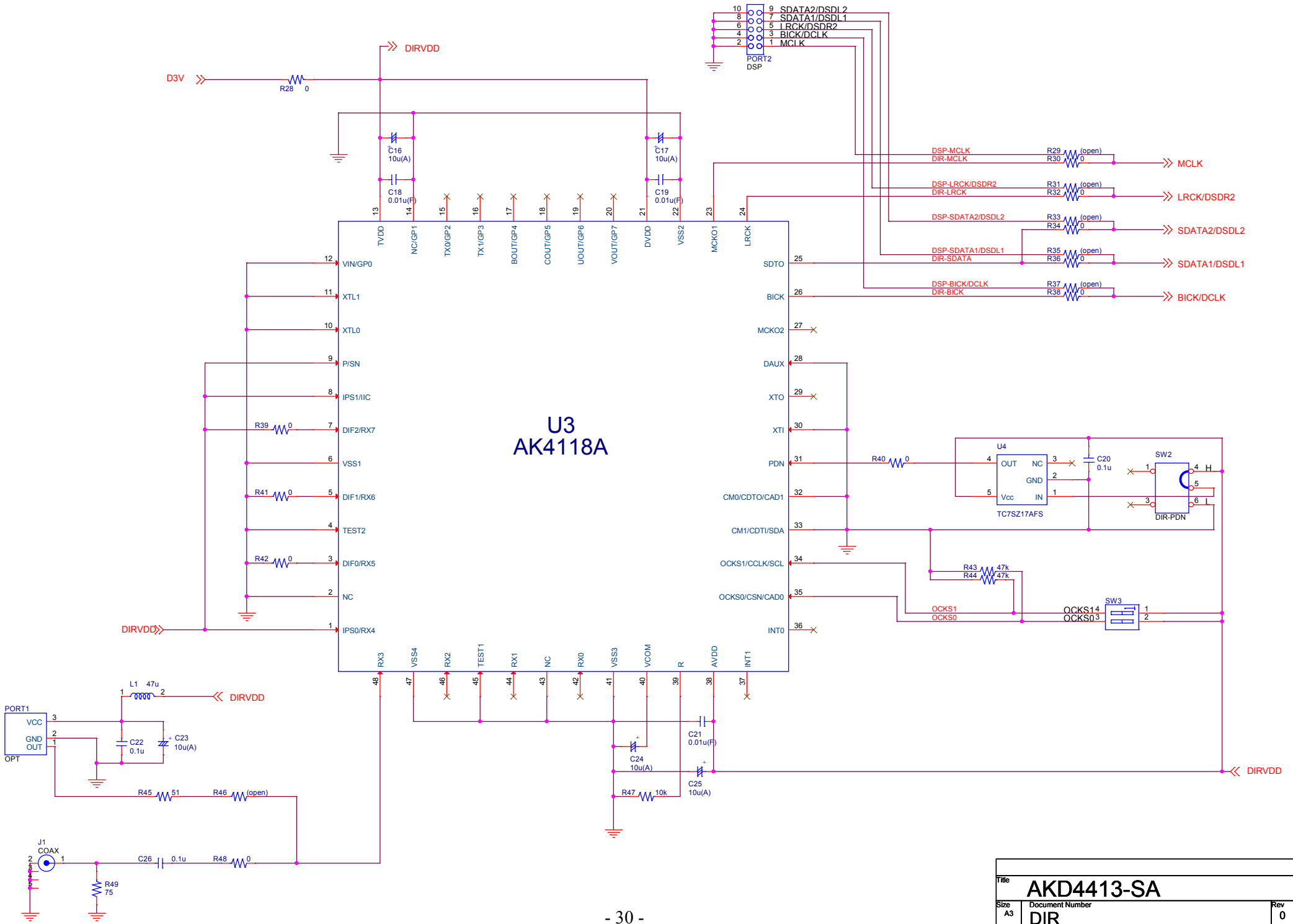

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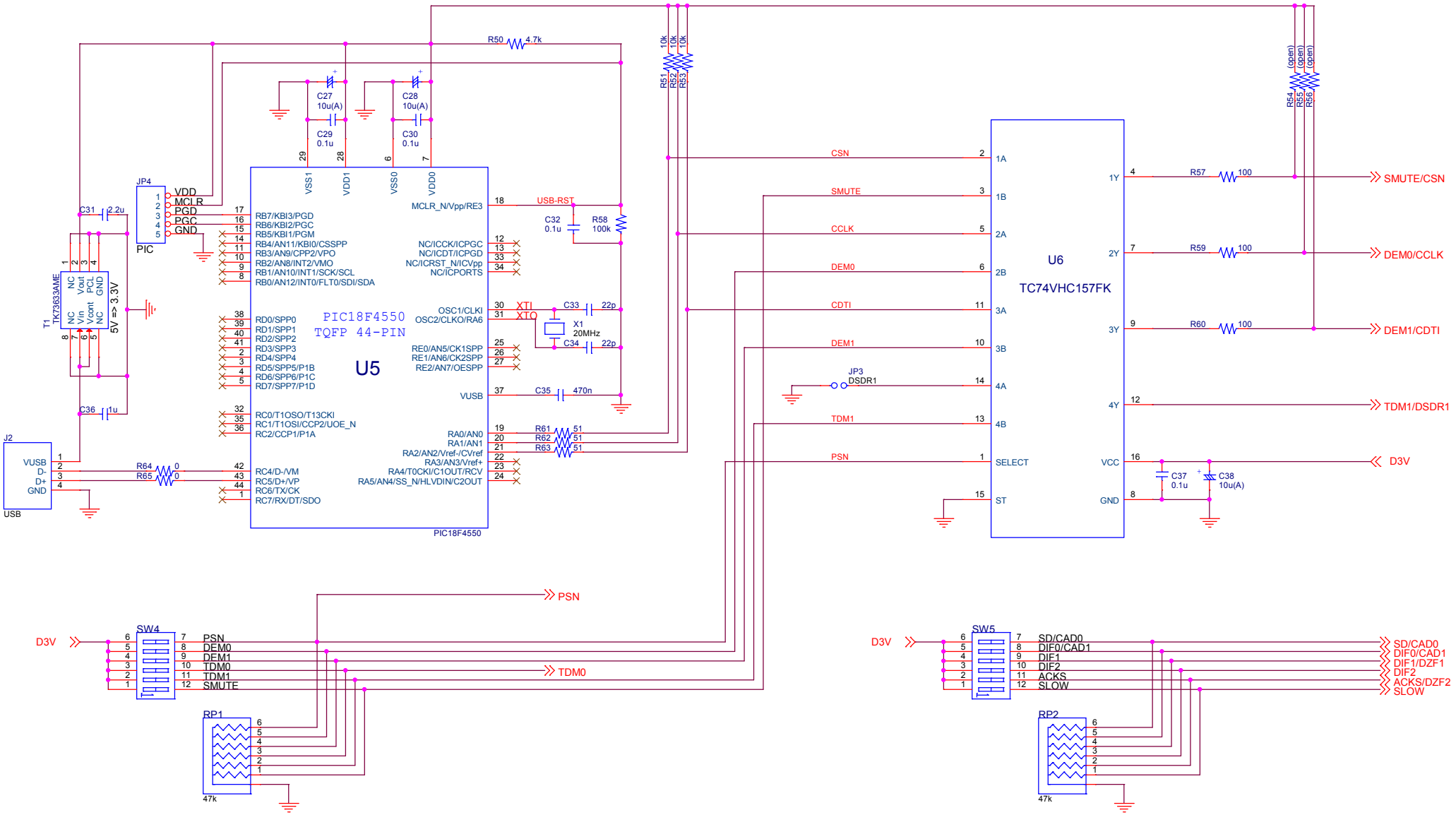

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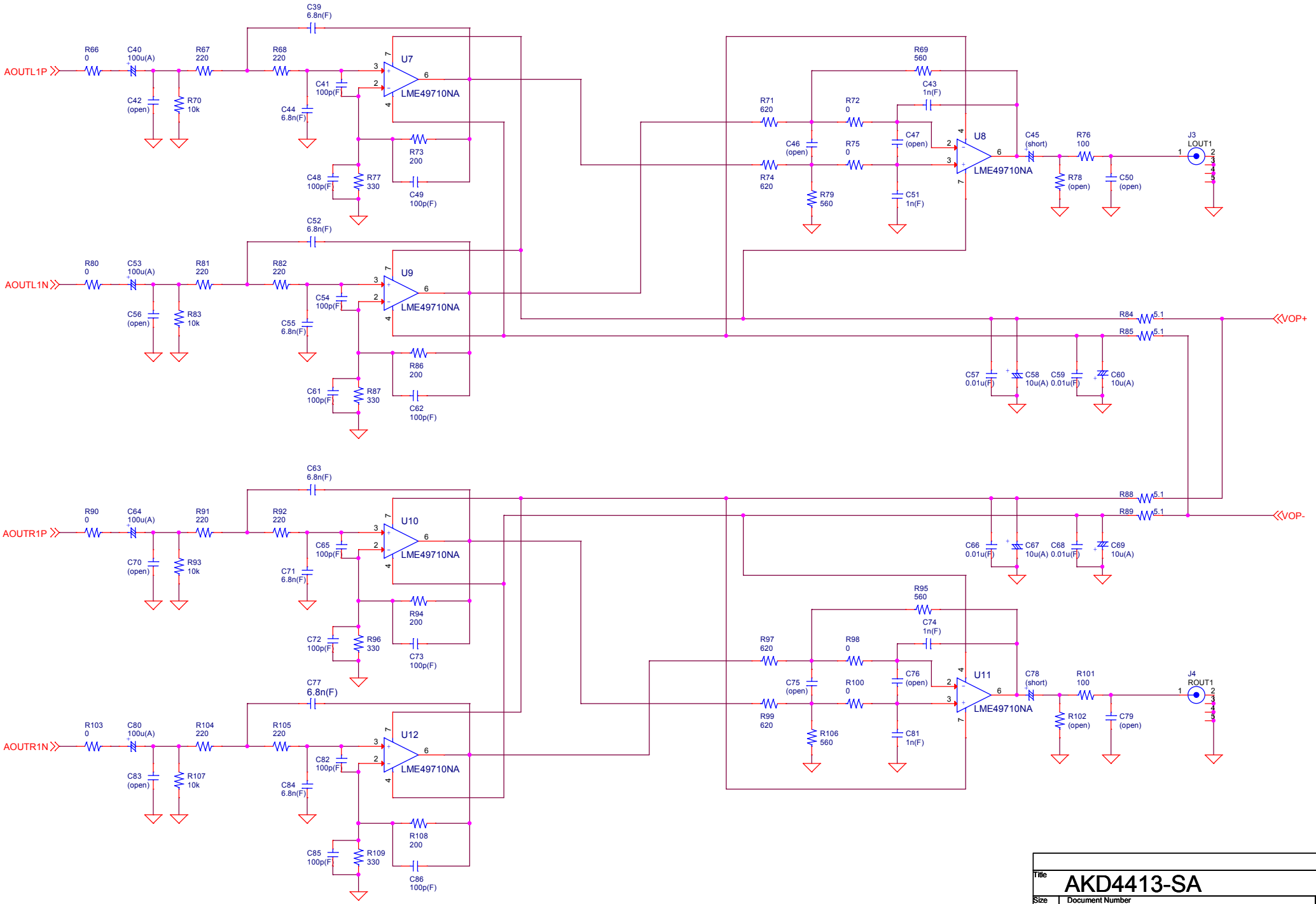

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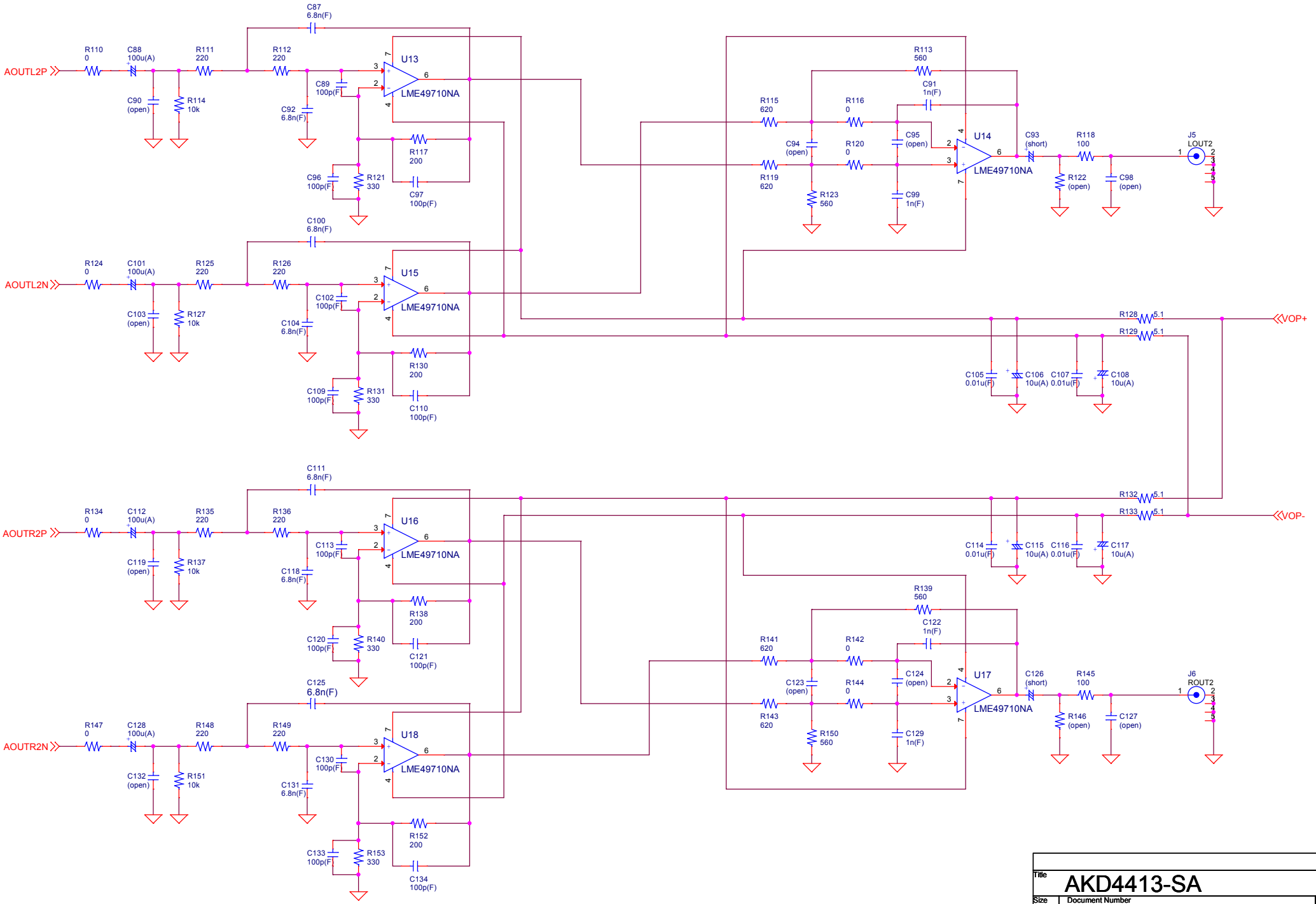

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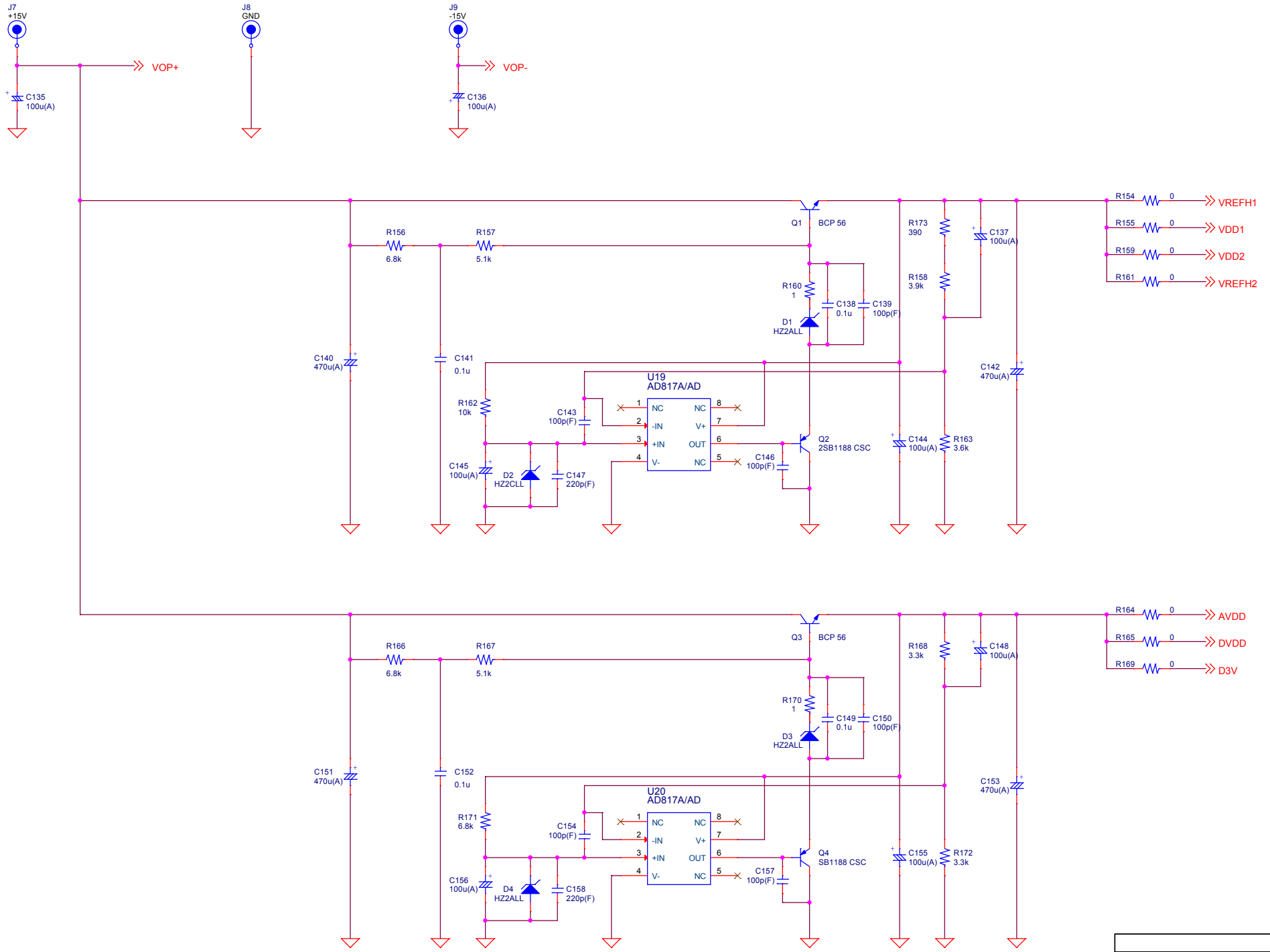

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