AKD4490R-A

AK4490R Evaluation Board Rev.0

1. General Description

The AKD4490R-A is an evaluation board for the AK4490R (Premium 32-bit 2ch stereo DAC) that supports Network-Audios, USB-DAC, Car-Audio Systems. It integrates differential output low pass filters, allowing quick evaluation with digital audio interface.

■ Ordering Guide

AKD4490R-A -- Evaluation Board for the AK4490R
(A USB I/F board for IBM-AT compatible computers and control software are included in this package.)

2. Function

- **Low Pass Filters (LPF) for Pre-amplifier Outputs**
- **Digital Audio Interface (AK4118A)**
- **10-pin Header for Serial Control (AK4490R)**

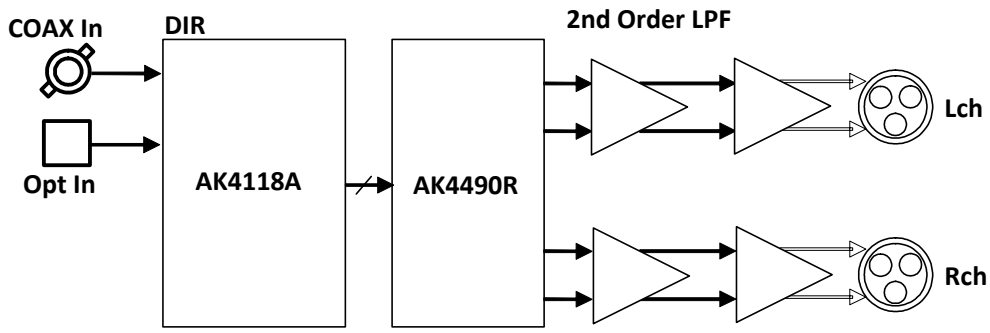


Figure 1. AKD4490R-A Block Diagram (Note 1)

Note 1. Circuit schematics are attached at the end of this document.

3. Board Appearance

■ Appearance Diagram

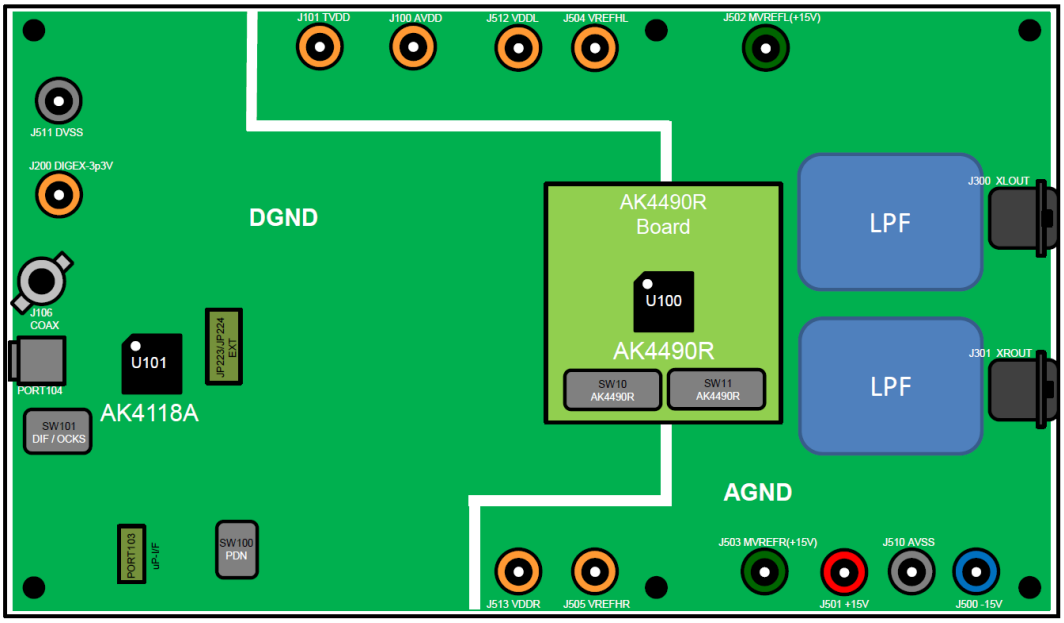


Figure 2. AKD4490R-A Outline View

■ Description

(1) Connectors for Power Supply and GND
(J501/J500/J100/J101/J512/J513/J504/J505/J502/J503/J510/J511/J200)
(+15V, -15V, AVDD, TVDD, VDDL, VDDR, VREFHL, VREFHR, MVREFL(+15V), MVREFR(+15V), AVSS, DVSS, DIGEXT-3p3V)
Connectors for power supply and the ground
Refer to the "Power Supply Connections" for details.

(2) SPDIF Input Connectors (J106 / BNC Connector, PORT104 / Optical Connector)
Input a SPDIF signal to the AK4118A.
Set the JP108 jumper pin to 'Up' side when using the J106 (BNC Connector) jack.
Set the JP108 jumper pin to 'Down' side when using the PORT104 (Optical Connector).

(3) Analog Output Terminals (J300 / J301, XLR Connector)
Differential Analog Output Connector

(4) AK4490R (PCB mounted on CN1, CN2, CN3 and CN4 connectors.)
The AK4490R is a premium 32-bit 2ch DAC.
Board: AKD4490R-A-SUB-48LQFP

(5) AK4118A (U101)
The AK4118A is a digital audio transceiver.
It is used when evaluating sound quality of the AK4490R by SPDIF signals.

(6) µP-IF PORT (PORT103)
10-pin Header for the USB I/F board for AK4490R.
Connect the USB I/F board for IBM-AT compatible computers to this port for a connection to a USB port of a PC. Refer to the "Serial Control Mode" for details.

(7) DIP Switches
(Main Board : SW101 / SW200)
(Sub Board (AKD4490R-A-SUB-48LQFP) : SW10 / SW11)
Setting Switches for the AK4490R and the AK4118A.
Upside is "H" (ON) and Downside is "L" (OFF).
Refer to "■ Jumper Pin and DIP Switch Settings" for details.

(8) Toggle Switch (Main Board: SW100)
Setting Switches for the AK4490R and the AK4118A.
Upside is "H" (ON) and Downside is "L" (OFF).

4. Operation Sequence

■ **Operation sequence**

1). Power Supply Connections
2). Evaluation Mode
3). Jumper Pin and DIP Switch Settings
4). Power-up
5). Register control (Serial control)

■ Power Supply Connections

No.	Name	Color	Voltage	Content	Note	Default Setting
J501	+15V	Red	+10 to +15V	MVDD+ (Regulator), Op-Amp	This jack is always needed.	+15V
J500	-15V	Blue	-10 to -15V	Op-Amp	This jack is always needed.	-15V
J502	MVREFL(+15V)	Green	+10 to +15V	MVREFL (Regulator for AK4490R)	These are used when supplying MVREFL/R(+15V) from a MVREF connector for a regulator. Set the JP509 and JP510 jumper pins to “MVREF” side.	Open
J503	MVREFR(+15V)	Green	+10 to +15V	MVREFR (Regulator for AK4490R)		Open
J101	TVDD	Orange	+2.7 to +3.6V	TVDD (AK4490R)	These are used when supplying TVDD, AVDD, VDDL and VDDR from a 1.8V or a 3.3V or a +5V or a EXT connector without a regulator. Set the JP100 and JP101 jumper pins to “REG(3.3V)” side. Set the JP505 and JP506 jumper pins to “+5V” side.	Open
J100	AVDD	Orange	+2.7 to +3.6V	AVDD (AK4490R)		Open
J512	VDDL	Orange	+4.75 to +5.25V	VDDL (AK4490R)		Open
J513	VDDR	Orange	+4.75 to +5.25V	VDDR (AK4490R)		Open
J504	VREFHL	Orange	+4.75 to +5.25V	VREFHL (AK4490R)	These are used when supplying VREFHL/R from a +5V connector without a regulator. Set the JP501 and JP502 jumper pins to “+5V” side.	Open
J505	VREFHR	Orange	+4.75 to +5.25V	VREFHR (AK4490R)		Open
J510	AVSS	Black	0V	Analog Ground	This jack is always needed.	0V
J511	DVSS	Black	0V	Digital Ground	This jack is always needed.	0V

Table 2. Power Supply Connections (Note 2)

Note 2. Each power supply line should be distributed separately from the power supply unit.

■ Evaluation Mode

(1) Evaluation with a DIR (COAX) < Default >

The J106 (COAX) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the J106 (COAX) connector.
Set the JP108 (RX-SEL) jumper pin to 'Up' side (3pin"BNC") , and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open'.

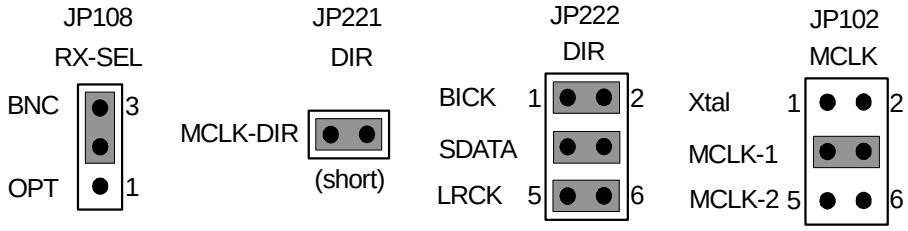


Figure 3. Jumper Pin Settings with DIR

(2) Evaluation with a DIR (OPTICAL)

The PORT104 (OPTICAL) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the PORT104 (OPTICAL) connector.
Set the JP108 (RX-SEL) jumper pin to 'Down' side (1pin"OPT") , and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open'.

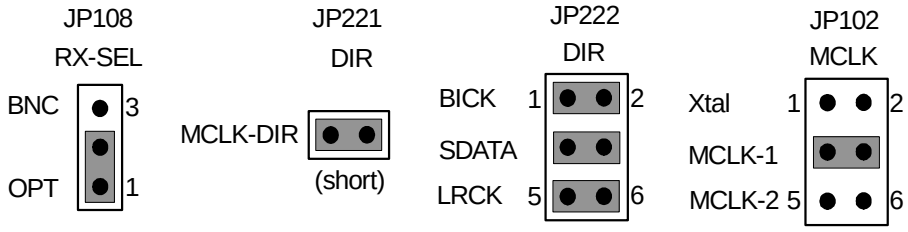


Figure 4. Jumper Pin Settings with DIR

(3) In the case that all interface clocks including the master clock are input externally. (JP223, JP224)

Input all interface clocks including the master clock to the JP223 and JP224.
The JP223 (EXT for MCLK) and the JP224 (EXT for BICK and SDATA and LRCK) jumper ports is used in this mode.
MCLK from the input master clock of the JP223 2pin.
Set the JP221 (DIR: MCLK) jumper pin to 'open'.
BICK, LRCK and SDATA from the input data of the JP224 2pin, 4pin and 6pin.
Set the JP222 (DIR: BICK, SDATA, LRCK) jumper pin to 'open'.

External master clock input :

JP223 : MCLK

Signal	Pin No.		Signal
VSS or open	1	2	MCLK

Note. Jumper settings for JP223. : open

External data and clock input :

JP224 : BICK, SDATA, LRCK

Signal	Pin No.		Signal
VSS or open	1	2	BICK
VSS or open	3	4	SDATA
VSS or open	5	6	LRCK

Note. Jumper settings for JP224. : open

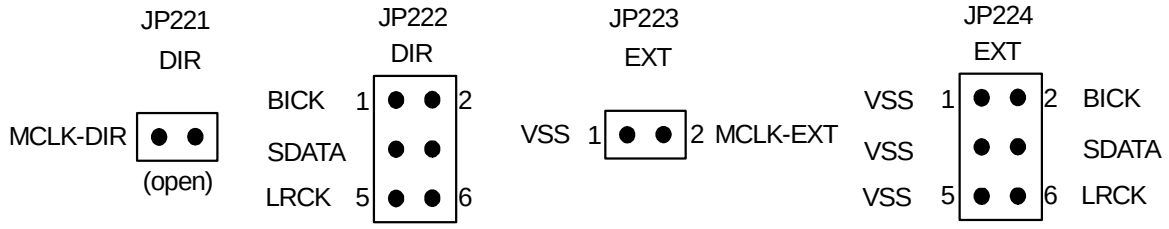


Figure 5. Jumper Pin Settings with External Clocks

■ Jumper Pin and DIP Switch Settings

(1) Jumper Pin Settings

Table 3-1-1. Jumper Settings for power supply [**Main Board**]

No.	Name	Content	Default Setting
JP100	AVDD	AVDD pin input select REG(3.3V): The AVDD pin is supplied from the T100 regulator. REG(1.8V): The AVDD pin is supplied from the T104 regulator. EXT: The AVDD pin is supplied from the J100 (AVDD) connector.	REG(3.3V)
JP101	TVDD	TVDD pin input select REG(3.3V): The TVDD pin is supplied from the T101 regulator. REG(1.8V): The TVDD pin is supplied from the T105 regulator. EXT: The TVDD pin is supplied from the J101 (TVDD) connector.	REG(3.3V)
JP501	VREFHL	VREFHL pin input select REG: The VREFHL pin is supplied from the VREFHL regulator. +5V: The VREFHL pin is supplied from the J504 (VREFHL) connector.	REG
JP502	VREFHR	VREFHR1 pin input select REG: The VREFHR pin is supplied from the VREFHR regulator. +5V: The VREFHR pin is supplied from the J505 (VREFHR) connector.	REG
JP509	MVREFL(+15V)	MVREFL(+15V) power supply for VREFHL1 regulator input select MVDD+: The power supply (MVREFL) for VREFHL1 regulator is supplied from the J501 (+15V) connector. MVREF: The power supply (MVREFL) for VREFHL1 regulator is supplied from the J502 (MVREFL(+15V)) connector.	MVDD+
JP510	MVREFR(+15V)	MVREFR(+15V) power supply for VREFHR1 regulator input select MVDD+: The power supply (MVREFR) for VREFHR1 regulator is supplied from the J501 (+15V) connector. MVREF: The power supply (MVREFR) for VREFHR1 regulator is supplied from the J503 (MVREFR(+15V)) connector.	MVDD+
JP505	VDDL	VDDL pin input select REG: The VDDL pin is supplied from the T500 regulator. +5V: The VDDL pin is supplied from the J512 (VDDL) connector.	REG
JP506	VDDR	VDDR pin input select REG: The VDDR pin is supplied from the T501 regulator. +5V: The VDDR pin is supplied from the J513 (VDDR) connector.	REG
JP500	VSS-SEL1	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	short
JP520	VSS-SEL2	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	short

CL100	Cut-Land	Connection between Analog VSS pattern and Digital VSS pattern. Solder short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open
CL101	Cut-Land	Connection between Analog VSS pattern and Digital VSS pattern. Solder short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	open

Table 3-1-2. Jumper Settings for power supply [**Sub Board : AKD4490R-A-SUB-48LQFP**]

No.	Name	Content	Default Setting
JP16	DVDD-SEL	DVDD power supply for DVDD (the AK4490R) regulator output select short: The DVDD pin (the AK4490R) is supplied from the T102 regulator. open: The DVDD pin (the AK4490R) is LDO output voltage.	short

Table 3-2-1. Jumper Settings for data & clock [**Main Board**]

No.	Name	Content	Default Setting
JP108	RX-SEL	SPDIF signal for AK4118A Upside: SPDIF signal is supplied from the J106 (COAX) connector. Downside: SPDIF signal is supplied from the PORT104 (Optical) connector.	Up side (BNC)
JP102	MCLK	MCLK pin input select MCLK-1 3pin-4pin short: MCLK-1 signal is supplied from the DIR (AK4118A) (JP221) or the external clock (JP223). MCLK-2 5pin-6pin short: MCLK-2 signal is supplied from U200 (MCLKO). Xtal 1pin-2pin short: Xtal MCLK signal is supplied from the crystal oscillator output.	MCLK-1 short
JP221	MCLK-DIR	MCLK pin from DIR (AK4118A) output select short: MCLK signal is supplied from the DIR (AK4118A). open: MCLK signal is open.	Short
JP222	BICK-DIR SDATA-DIR LRCK-DIR	DATA (BICK, SDATA, LRCK) pins from DIR (AK4118A) output select short: DATA signals are supplied from the DIR (AK4118A). open: DATA signals are open.	short

Table 3-2-2. Jumper Settings for data & clock [**Sub Board : AKD4490R-A-SUB-48LQFP**]

No.	Name	Content	Default Setting
JP13	PS4	AK4490R Input data select. H short: SSLOW input data is set to “Hight”. L short: SSLOW input data is set to “Low”. open: WCK (Word clock) input data signal is supplied from 2-pin of JP13.	L short
JP14	DZFL	AK4490R Input/Output data select. short: DIF0 input data is supplied from SW10. open: DZFL output data signal is monitored. (AK4490R)	open
JP15	DZFR	AK4490R Input/Output data select. short: DIF1 input data is supplied from SW10. open: DZFR output data signal is monitored. (AK4490R)	open

Table 3-3. Jumper Settings for control signal [**Sub Board : AKD4490R-A-SUB-48LQFP**]

No.	Name	Content	Default Setting
JP10	PS1 CSN/SMUTE	CSN/SMUTE pin input select CSN: This setting is for Serial Control Mode. SMUTE: This setting is for Parallel Control Mode. (Parallel Control setting by SW10)	CSN Short
JP11	PS2 CCLK/SD	CCLK/TST2 pin input select CCLK: This setting is for Serial Control Mode. SD: This setting is for Parallel Control Mode. (Parallel Control setting by SW10)	CCLK Short
JP12	PS3 CDTI/SLOW	CDTI/TST3 pin input select CDTI: This setting is for Serial Control Mode. SLOW: This setting is for Parallel Control Mode. (Parallel Control setting by SW10)	CDTI short

(2) DIP Switch Setting
Upside is ON (“H”), and Downside is OFF (“L”).

AK4118A Settings : Main Board

[SW101]: Setting of the AK4118A

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF2	Audio I/F Format for AK4118A Refer to **Table 4-1-1.**		H
2	DIF1			L
3	DIF0			L
4	OCKS1	Master Clock setting for AK4118A Refer to **Table 4-1-2.**		L
5	OCKS0			L

Table 4-1. SW101 Setting (AK4118A)

Mode	DIF2 pin	DIF1 pin	DIF0 pin	SDTO	LRCK		BICK		
0	L	L	L	16bit Right justified	H/L	O	64fs	O	
1	L	L	H	18bit Right justified	H/L	O	64fs	O	
2	L	H	L	20bit Right justified	H/L	O	64fs	O	
3	L	H	H	24bit Right justified	H/L	O	64fs	O	
4	H	L	L	24bit Left justified	H/L	O	64fs	O	< Default >
5	H	L	H	24bit I2S	L/H	O	64fs	O	
6	H	H	L	24bit Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit I2S	L/H	I	64-128fs	I	

Table 4-1-1. Audio I/F Format of the AK4118A

Mode	OCKS1	OCKS0	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	< Default >
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	
3	H	H	128fs	192 kHz	

Table 4-1-2. Master Clock Setting of the AK4118A

AK4490R Settings : Sub Board [AKD4490R-A-SUB-48LQFP]

[SW10]: Setting of the AK4490R

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SMUTE	Mute “ON”	Mute “OFF”	L
2	SD	Digital Filter Setting: Refer to **Table 4-2-1**		H
3	SLOW			L
4	DIF0	Audio I/F Format for AK4490R: Refer to **Table 4-2-2**		L
5	DIF1			H
6	DIF2/CAD0			L
		CAD0 pin = “H”	CAD0 pin = “L”	
7	PSN	Parallel Control Mode	Serial Control Mode	L
8	DEM0	De-emphasis Control: Refer to **Table 4-2-3** (In Parallel Control Mode)		H
9	LODE	LDO “ON”	LDO “OFF”	L
10	ACKS/CAD1	Auto Setting Mode	Manual Setting Mode	L
		CAD1 pin = “H”	CAD1 pin = “L”	

Table 4-2. SW10 Setting (AK4490R)

[SW11]: Setting of the AK4490R

No.	Name	ON (“H”)	OFF (“L”)	Default
1	I2C/INV	I2C-Bus Control mode	3-wire Serial Control mode	H
		Output Select: Refer to **Table 4-3-1** (In Parallel Control Mode)		
2	TESTE	Test Mode	Normal Mode	L
3	NC	-	-	L
4	NC	-	-	L
5	NC	-	-	L

Table 4-3. SW11 Setting (AK4490R)

SSLOW	SD	SLOW	Mode	
L	L	L	Sharp roll-off filter	
L	L	H	Slow roll-off filter	
L	H	L	Short delay sharp roll-off filter	< Default >
L	H	H	Short delay slow roll-off filter	
H	L	*	Super Slow roll-off filter	
H	H	*	Low dispersion Short delay filter	

*: Do not care

Table 4-2-1. Digital Filter Setting of the AK4490R (Pin Control Mode)

Mode	DIF2 pin	DIF1 pin	DIF0 pin	Input Format	BICK	
0	L	L	L	16bit LSB justified	≥ 32fs	
1	L	L	H	20bit LSB justified	≥ 40fs	
2	L	H	L	24bit MSB justified	≥ 48fs	< Default >
3	L	H	H	24bit I^2S Compatible	≥ 48fs	
4	H	L	L	24bit LSB justified	≥ 48fs	
5	H	L	H	32bit LSB justified	≥ 64fs	
6	H	H	L	32bit MSB justified	≥ 64fs	
7	H	H	H	32bit I^2 Compatible	≥ 64fs	

Table 4-2-2. Audio I/F Format of the AK4490R (Pin Control Mode)

DEM0	Mode	
L	44.1kHz	
H	OFF	< Default >

Table 4-2-3. De-emphasis Control of the AK4490R (Pin Control Mode)

INV	Lch Out	Rch Out	
L	Lch In	Rch In	< Default >
H	Lch In Invert	Rch In Invert	

Table 4-3-1. Output Select of the AK4490R (Pin Control Mode)

■ Power-up

Upside is ON (“H”), and Downside is OFF (“L”).

[SW100] (PDN): DAC Reset control. It must be set to “H” during operation.
After power-up, the AKD4490R-A must be reset once.
To reset the AKD4490R-A, set the SW100 toggle switch to “L” and power down the AK4490R and the AK4118A.
Then, release the power-down by setting back the SW100 to “H”.

■ Register control (Serial control)

AKD4490R-A can be controlled via USB (serial port).

For the AK4490R:
Connect board to PC using the USB cable (PORT103 - serial) included with the AKD4490R-A.

The control software is packed with the evaluation board.
The software operation sequence is included in the datasheet of each device.

■ Example of evaluation mode:

(1) Normal Mode Sequence : fs=44.1kHz, MCLK=256fs, BICK=64fs, 24bit,Left Justified

■ **Start up Setting**

1: Jumpers and Dip-switches and Toggle-switches are default (Normal Mode) setting.
Note.
Main Board :
SW101: OCKS1-0="LL" (256fs), DIF2-0="HLL" (24bit Left Justified)
Sub Board(AK4490R):
SW10: SMUTE="L", PSN="L", CAD1-0="LL", DEM0="H", LDOE="L"
SW10: I2C="H", TESTE="L"

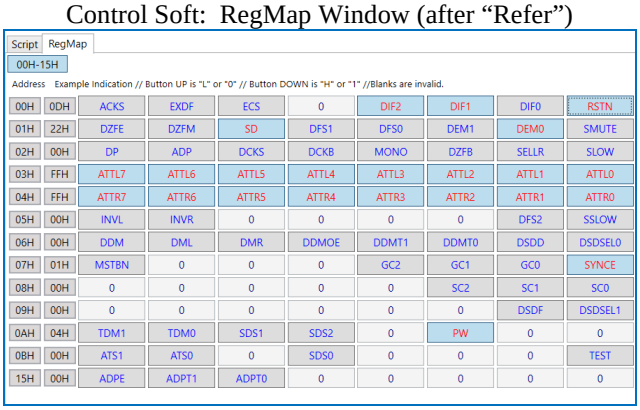
2: Set the SW100 toggle switch to "L".
Then, release the power-down by setting back the SW100 to "H"

SW100
L→H
AK4490R, AK4118A : Used

Table 5-1. Toggle switch setting

3: Control Soft "ak4490r.exe" open.
2-1: Setting : I2C, CAD1-0
2-2: InitPort & Write Default.
2-3: [Script] Tab -> Refer -> "ak4490r-defaultset.txt" Load.
Note. The read file (text file) is packed with the evaluation board.

Control Soft: RegMap Window (after "Refer")



Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized. (default)
1: Normal Operation
DIF[2:0]: Audio Data Interface modes
Initial value is "110" (Mode 6: 32bit MSB justified)

DIF2/1/0 bit: Set Audio Data Interface Mode for Input Digital Data (Normal Single Mode)
000: 16bit, LSB justified

001: 20bit, LSB justified
010: 24bit, MSB justified
011: 24 or 16bit, I2S compatible
100: 24bit, LSB justified
101: 32bit, LSB justified
110: 32bit, MSB justified
111: 32bit, I2S compatible

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SD: Minimum delay Filter Enable
0: Traditional filter
1: Short Delay filter (default)
SLOW: Slow Roll-off Filter Enable
0: Slow Roll-off filter disable (default)
1: Slow Roll-off filter
SSLOW: Super Slow Roll-off (Digital Filter bypass mode) Enable
0: Disable (default)
1: Enable

SSLOW / SD / SLOW bit: Set Digital Filter Setting (1x/2x/4x/8x/16x speed mode)
000: Sharp Roll-off filter
001: Slow Roll-off filter
010: Short Delay Sharp Roll-off filter
011: Short Delay Slow Roll-off filter
100: Super Slow Roll-off filter
101: Super Slow Roll-off filter
110: Low Dispersion Short Delay filter
111: Low Dispersion Short Delay filter

■ Serial Control Mode

The AKD4490R-A (for the AK4490R) should be connected to a PC (IBM-AT compatible) via a USB control box (AKDUSBIF-B) included in this package. The USB control box is connected to a PC with a USB cable and the AKD4490R-A with a 10-pin flat cable. (Note.3, Note.4)

Note 3. The AKD4490R-A accepts only one AKDUSBIF-B at one time. It does not operate if two or more AKDUSBIF-Bs are connected.

Note 4. Connect the 10pin Flat Cable as the red line of the cable is connected to the 1 pin of the 10pin Header of the board.

PORT103 : for the AK4490R

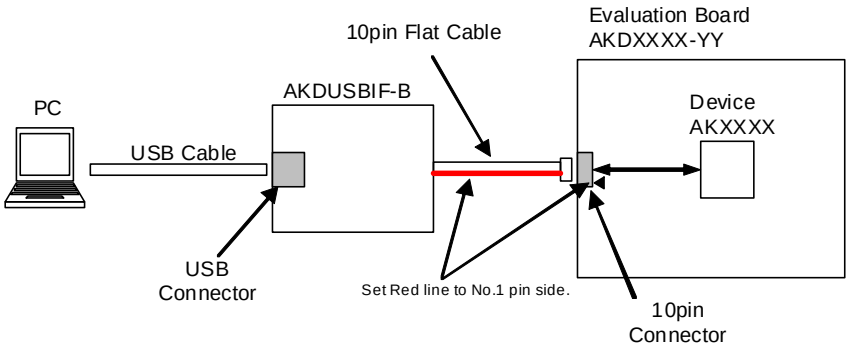


Figure 10. AKDUSBIF-B Connection

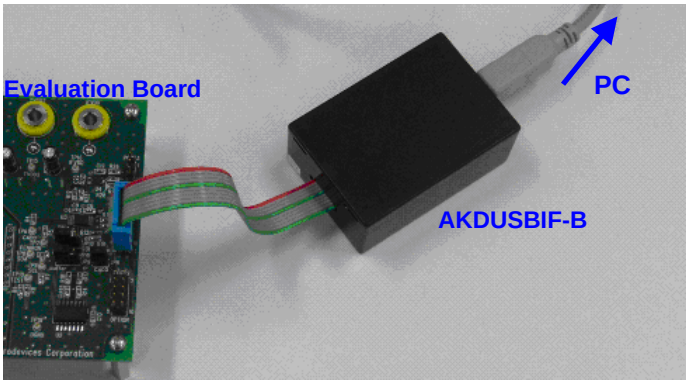


Figure 11. AKDUSBIF-B

Set up the resistor parts. (Control Mode Setting) : For the AK4490R

Control Mode settings. ⋯ Selected Position

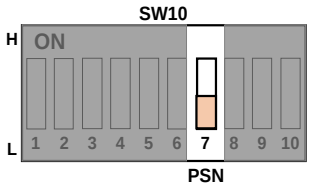
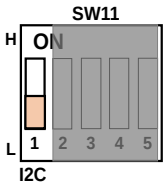
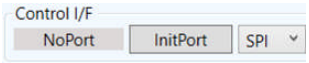
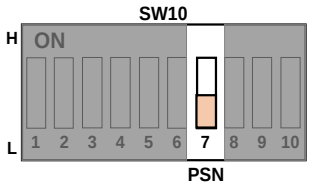
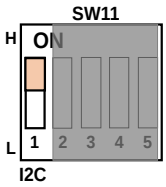
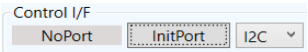
Serial Control Mode	SW10 (AK4490R) (No.7: PSN)	SW11 (AK4490R) (No.1 : I2C)	Control Software (Control I/F)
3-wire	 SW10-No.7 = L	 SW11-No.1 = L	
I²C-Bus	 SW10-No.7 = L	 SW11-No.2 = H	

Table 6-1. Serial control mode setting

When using this evaluation board in serial control mode, settings of the CAD1 pin and the CAD0 pin on the board must match the Chip Address settings of the control software.

⋯ Selected Position

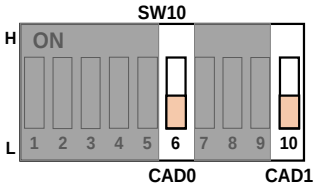
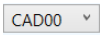
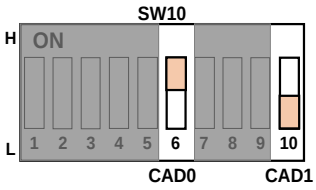
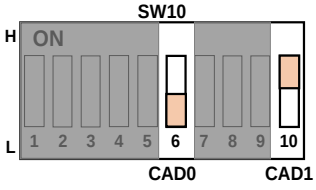
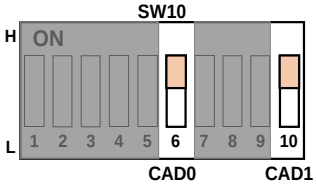
Chip Address	SW10 (AK4490R) (No.10: CAD1, No.6: CAD0)	Control Software (Chip Address)
"00"	 SW10-No.10 = L , SW10-No.6 = L	
"01"	 SW10-No.10 = L , SW10-No.6 = H	
"10"	 SW10-No.10 = H , SW10-No.6 = L	
"11"	 SW10-No.10 = H , SW10-No.6 = H	

Table 6-2. "Chip Address" setting

Set up the jumper pins.

JP10 = CSN short, JP11 = CCLK/SCL short, JP12 = CDTI/SDA short
JP13 = L short, JP14 = open, JP15 = open

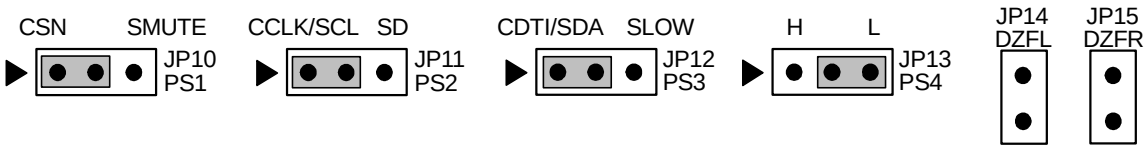


Figure 12. Jumper pin setting

Control Software Manual

■ Evaluation Board and Control Software Settings

(for the AK4490R)

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD4490R-A Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “ak4490r.exe” to open the control program.
6. Begin evaluation by following the procedure below.

[Supported OS]
Windows 7 (32bit) / Windows 10 (64bit)

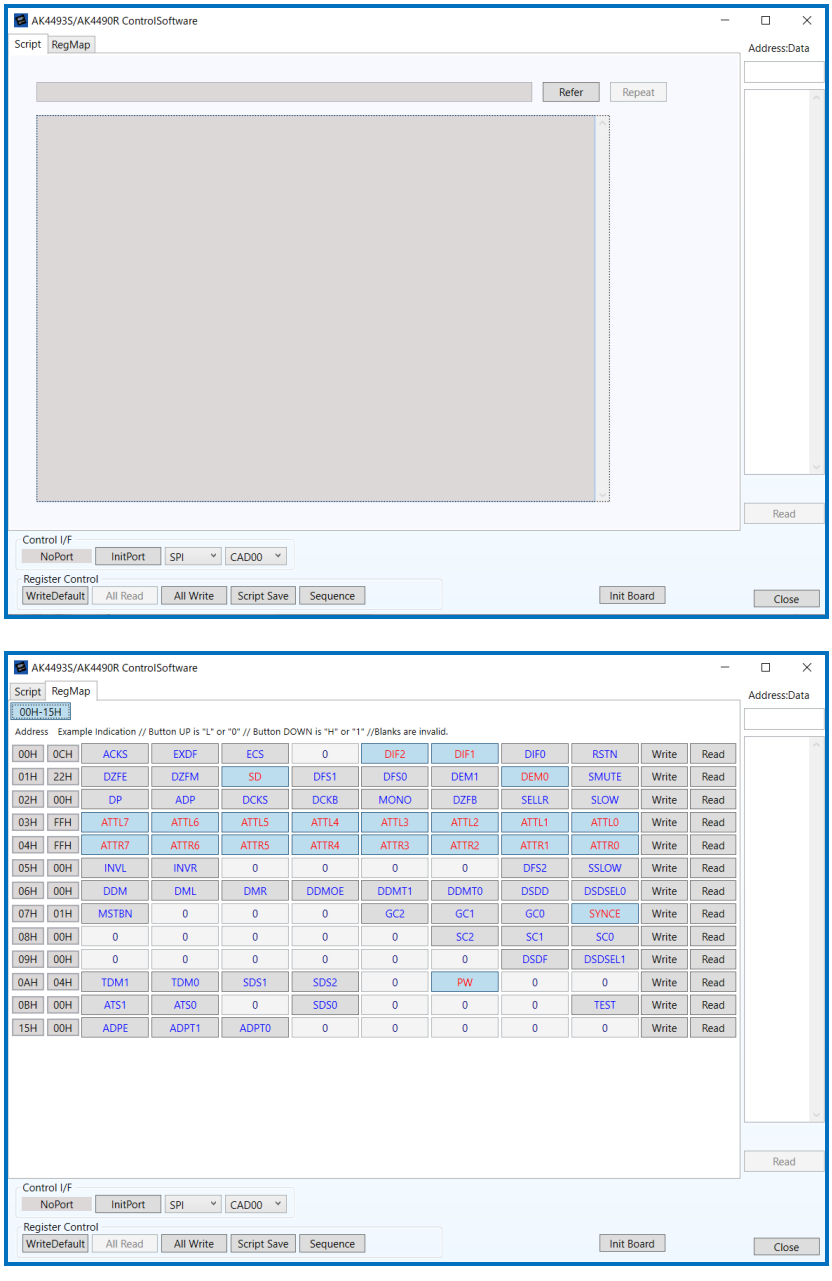
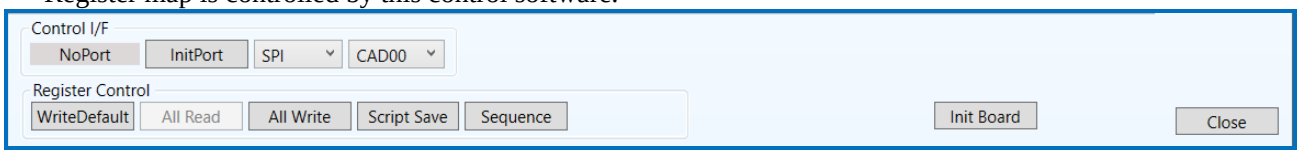


Figure 13. Control Program Window

■ Operation Overview

Register map is controlled by this control software.



Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Box” section for details of each dialog box setting.

1.[Init Port]: Reset the USB port.
Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.

2.[SPI / I2C]: Select up interface of the AK4490R.
This setting can be changed when the PDN pin = “L”.

3.[CAD00 / CAD01 / CAD10 / CAD11]: Select the CAD pin settings.
This setting can be changed when the PDN pin = “L”.

4.[Write Default]: Initialize all registers of the AK4490R.

5.[All Read]: Executes read commands for all registers displayed. (Note 5)

6.[All Write]: Executes write commands for all registers displayed.

7.[Script Save]: Select a file and save all settings of this software.
The saved file can be used as a script.

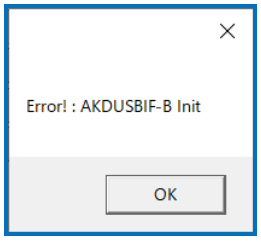
8.[Sequence]: [Sequence] dialog box pops up.

9.[Init Board]: Reset the USB port and the main board.

10.[Close]: Quit the control software.

Note 5. The [All Read] button is only valid when the interface mode for register control is in I^2C bus control mode.

When input dummy command settings to AK4490R and the connection error by the evaluation board to a PC with USB cable, the following Init error message will pop up. Click “OK”.



■ Tab Functions

1. [RegMap] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.
Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

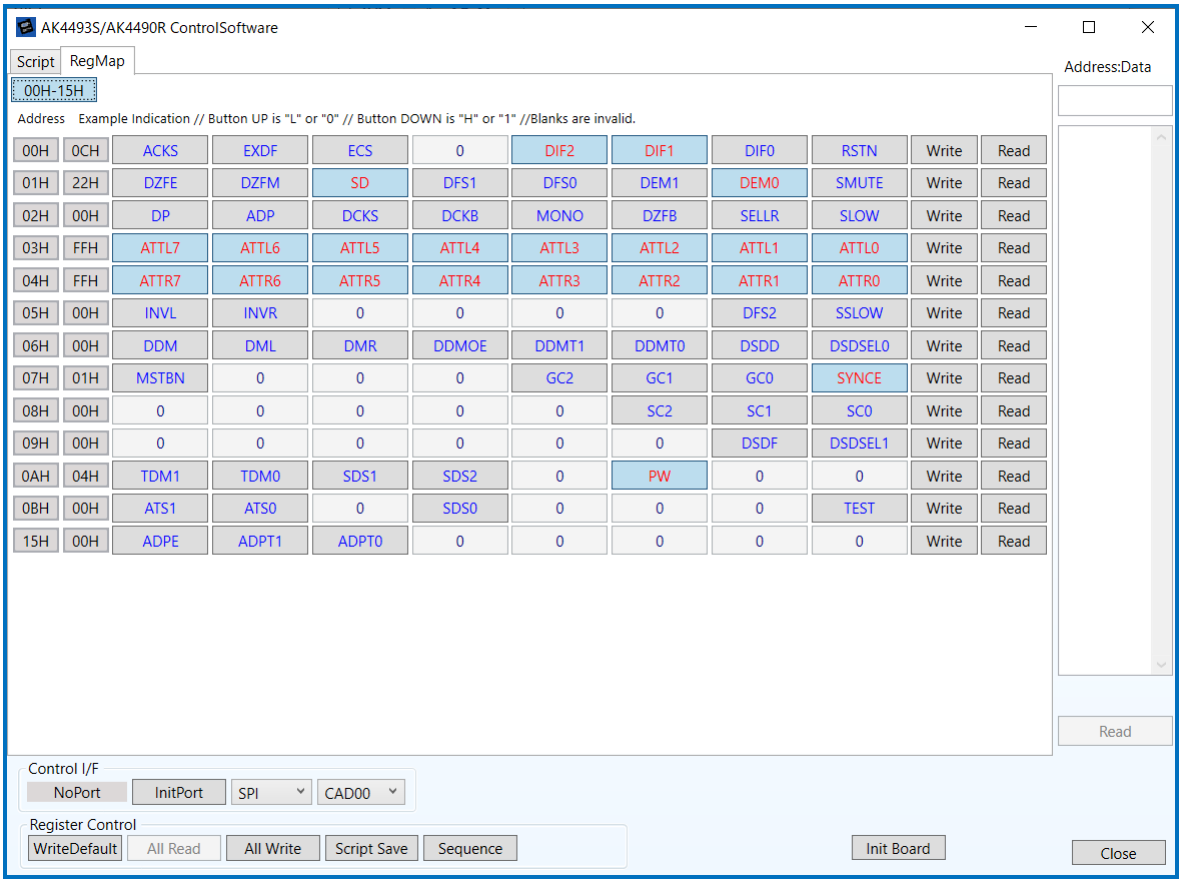


Figure 14-1. RegMap Window

[Write] button: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

Figure 14-2. Register Set Window

[Read] button: Data Read (Only in I²C-bus Control Mode)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.
Button Down indicates “1” and the bit name is shown in red (when read only the bit name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

2. [Script] Tab : Script Function

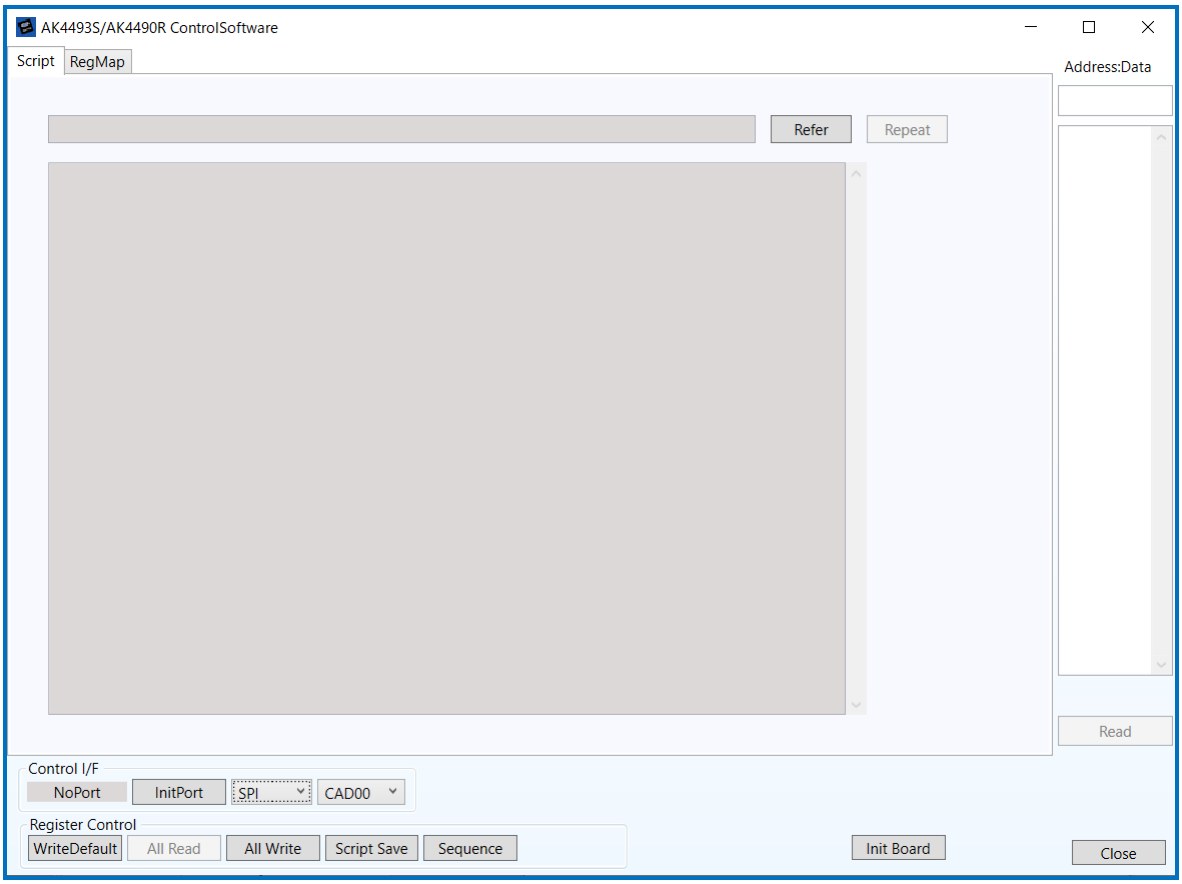


Figure 15. Window of [Script]

[Refer] : Select a script file. The script written on the file will be executed automatically.
[Repeat] : The selected script file will be executed once again.

■ Dialog Box

1. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

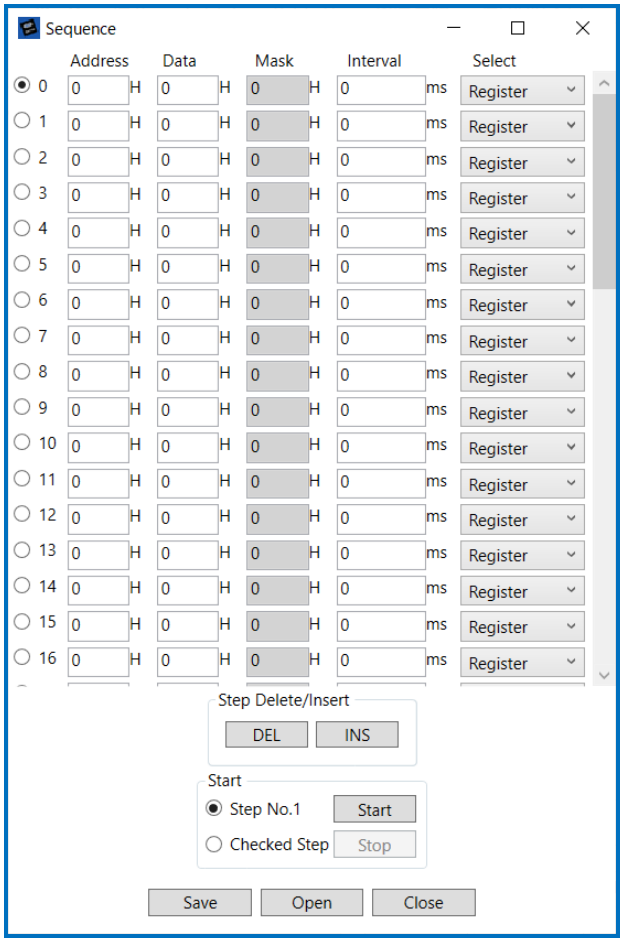


Figure 16. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

   Use [Select] pull-down box to choose commands.
   Corresponding input boxes will be valid.

<Combo Box>
- No_use: Not using this address
- Register: Register write
- Reg(Mask): Register write (Masked)
- Interval: Take an interval
- Stop: Pause the sequence
- End: End the sequence

2. Input Sequence

[Address]: Data Address
[Data]: Write Data
[Mask]: Mask
This value “ANDed” with the write data becomes the input data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

[Start] button : Execute the sequence.
[Stop] button : Pause the sequence.
[Save] button : Save sequence settings as a file. The file name is “*.aks”.
[Open] button : Open a sequence setting file “*.aks”.
[Close] button : Close the dialog box and finishes the process.

Start Sequence: [Start] Functions

[Step No.1] check box : Start at number “0” in the sequence.
[Checked Step] check box : Start from checked number in the sequence.

Revision History

Date (y/m/d)	Manual Revision	Board Revision	Reason	Page	Contents
22/01/01	KM136000	0	First Edition	-	-

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Rev.1

1. Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision APX555 audio analyzer (APX555)
- MCLK : 256fs (44.1 kHz), 256fs (96kHz), 128fs (192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply for AK4493S: AVDD=3.3V, TVDD=3.3V, DVDD=1.8V
  VDDL/R=5V, VREFHL/R=5V
- Pass : DIR → AK4490R → Cannon Connector
- Interface : Internal DIR (44.1 kHz / 96kHz / 192kHz)
- Temperature : Room Temperature
- Operational Amplifiers : OPA1612

fs=44.1kHz : 0dB=5.87Vrms

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	20kHz LPF	111.7 dB	/	111.9 dB
DR	1kHz, -60dB	20kHz LPF	58.0 dB	/	58.0 dB
		20kHz LPF A-weighted	121.0 dB	/	121.0 dB
S/N	“0” data	20kHz LPF A-weighted	121.1 dB	/	121.2 dB

fs=96kHz : 0dB=5.87Vrms

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	40kHz LPF	109.1 dB	/	110.1 dB
DR	1kHz, -60dB	40kHz LPF	56.0 dB	/	56.2 dB
		40kHz LPF A-weighted	121.0 dB	/	121.3 dB
S/N	“0” data	40kHz LPF A-weighted	121.1 dB	/	121.2 dB

fs=192kHz : 0dB=5.87Vrms

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	80kHz LPF	108.5 dB	/	109.1 dB
DR	1kHz, -60dB	80kHz LPF	53.3 dB	/	53.6 dB
		80kHz LPF A-weighted	121.0 dB	/	121.1 dB
S/N	“0” data	80kHz LPF A-weighted	121.1 dB	/	121.1 dB

[Plots]

fs = 44.1 kHz

AK4490R THD+N vs. Input Level
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

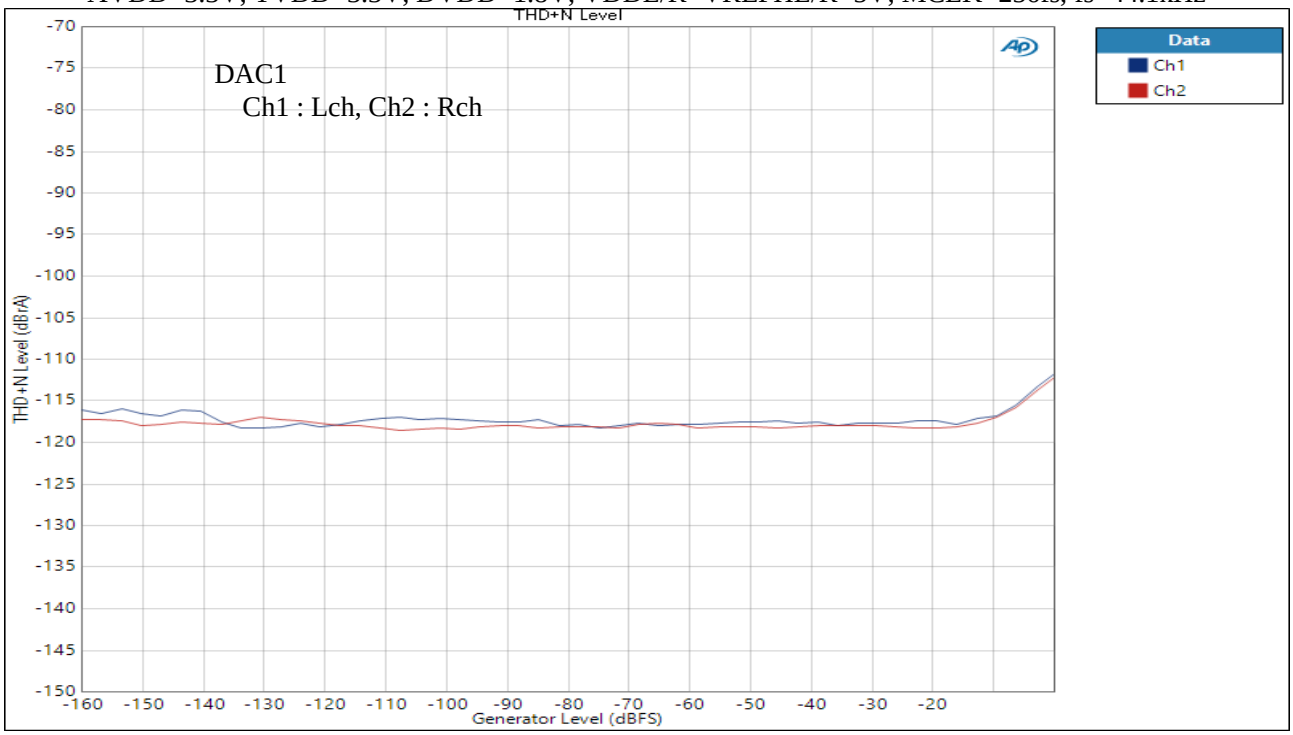


Figure 20-1. THD+N vs. Input Level

AK4490R THD+N vs. Input Frequency
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

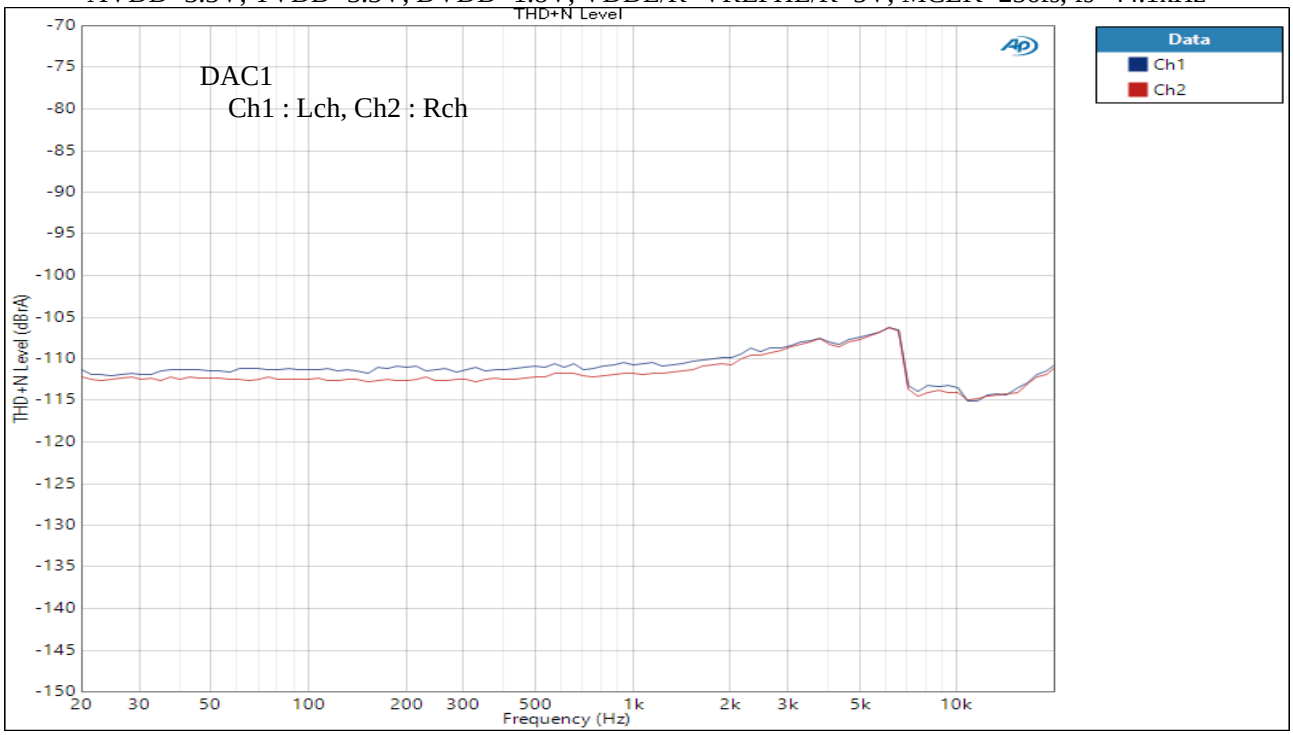


Figure 20-2. THD+N vs. Input Frequency

fs = 44.1 kHz

AK4490R Linearity

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

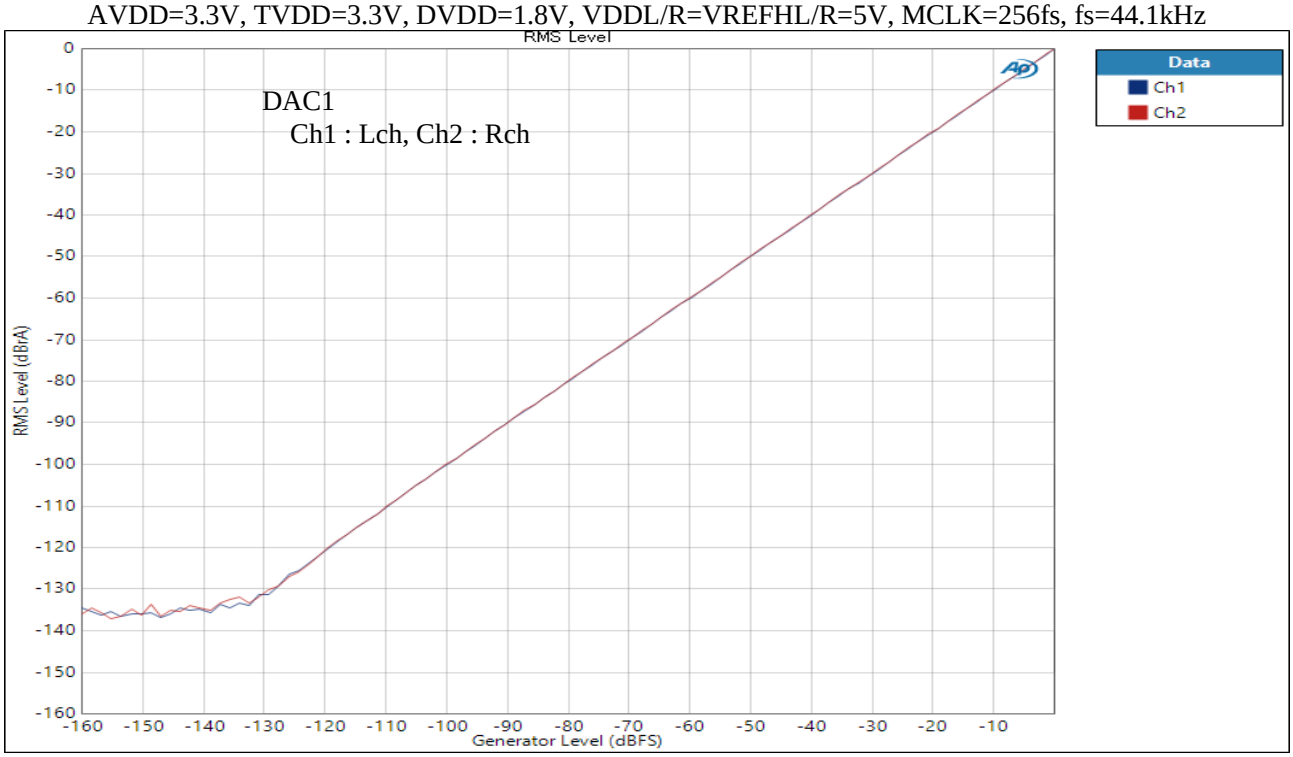


Figure 20-3. Linearity

AK4490R Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

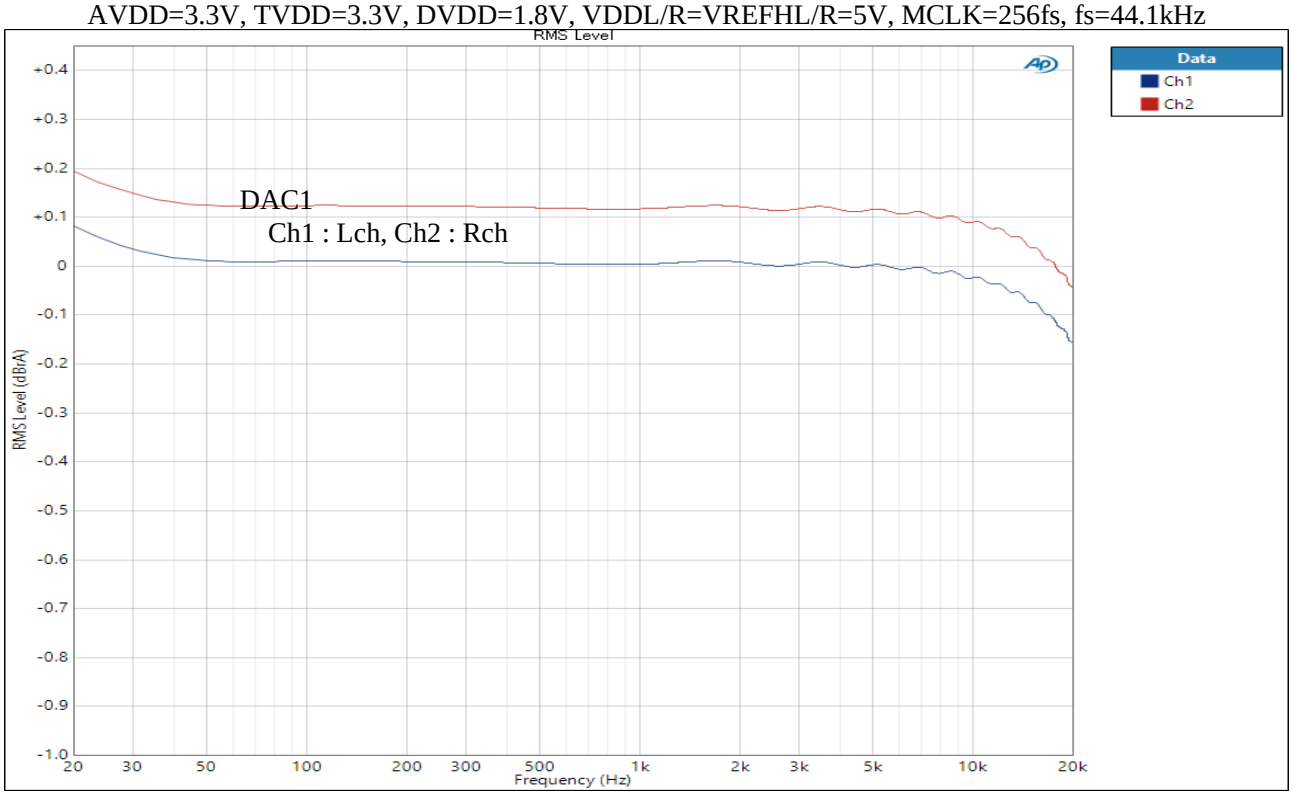


Figure 20-4. Frequency Response

fs = 44.1 kHz

AK4490R Crosstalk

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

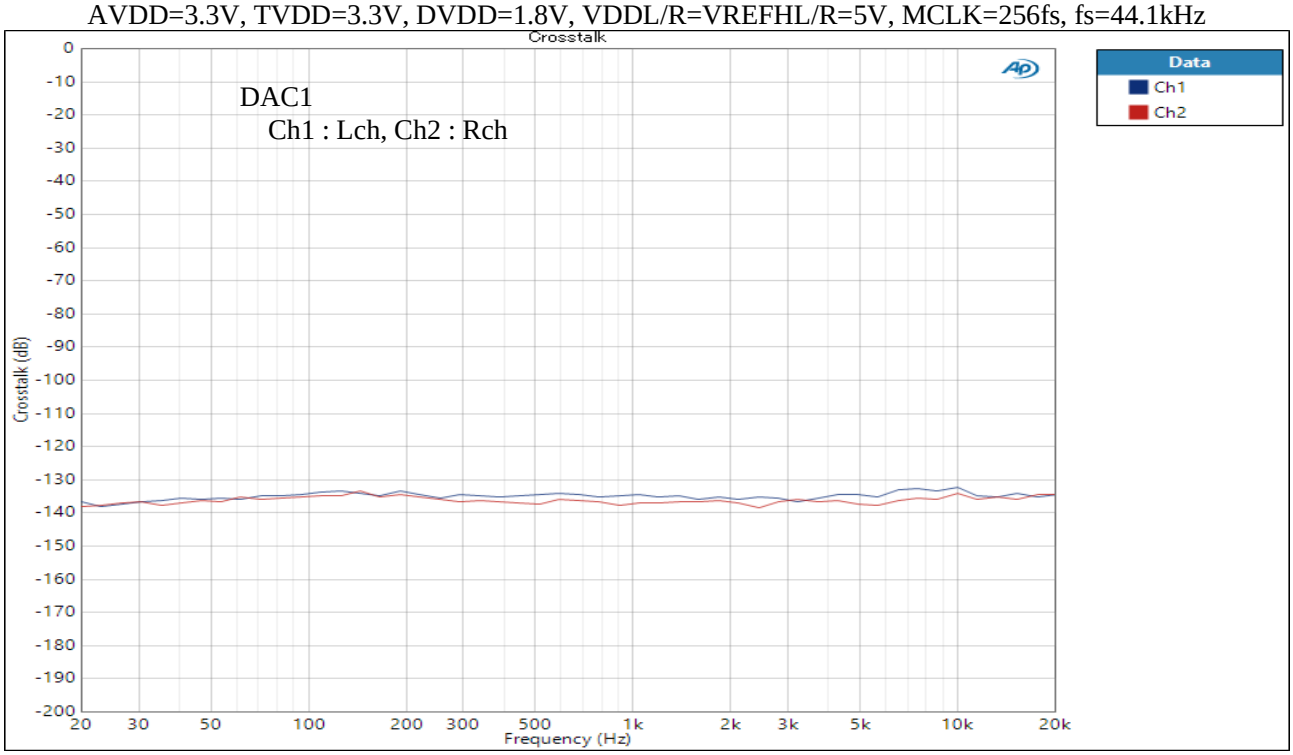


Figure 20-5. Crosstalk

AK4490R FFT (0dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

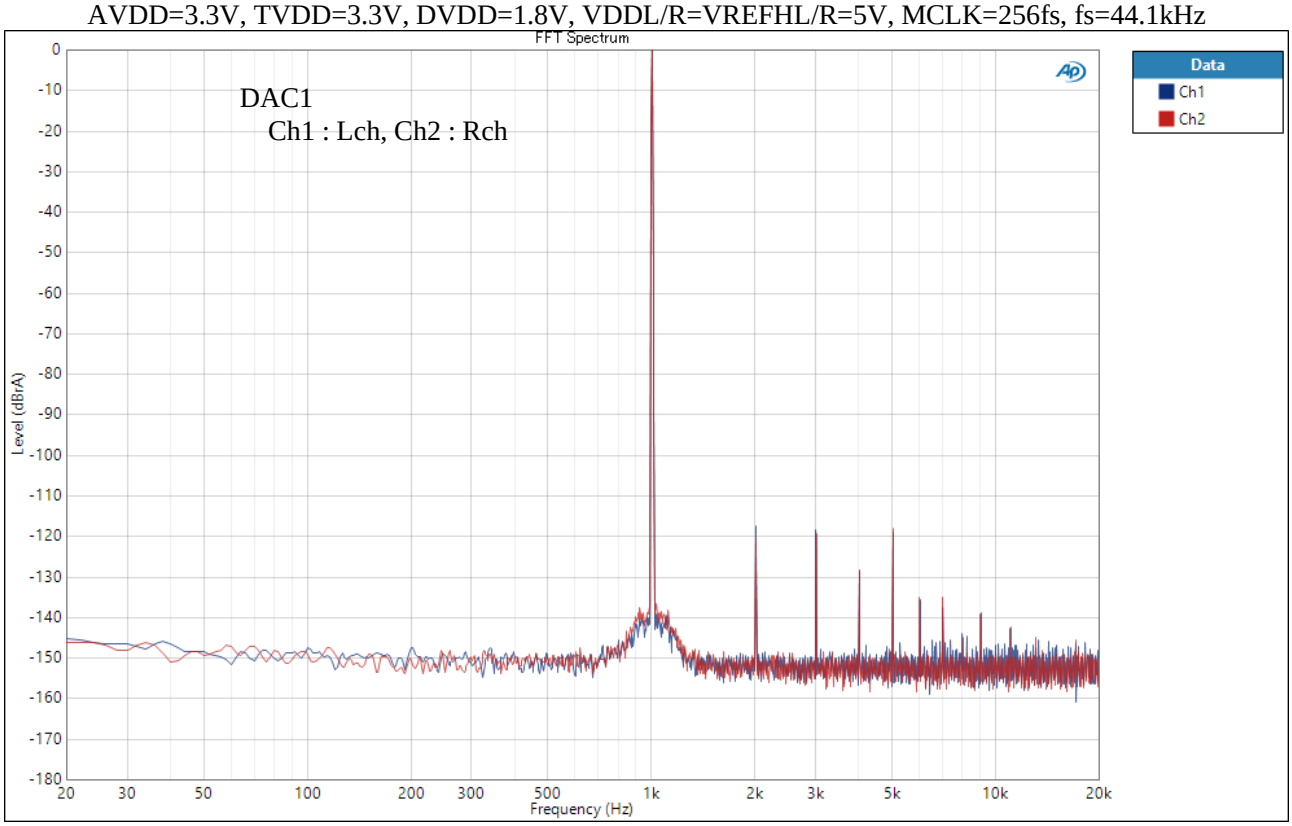


Figure 20-6. FFT (0dBFS Input)

fs = 44.1 kHz

AK4490R FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

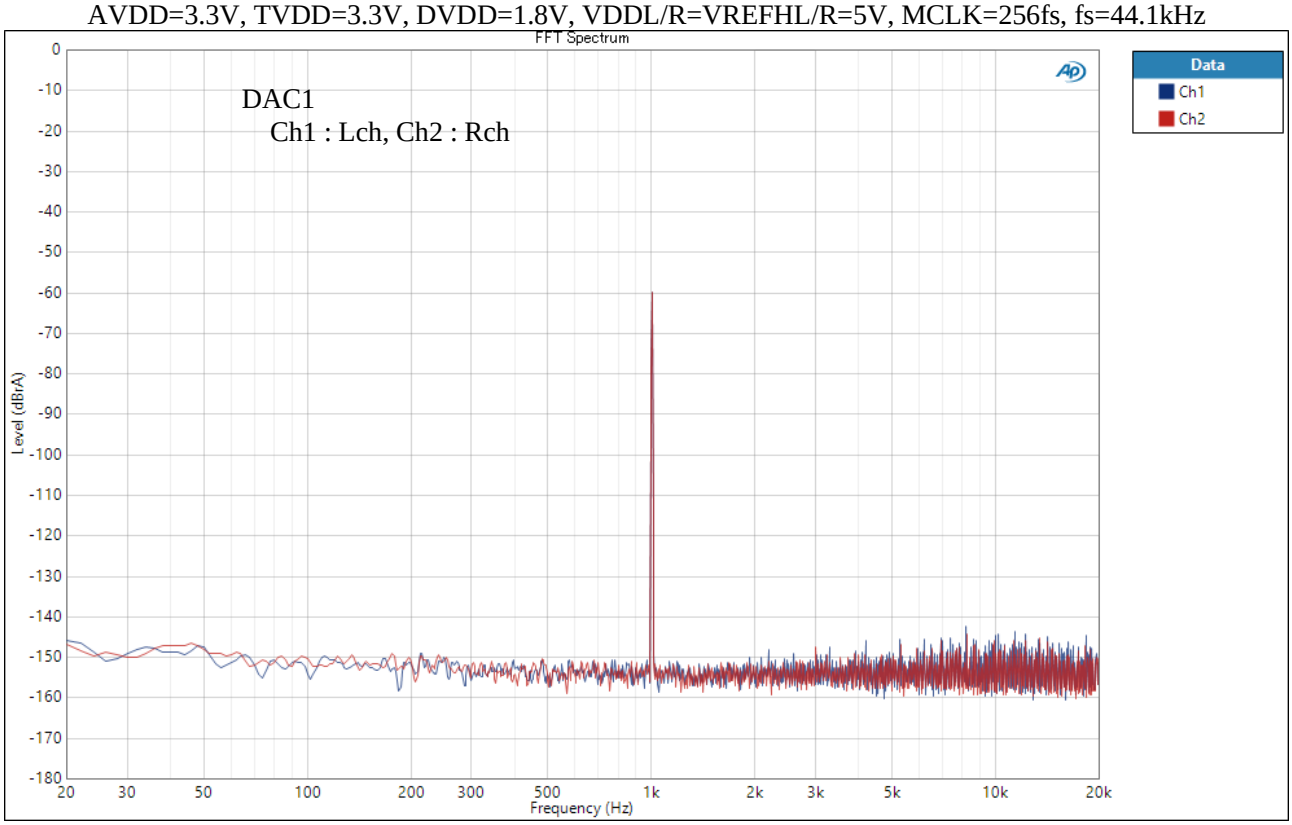


Figure 20-7. FFT (-60dBFS Input)

AK4490R FFT (No Signal Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

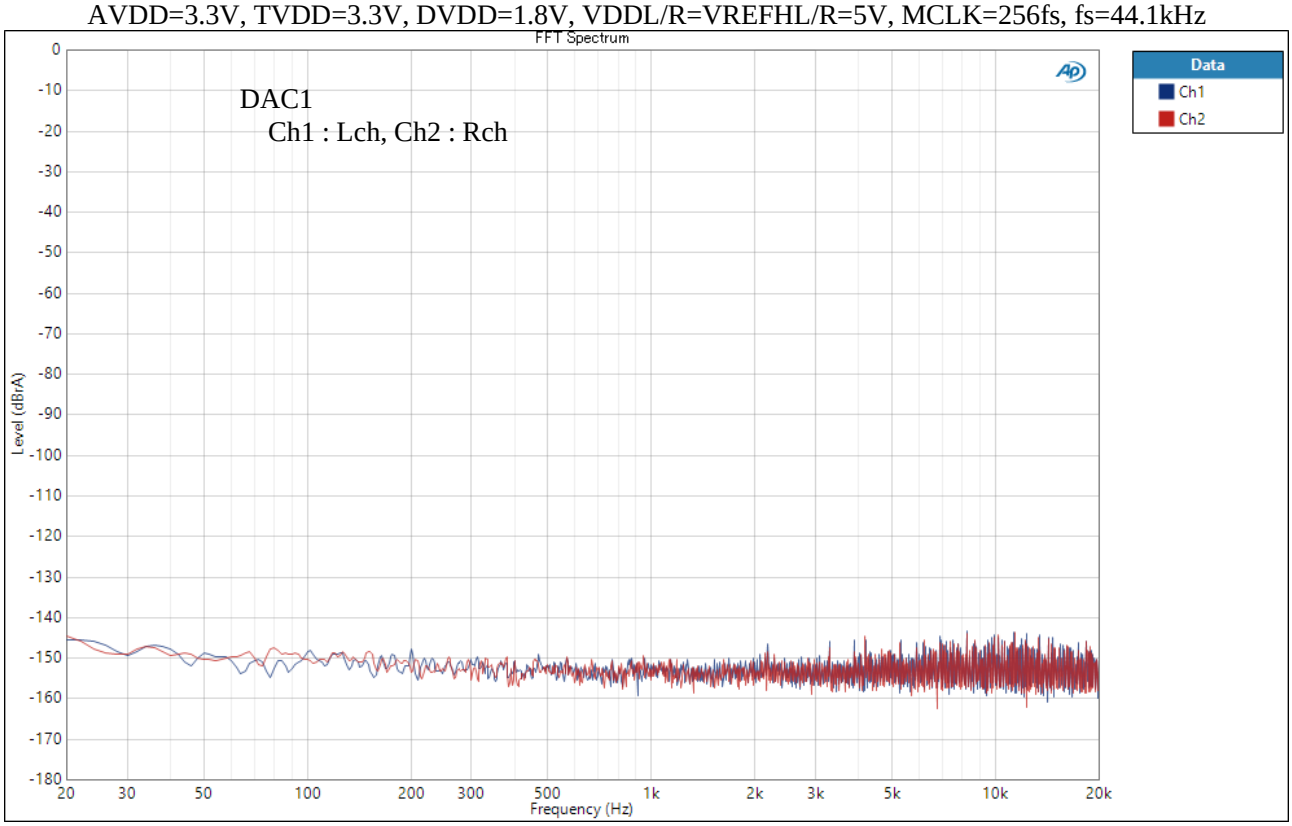


Figure 20-8. FFT (No Signal Input)

fs = 96kHz

AK4490R THD+N vs. Input Level

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

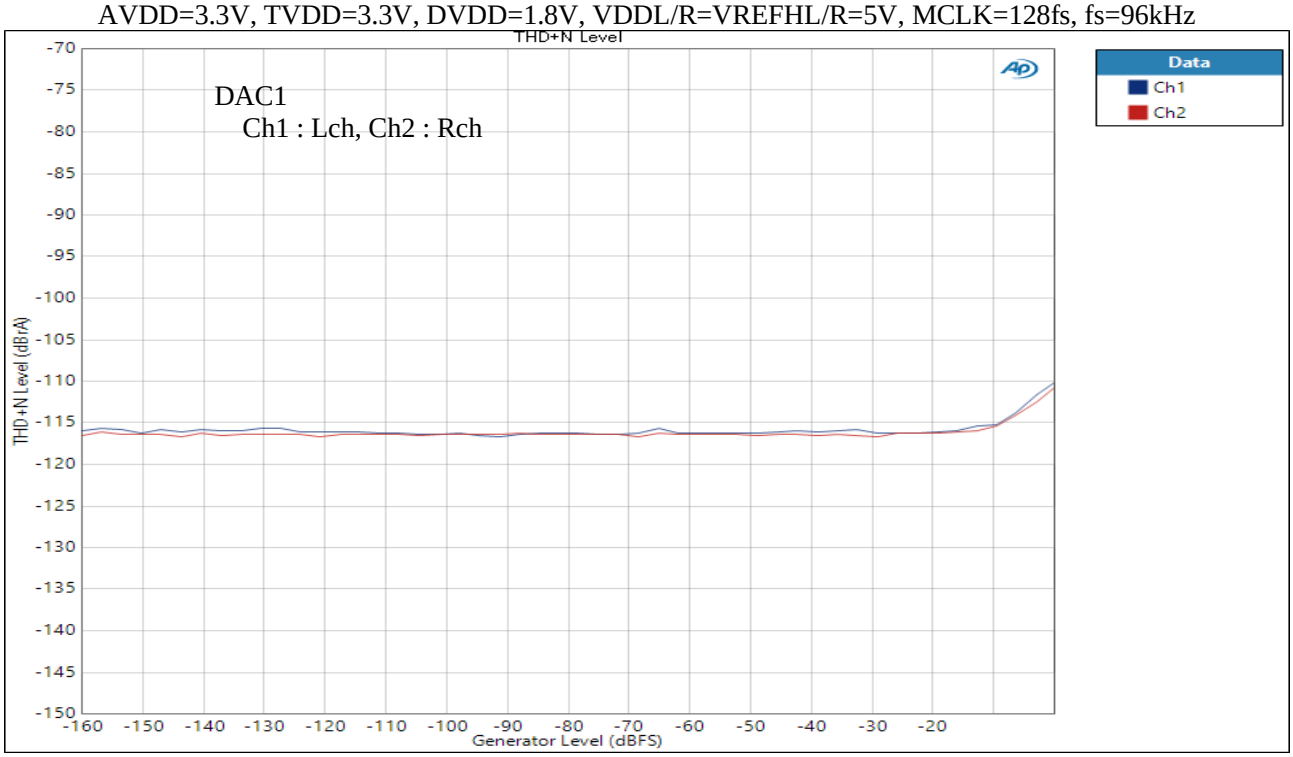


Figure 21-1. THD+N vs. Input Level

AK4490R THD+N vs. Input Frequency

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

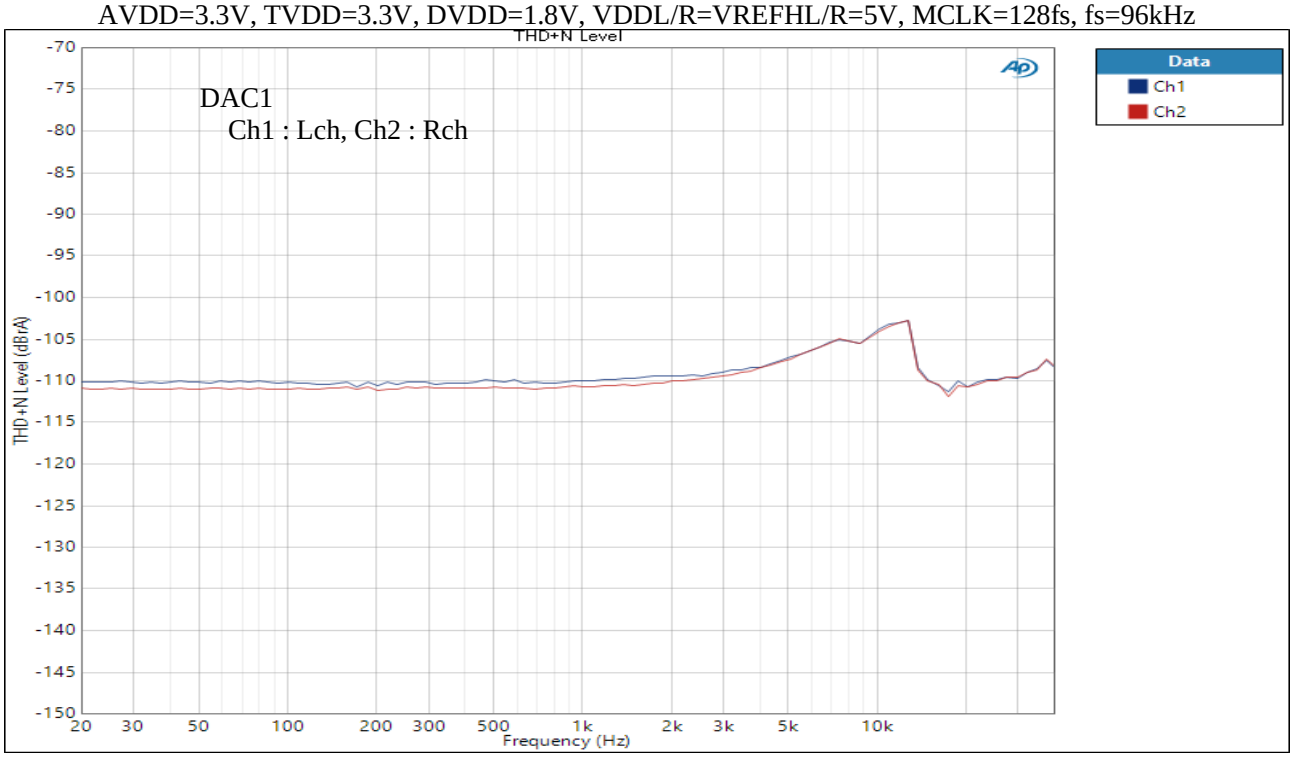


Figure 21-2. THD+N vs. Input Frequency

fs = 96kHz

AK4490R Linearity

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

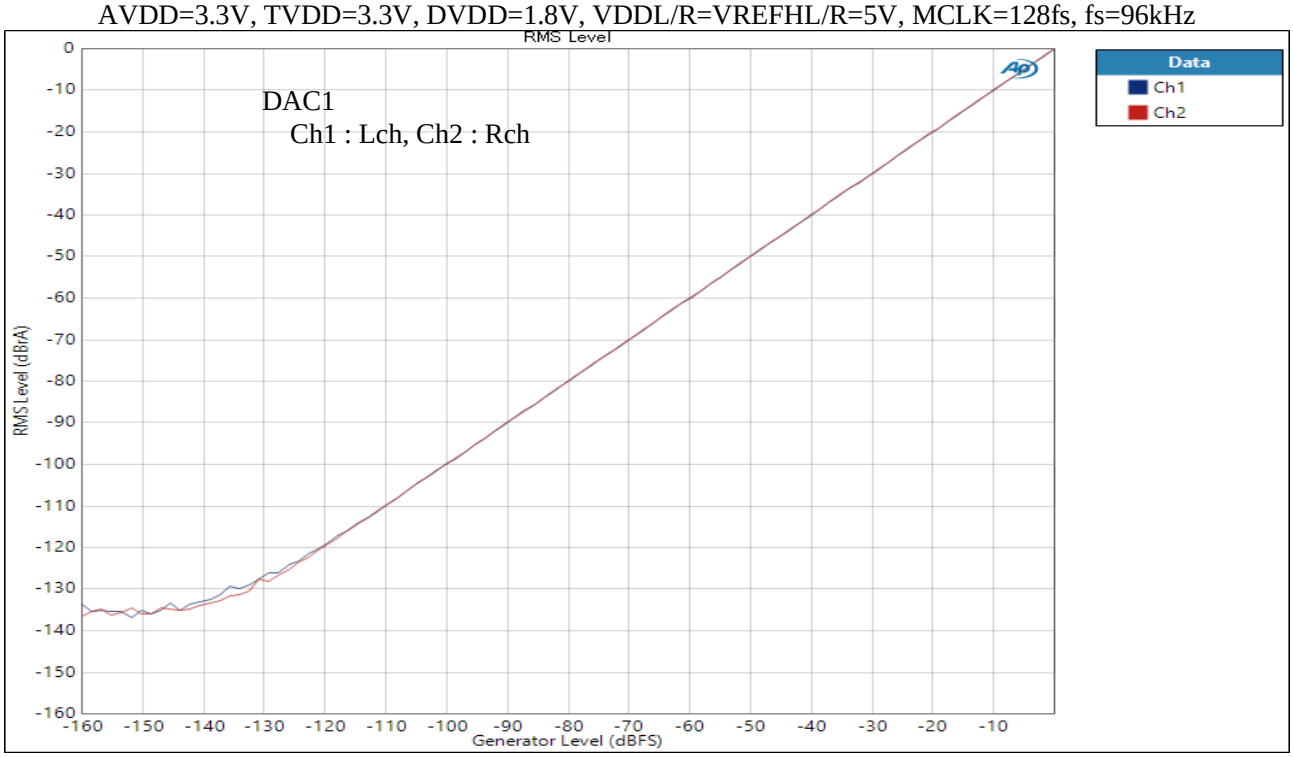


Figure 21-3. Linearity

AK4490R Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

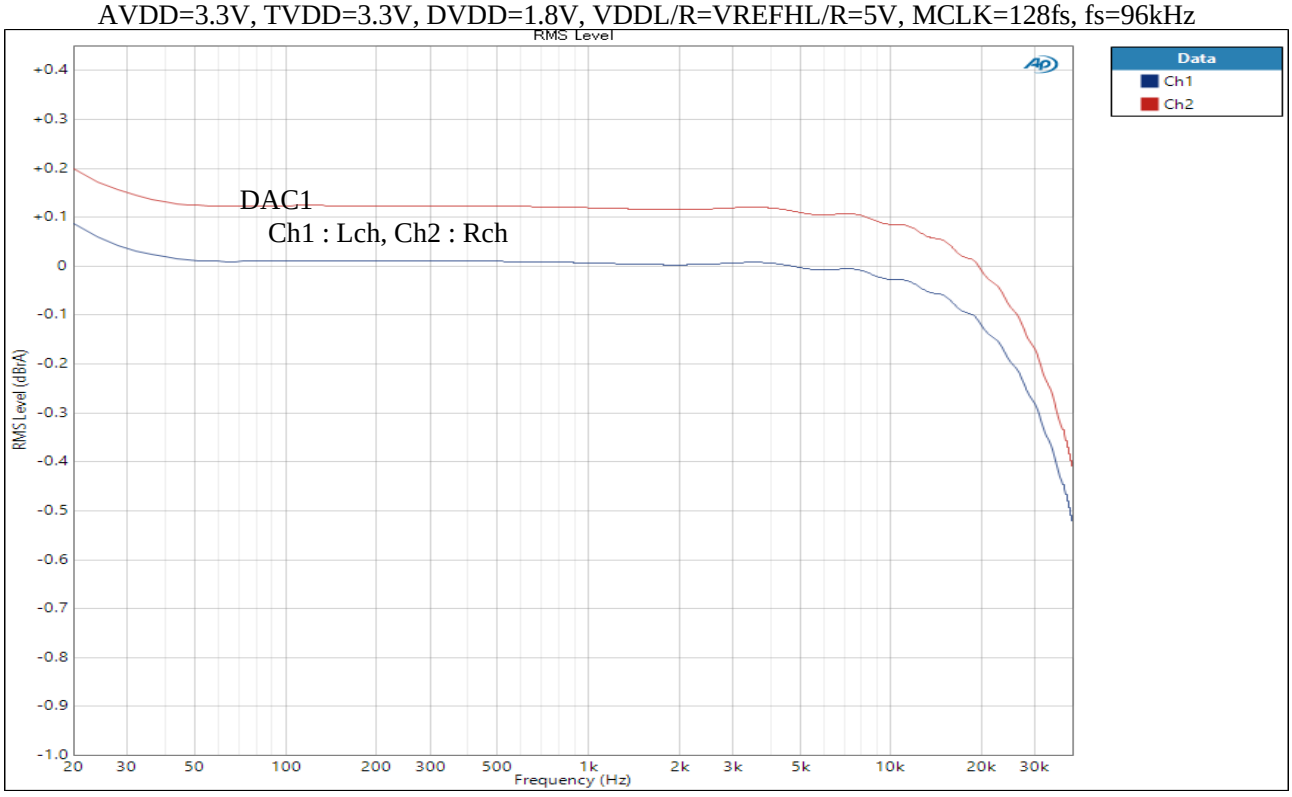


Figure 21-4. Frequency Response

fs = 96kHz

AK4490R Crosstalk

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

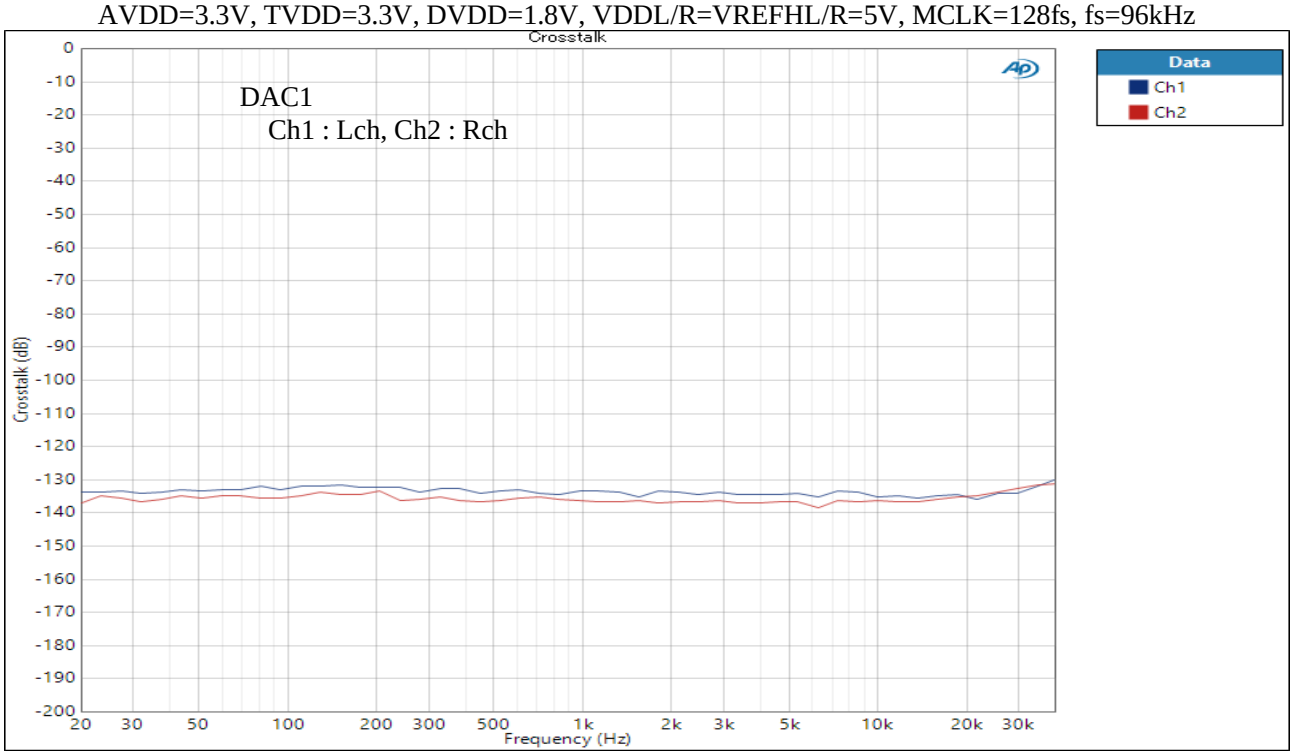


Figure 21-5. Crosstalk

AK4490R FFT (0dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

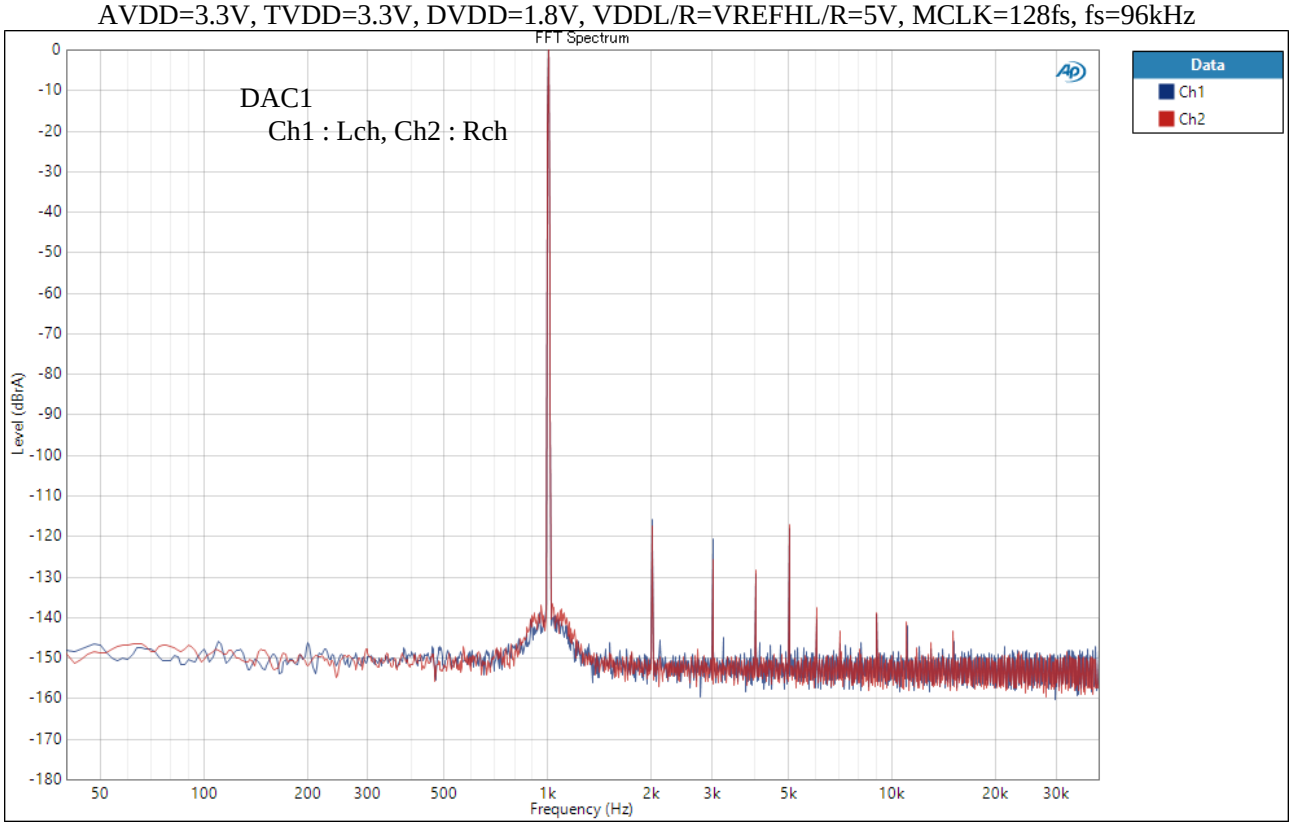


Figure 21-6. FFT (0dBFS Input)

fs = 96kHz

AK4490R FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

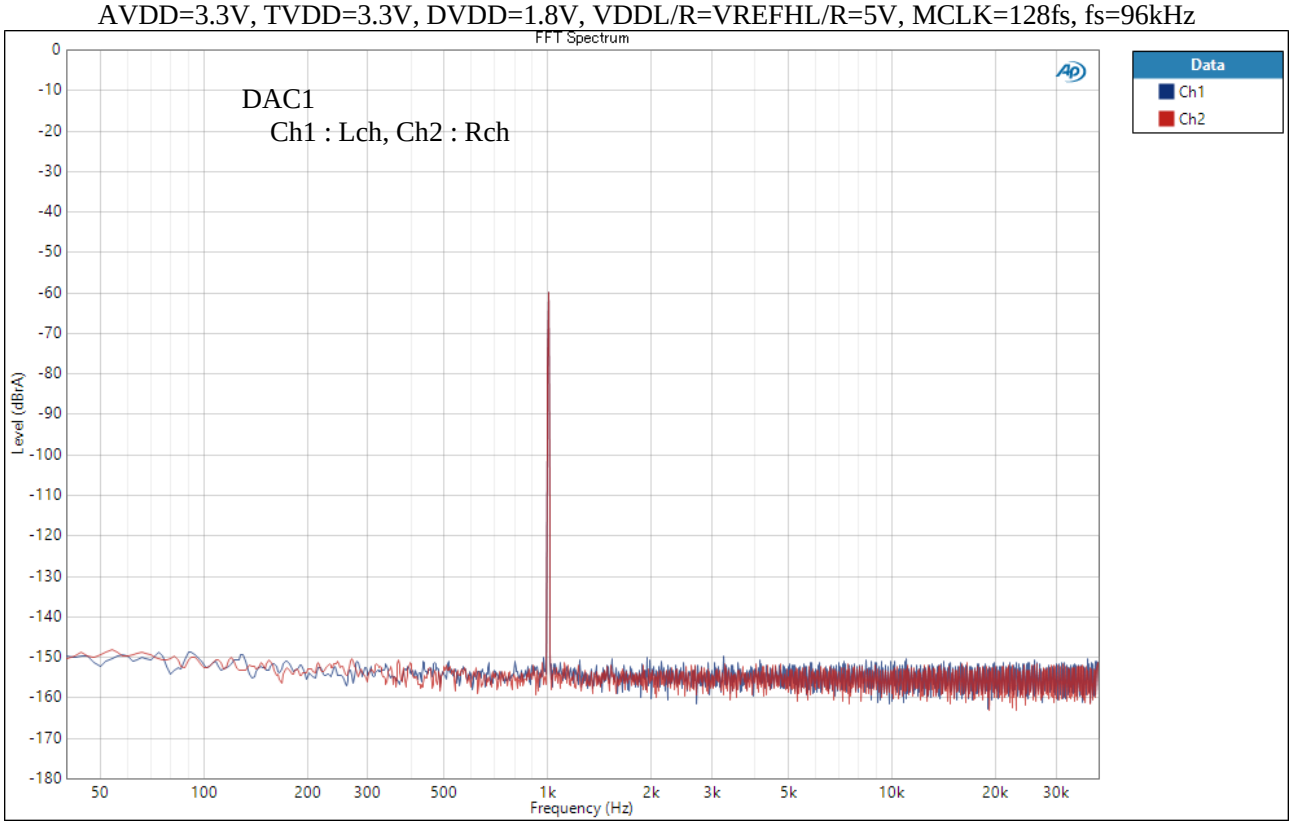


Figure 21-7. FFT (-60dBFS Input)

AK4490R FFT (No Signal Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=96kHz

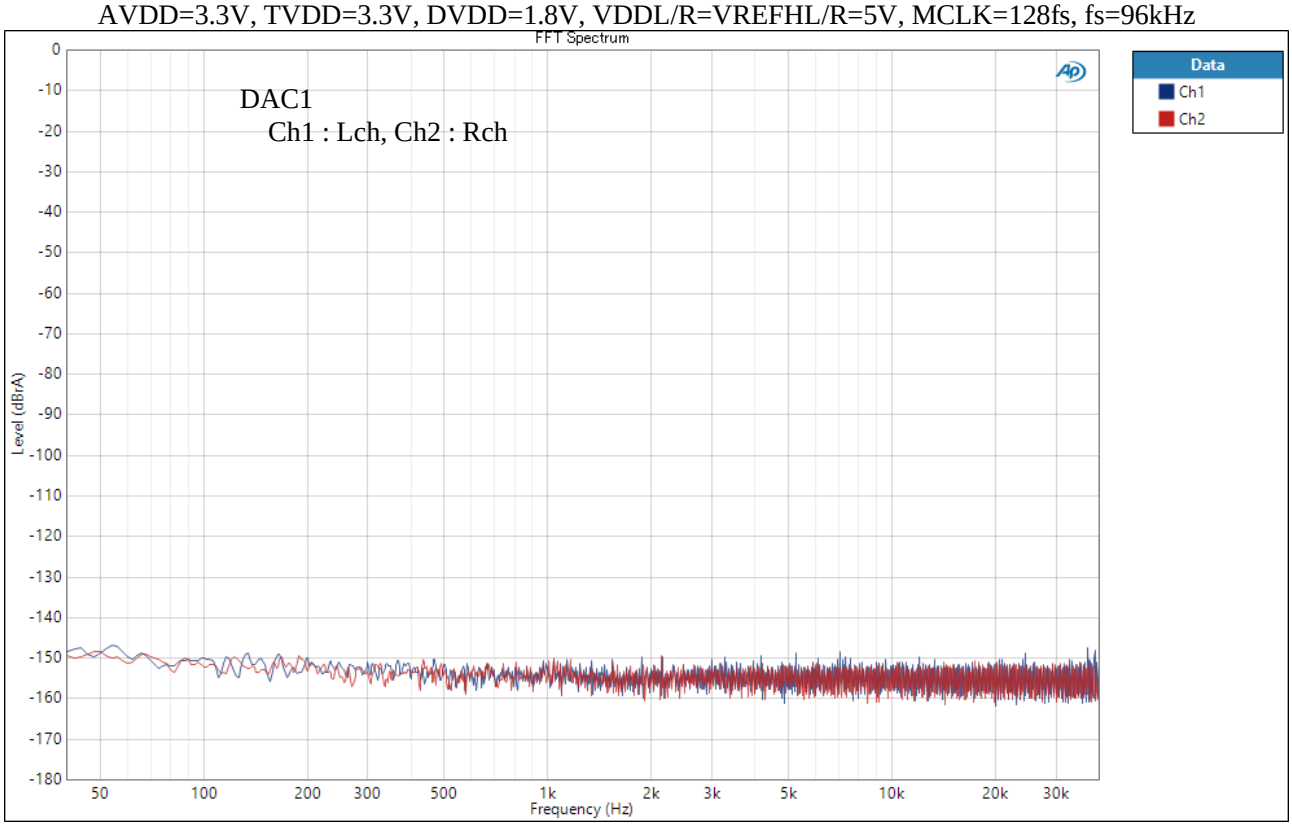


Figure 21-8. FFT (No Signal Input)

fs = 192kHz

AK4490R THD+N vs. Input Level

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

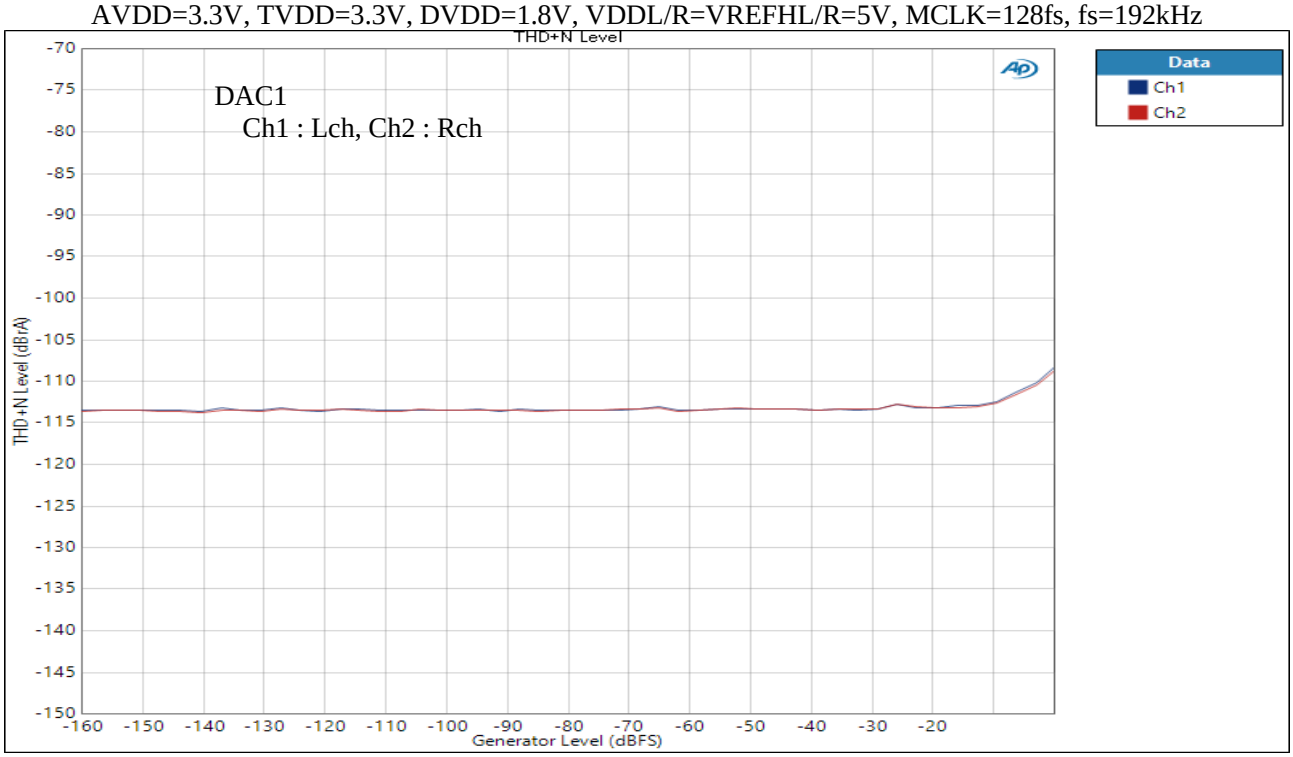


Figure 22-1. THD+N vs. Input Level

AK4490R THD+N vs. Input Frequency

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

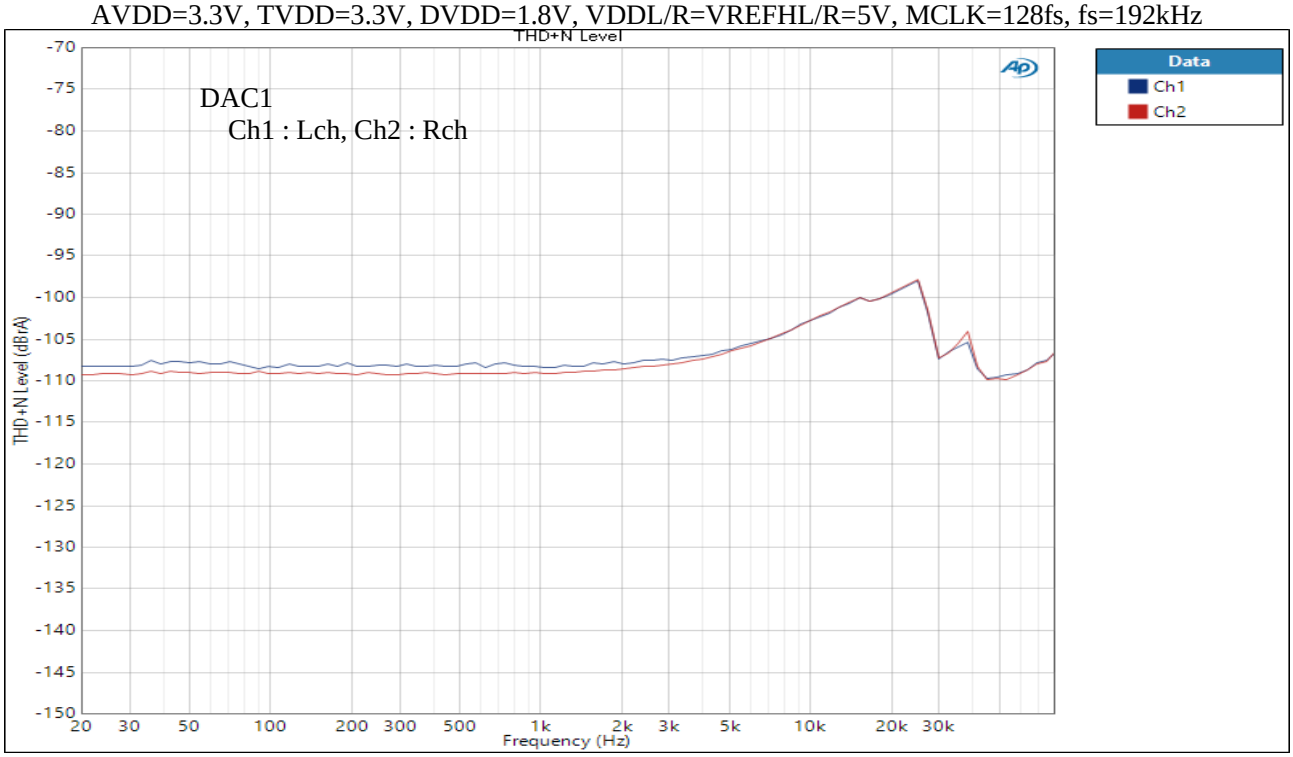


Figure 22-2. THD+N vs. Input Frequency

fs = 192kHz

AK4490R Linearity

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

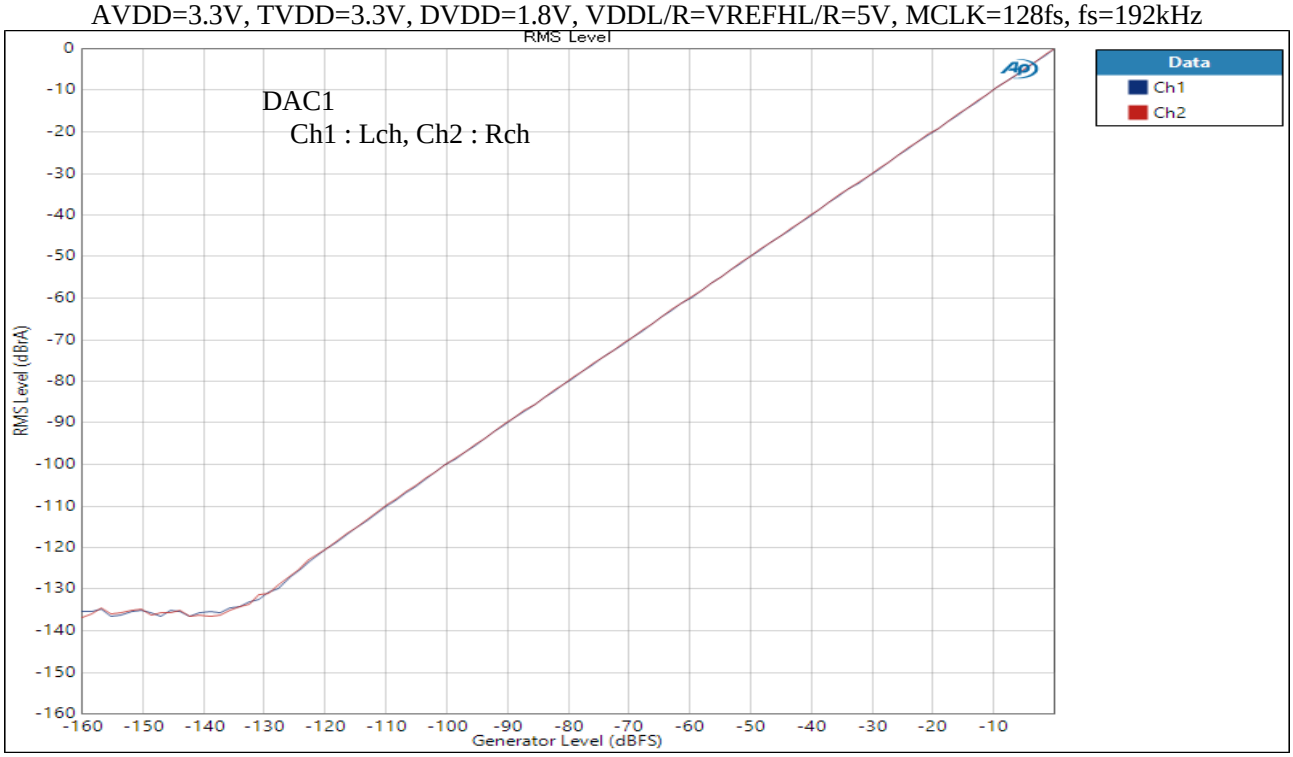


Figure 22-3. Linearity

AK4490R Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

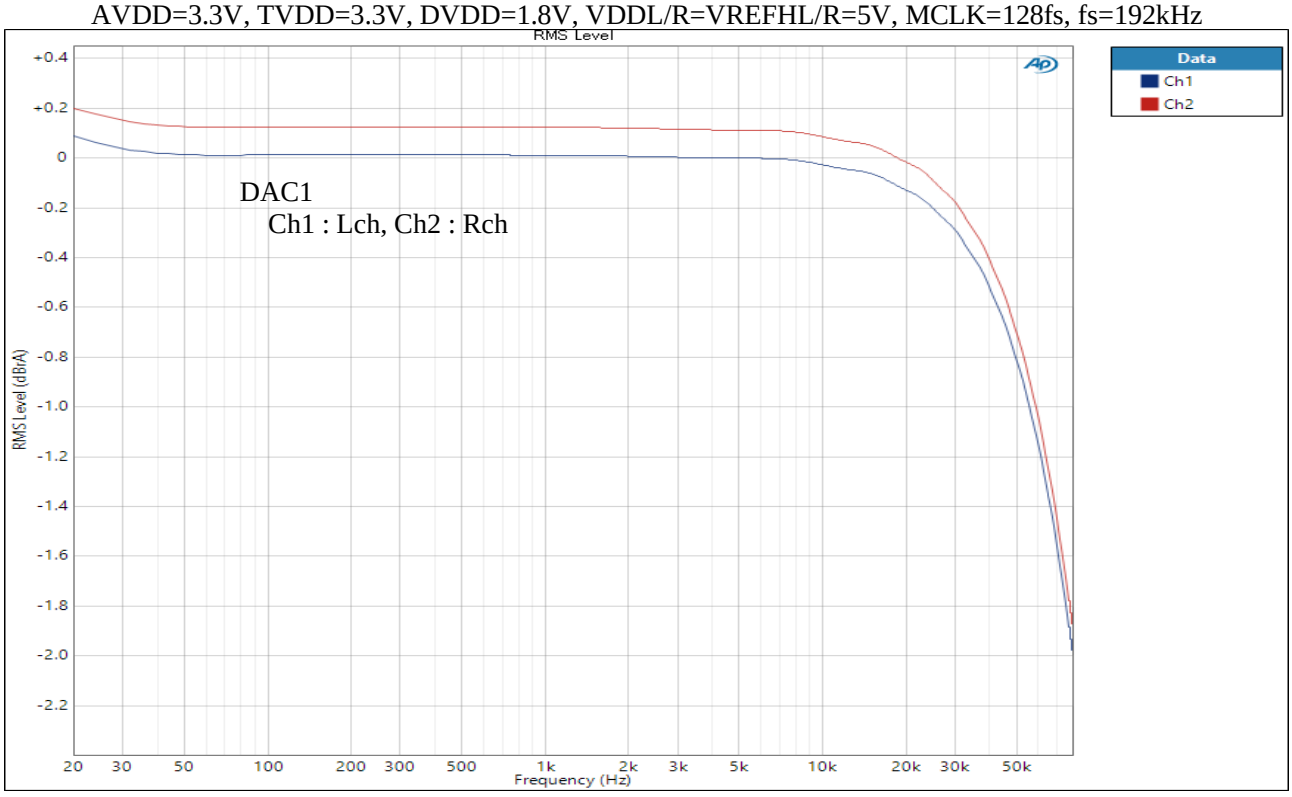


Figure 22-4. Frequency Response

fs = 192kHz

AK4490R Crosstalk

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

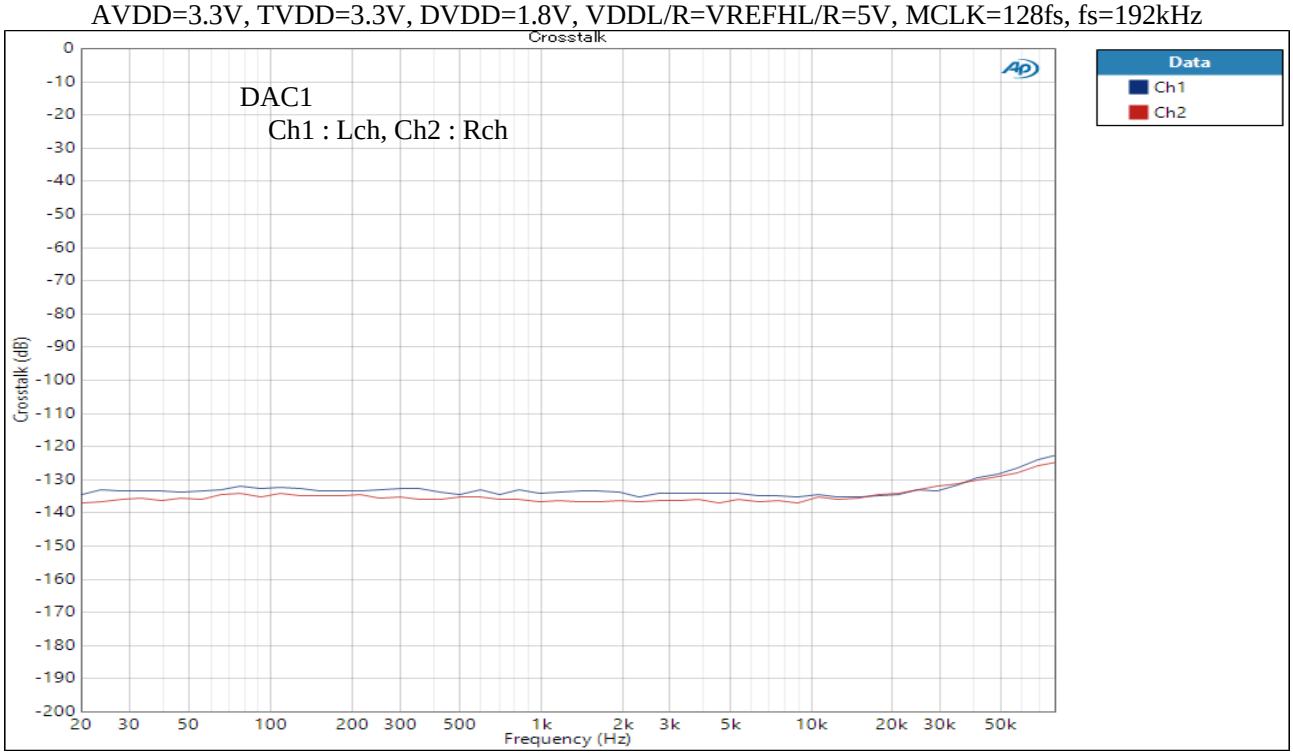


Figure 22-5. Crosstalk

AK4490R FFT (0dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

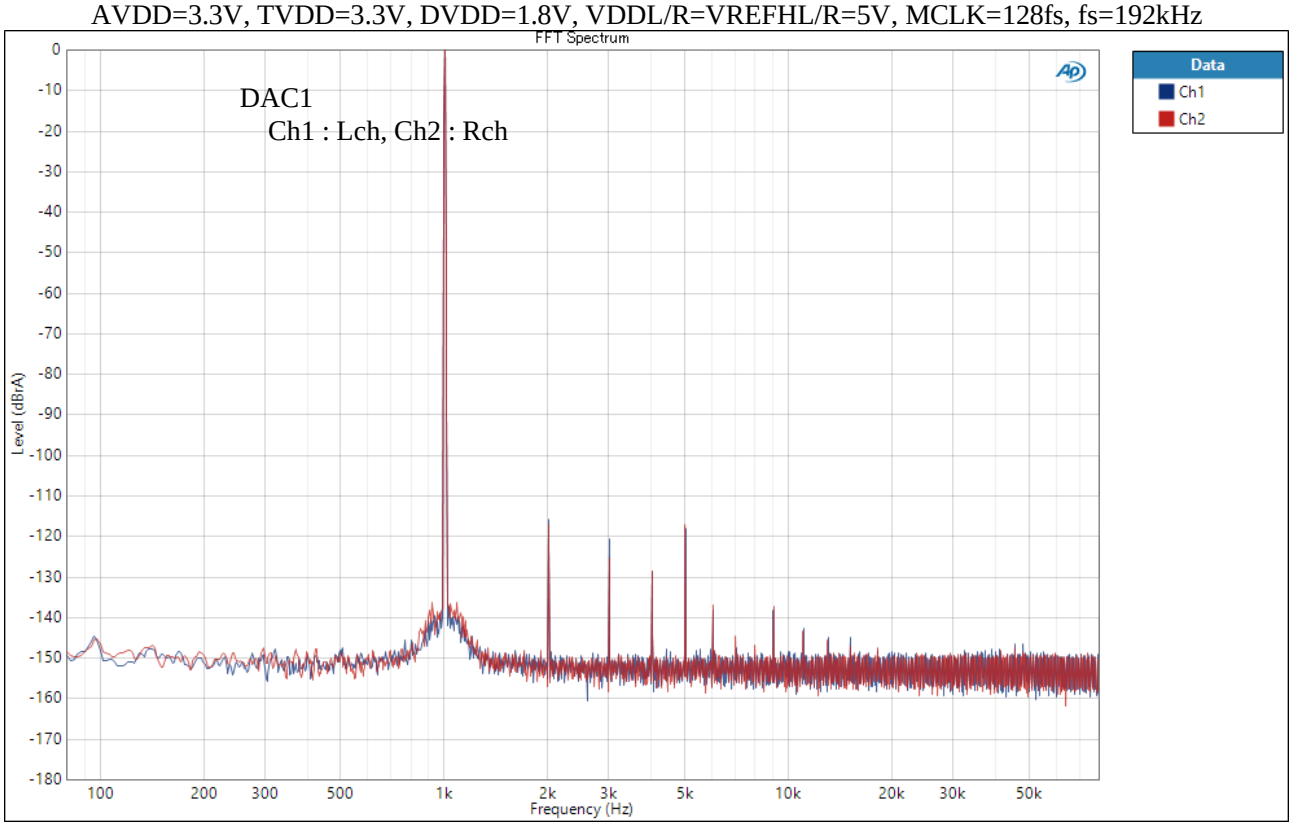


Figure 22-6. FFT (0dBFS Input)

fs = 192kHz

AK4490R FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

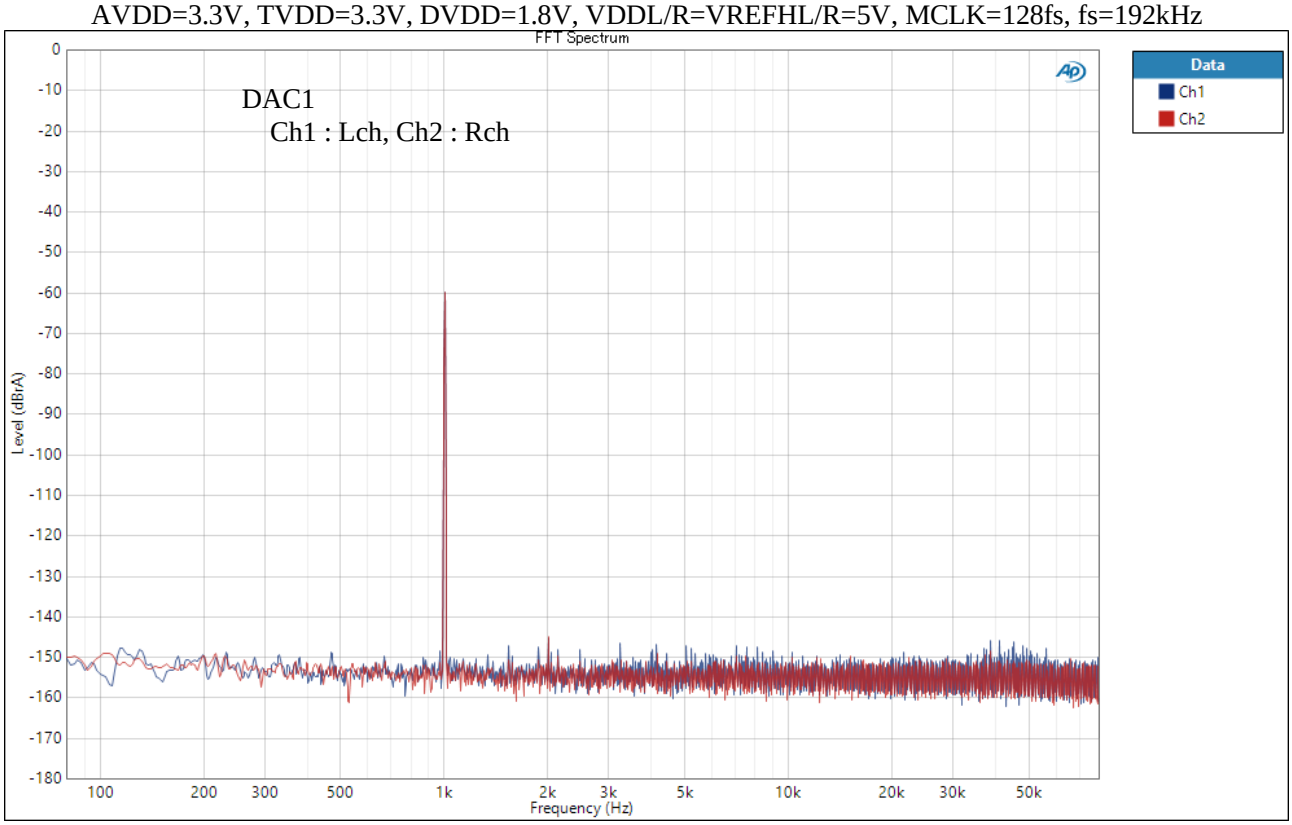


Figure 22-7. FFT (-60dBFS Input)

AK4490R FFT (No Signal Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

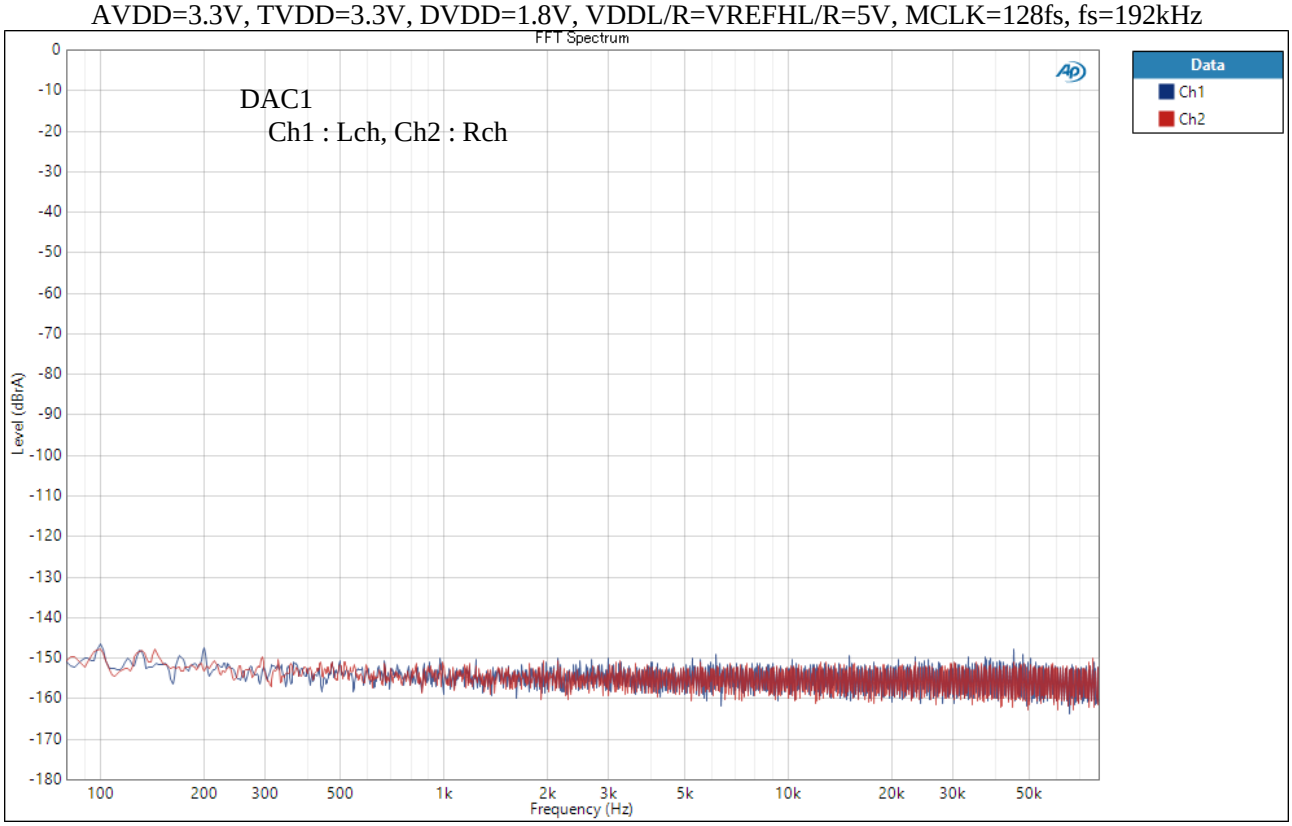
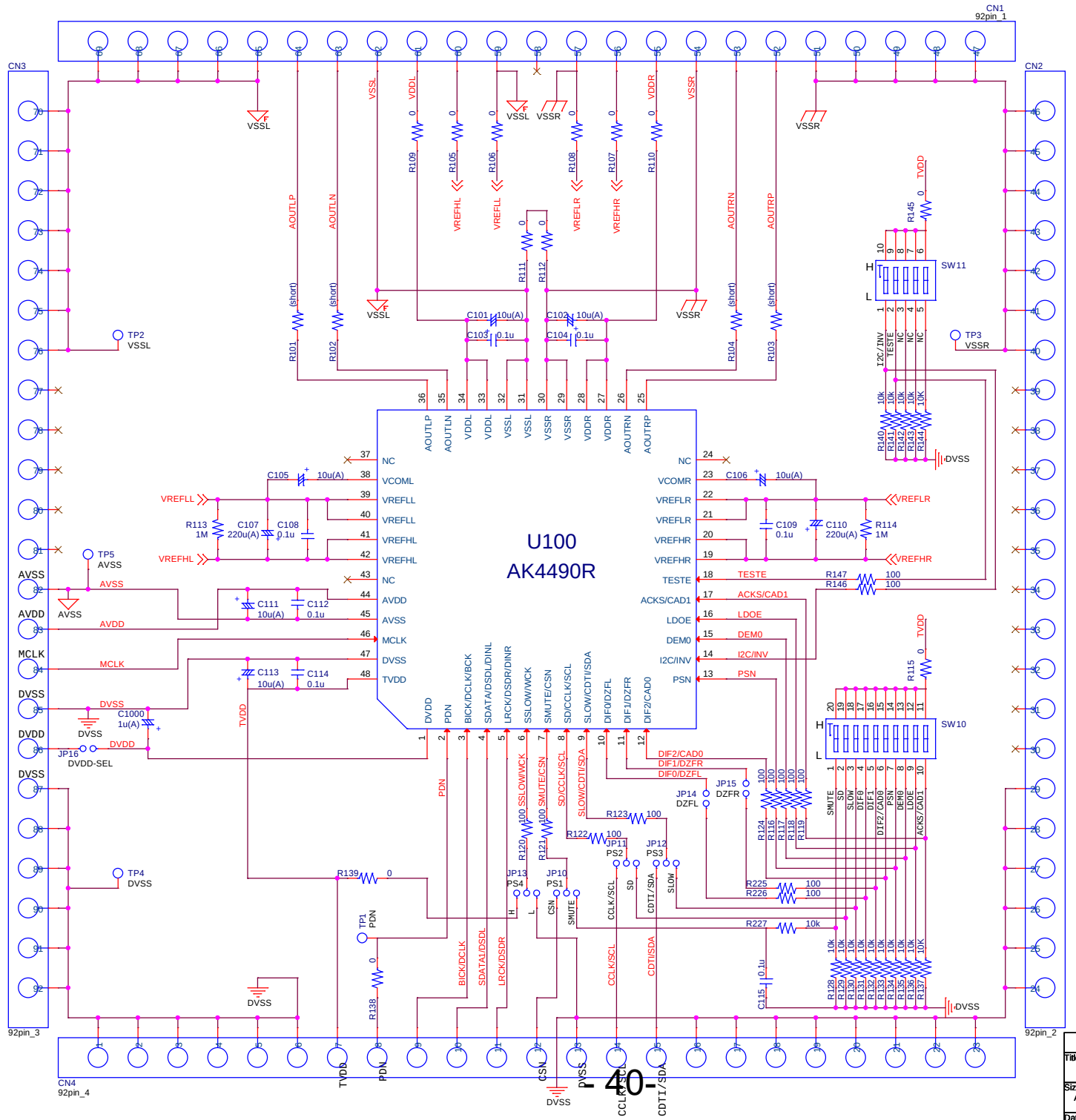


Figure 22-8. FFT (No Signal Input)



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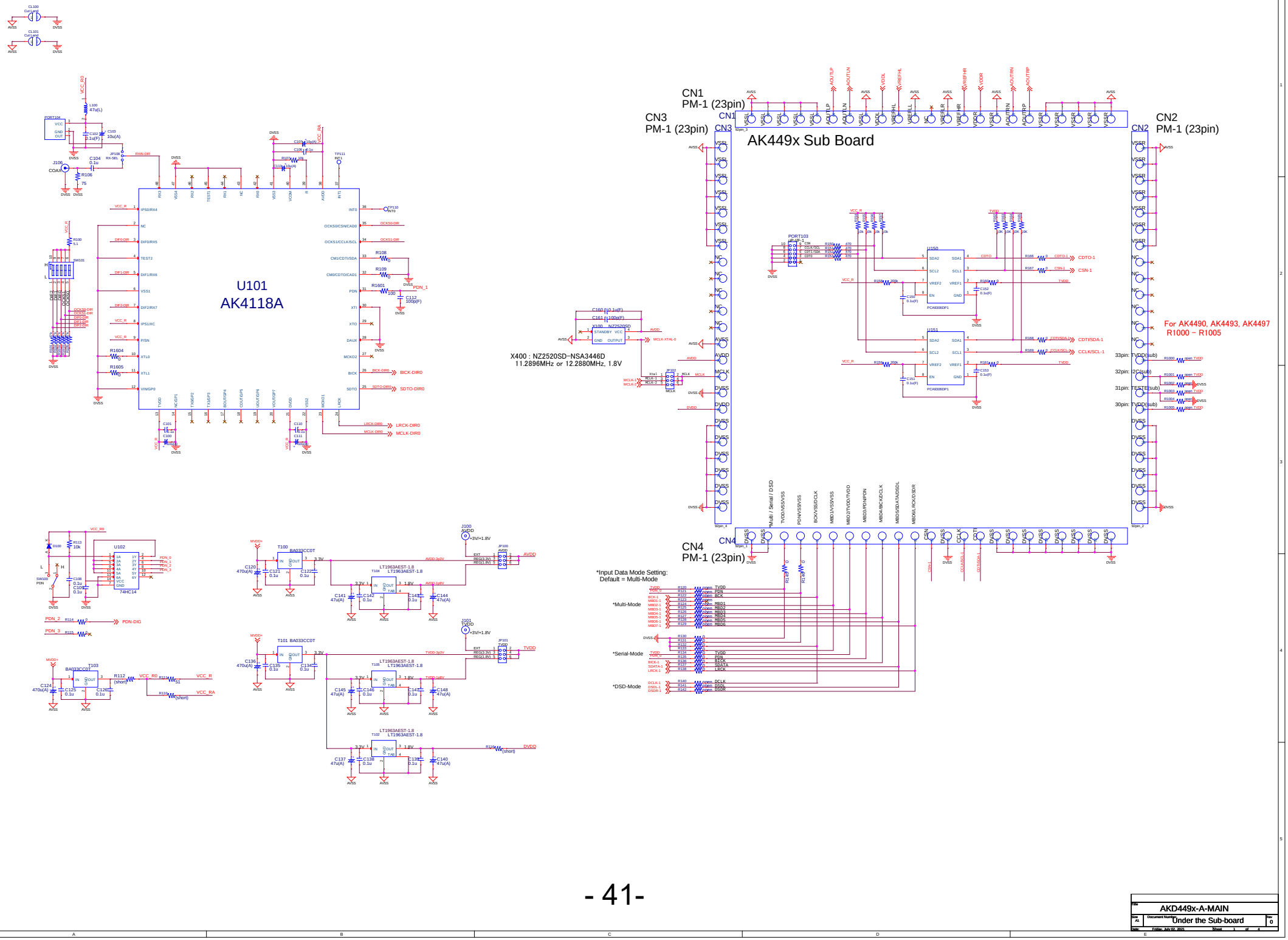
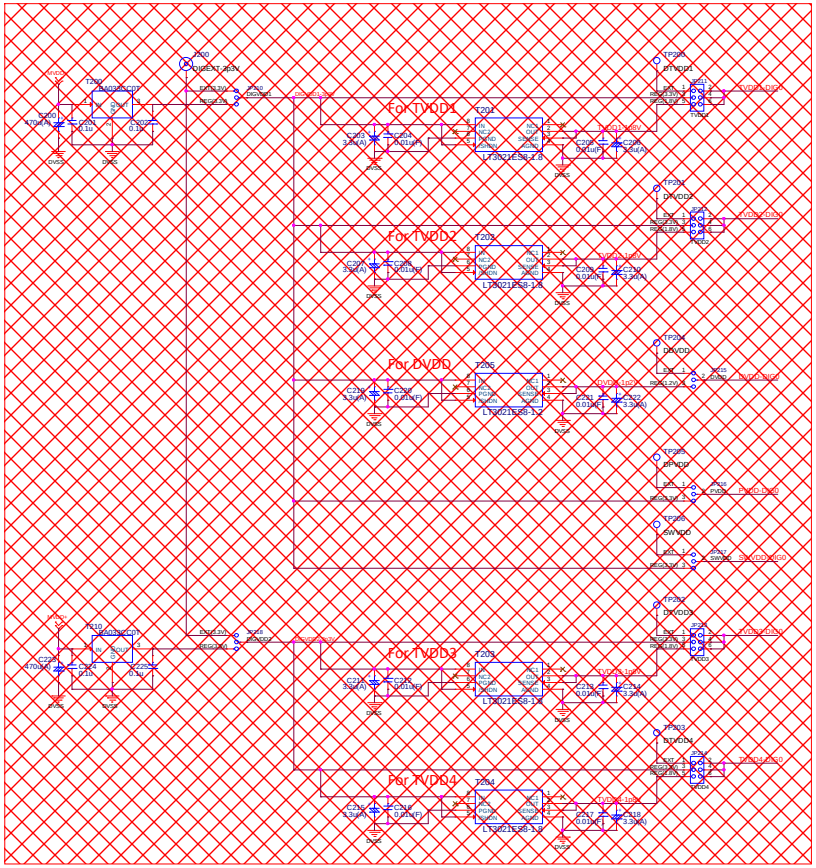
Size	A3
Document Number	AK4490R
Rev	0
Date:	Thursday, May 13, 2021
Sheet	1 of 1

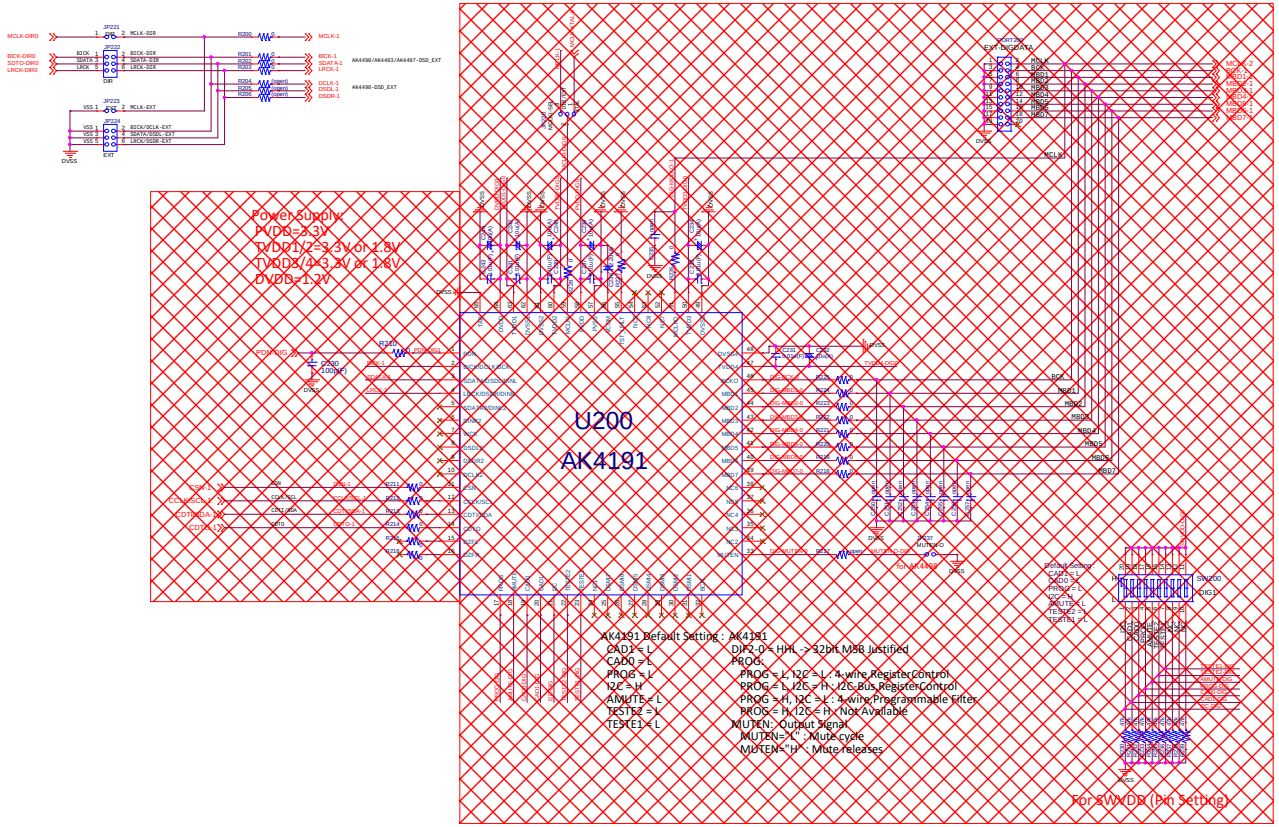


Title	AKD449x-A-MAIN		
Size A1	Document Number: Under the Sub-board		Rev 0
Date: Friday, July 02, 2021	Sheet 1 of 4		

AK4191 Digital-IC Block

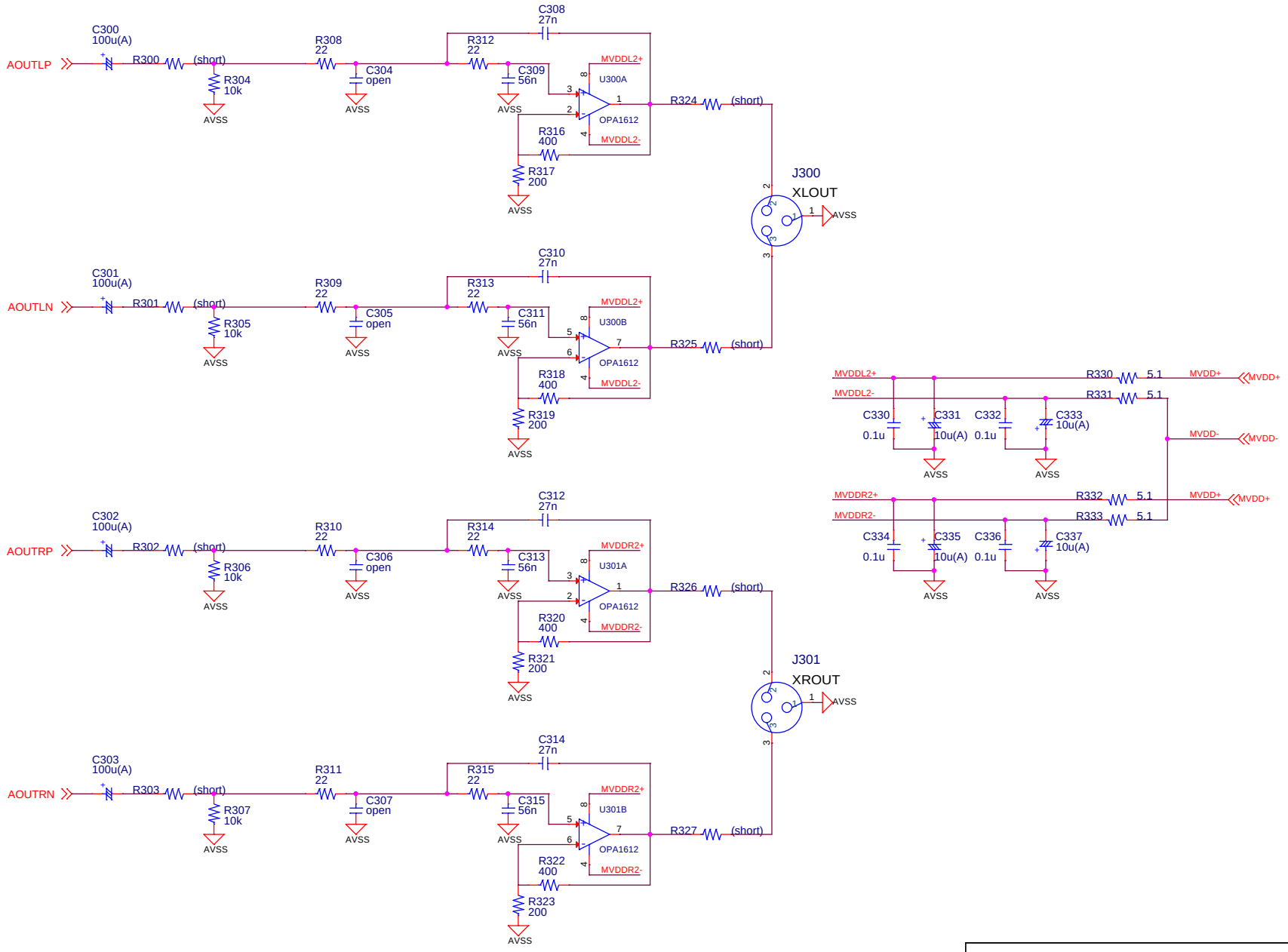


Parts no mounted



Parts no mounted

File	AKD449x-A-MAIN	
Size A1	Document Number AK4191	Rev 0
Date: Friday, July 02, 2021	Sheet 2 of 4	



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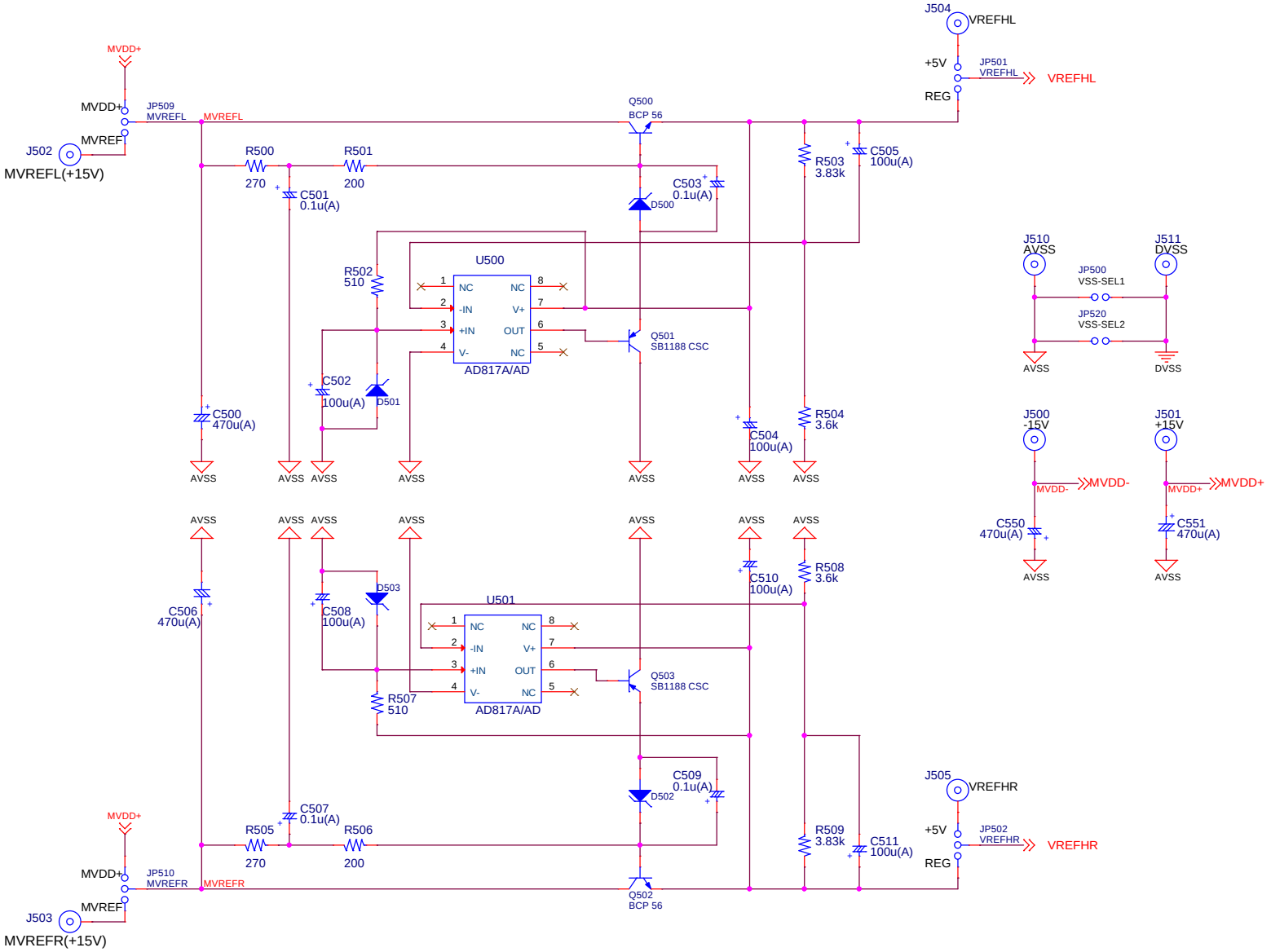
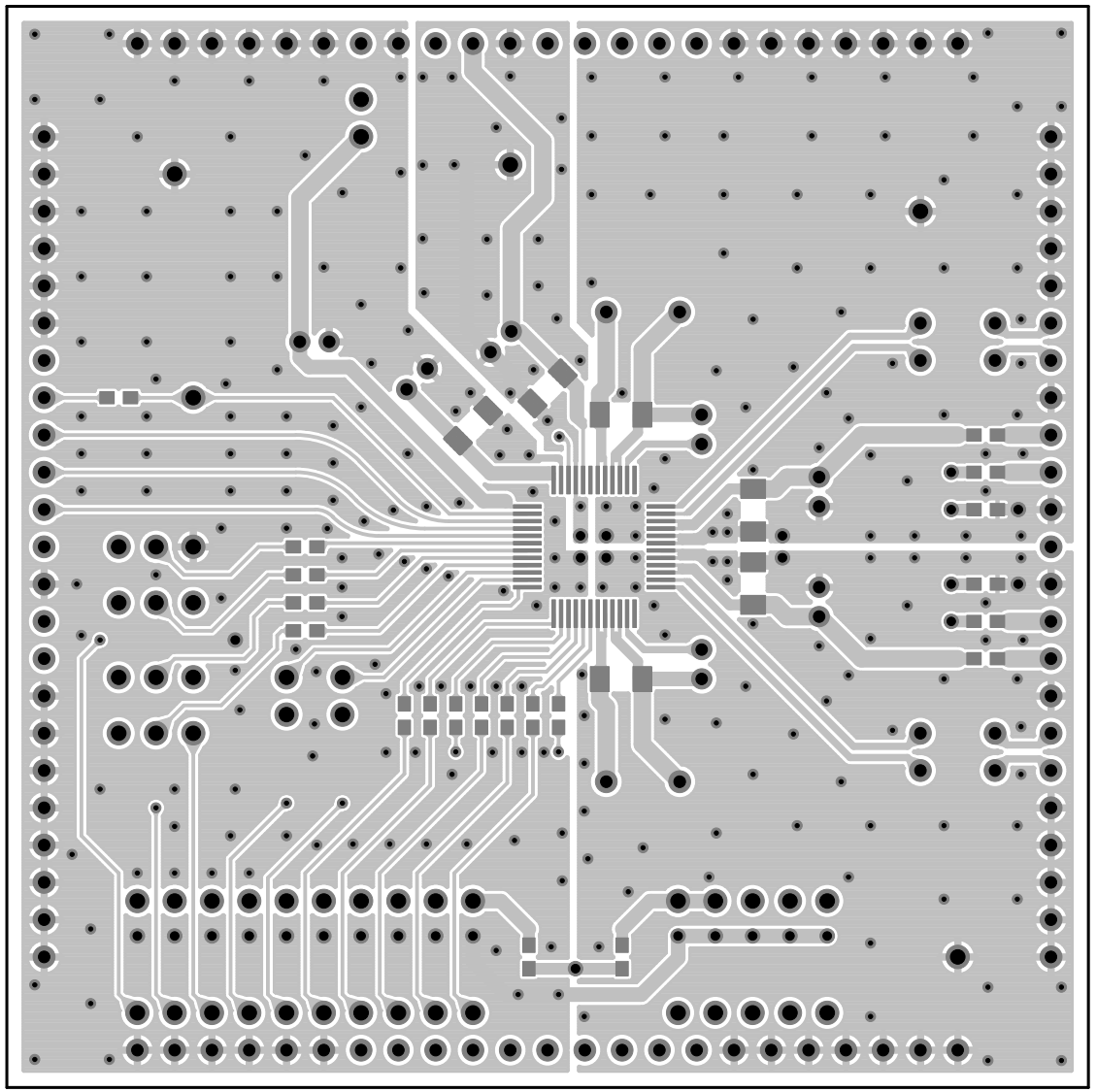
Size A3	Document Number External LPF2 Analog Output	Rev 0
Date: Friday, July 02, 2021	Sheet 3 of 4	

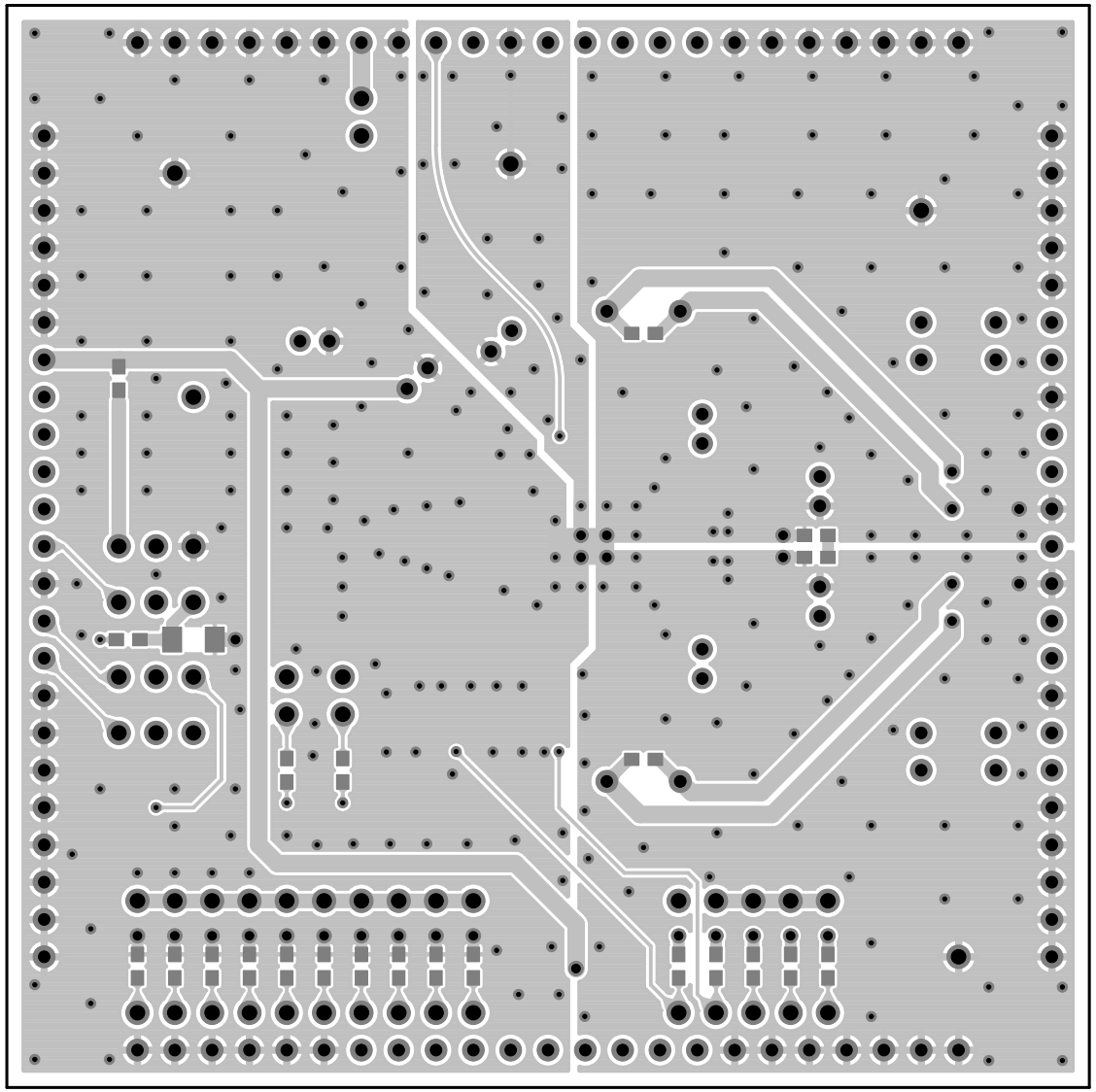


Title	AKD449x-A-MAIN	
Size A3	Document Number Power Supply Unit	Rev 0
Date: Friday, July 02, 2021	Sheet 4 of 4	



AKD4490R-A-SUB-48LQFP Rev.0
Lay1

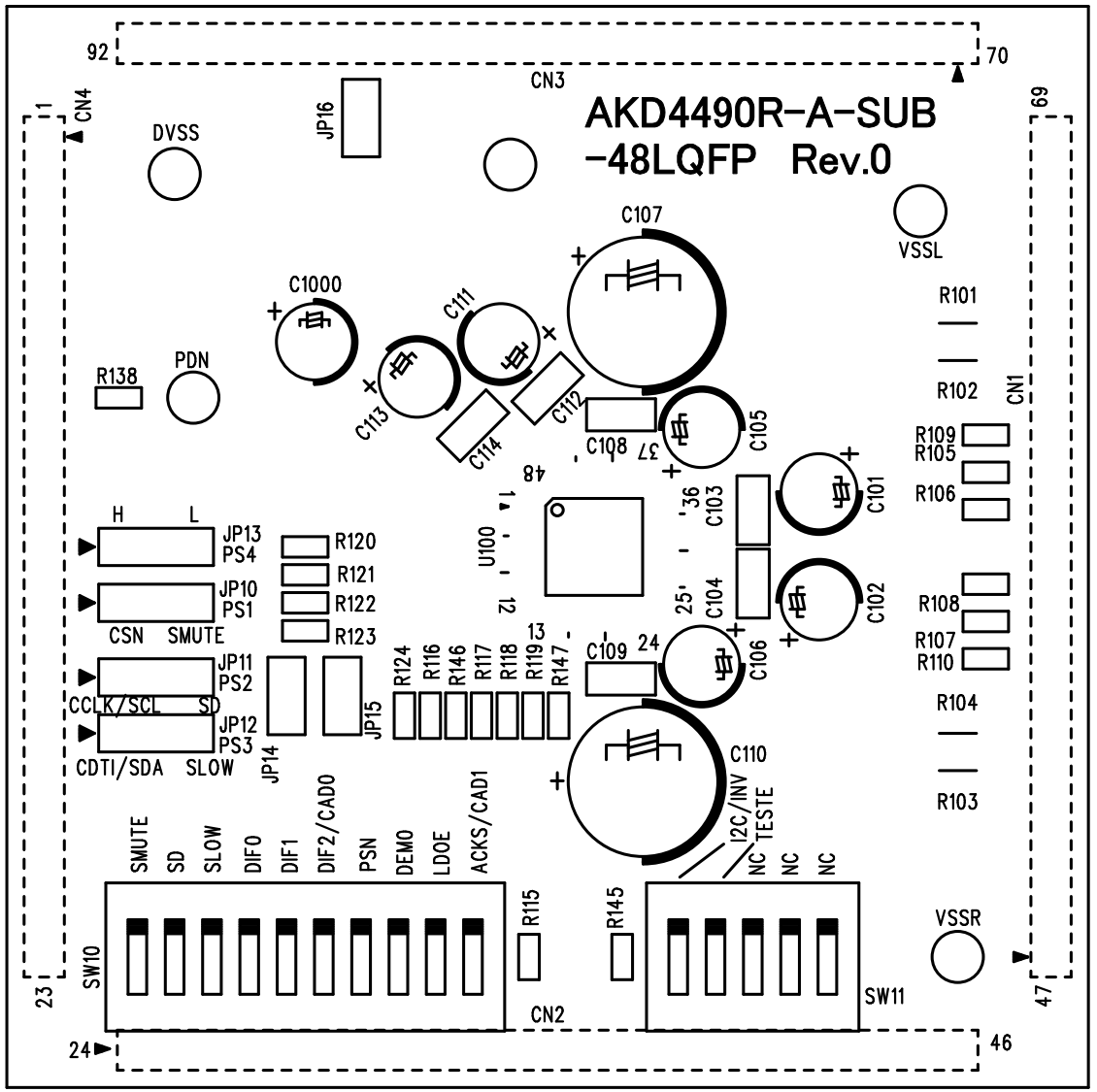
2021.6.25



AKD4490R-A-SUB-48LQFP Rev.0

Lay2

2021.6.25



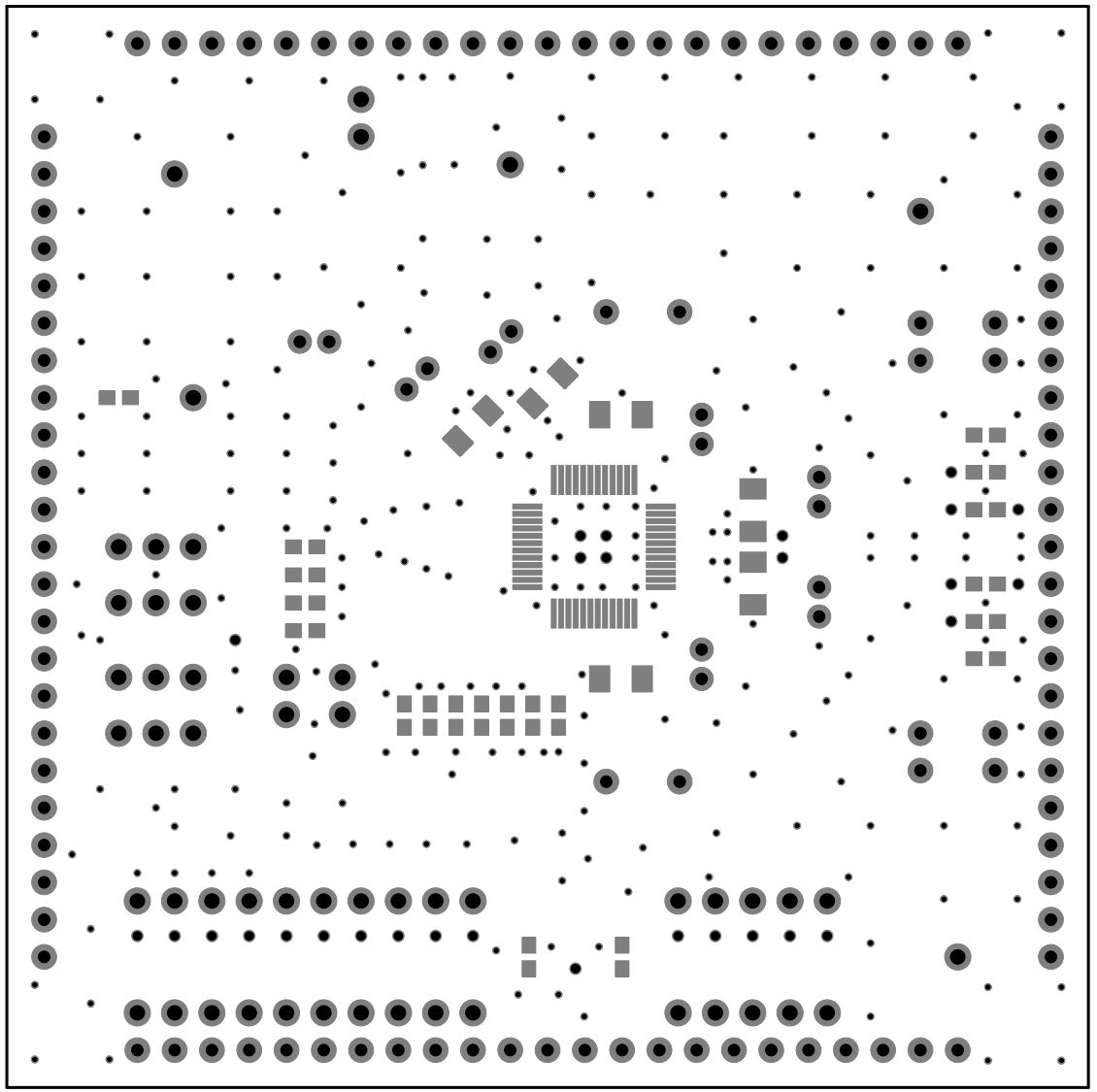
AKD4490R-A-SUB-48LQFP Rev.0
Silk1

2021.6.25

AKD4490R-A-SUB-48LQFP Rev.0

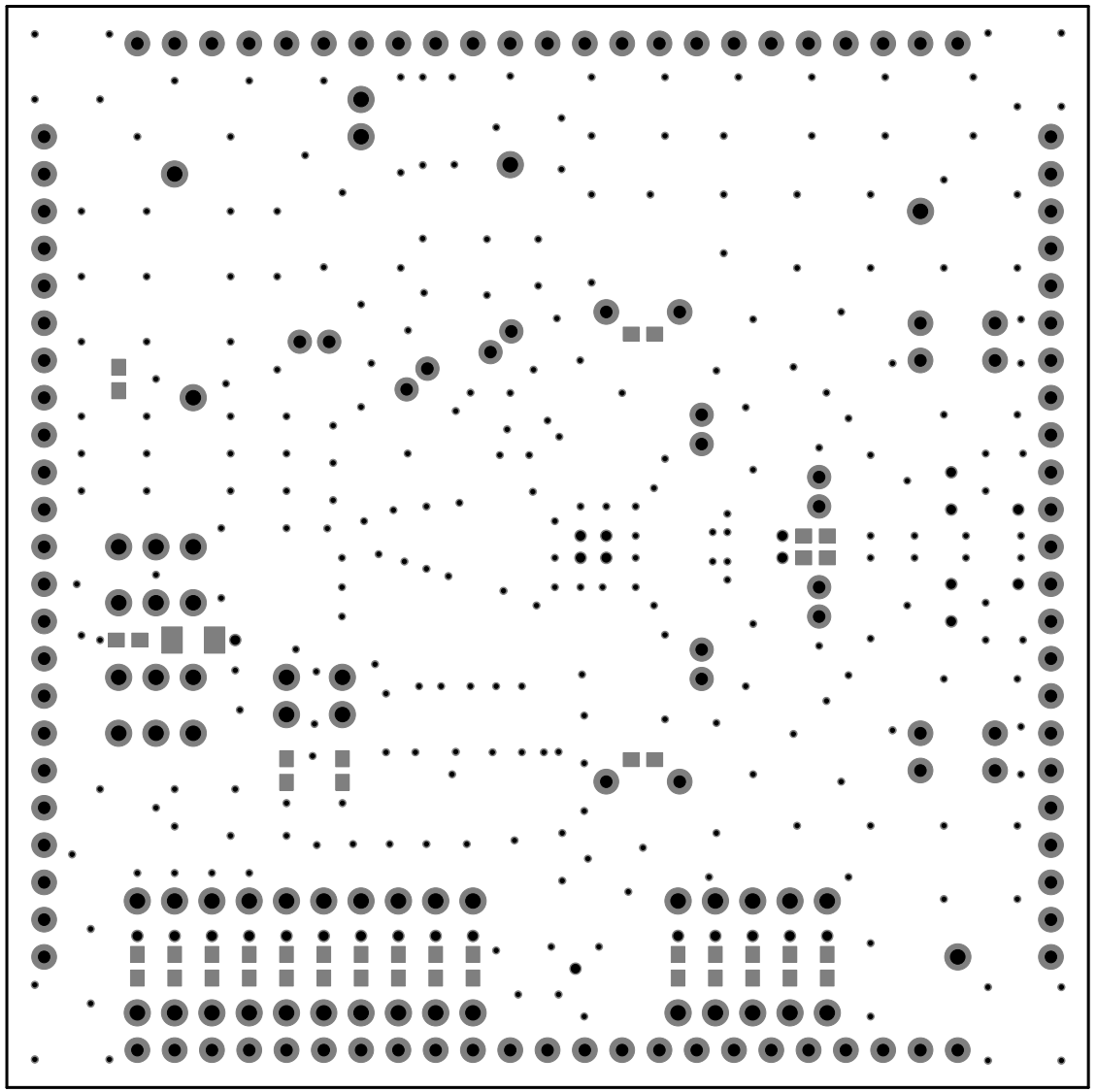
Silk2

2021.6.25



AKD4490R-A-SUB-48LQFP Rev.0
Resist1

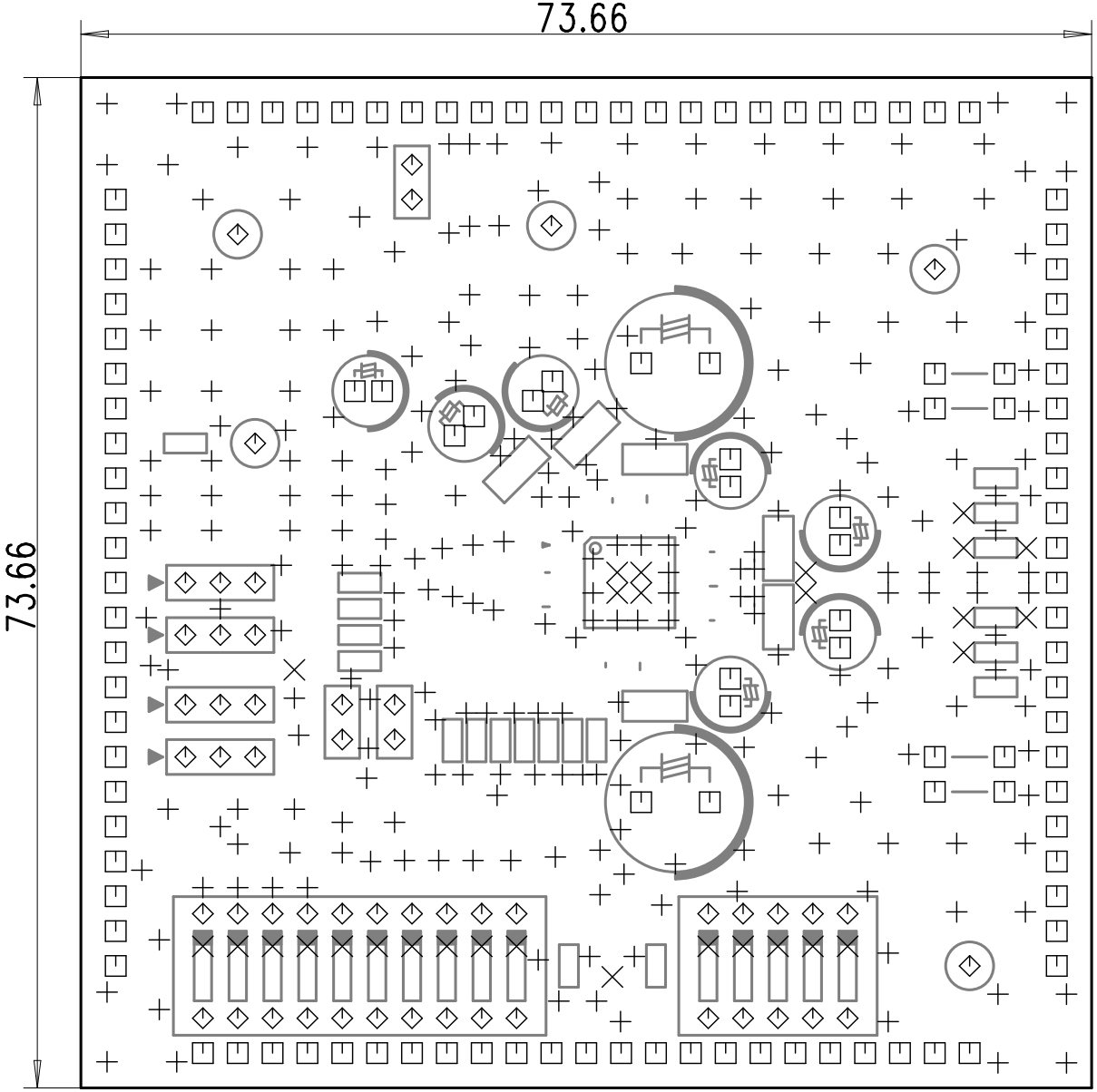
2021.6.25



AKD4490R-A-SUB-48LQFP Rev.0

Resist2

2021.6.25



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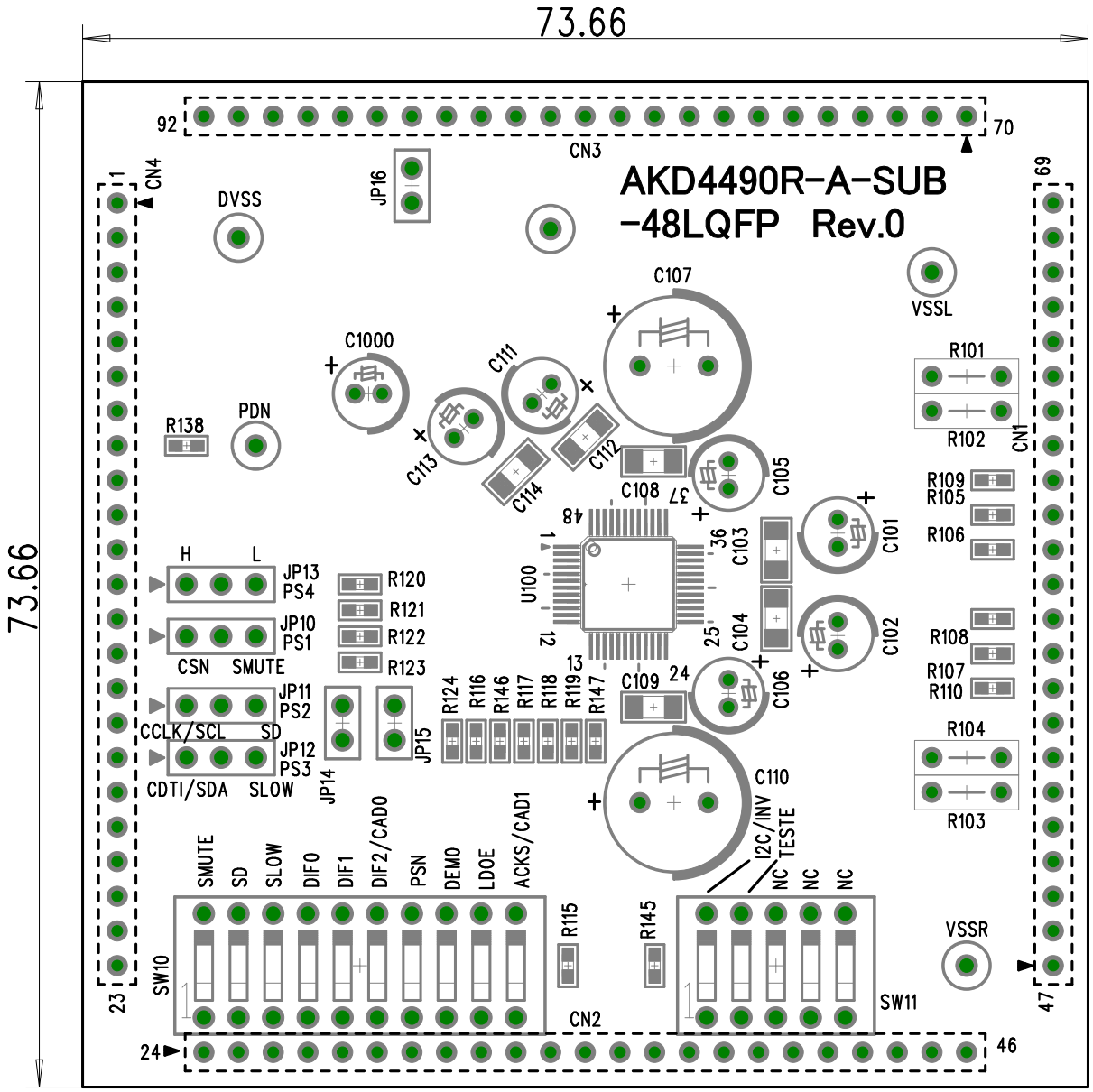
1	53	◇	YES	+/−0.0

AKD4490R-A-SUB-48LQFP Rev.0　　2021.6.25
Drill



AKD4490R-A-SUB-48LQFP Rev.0 2021.6.25
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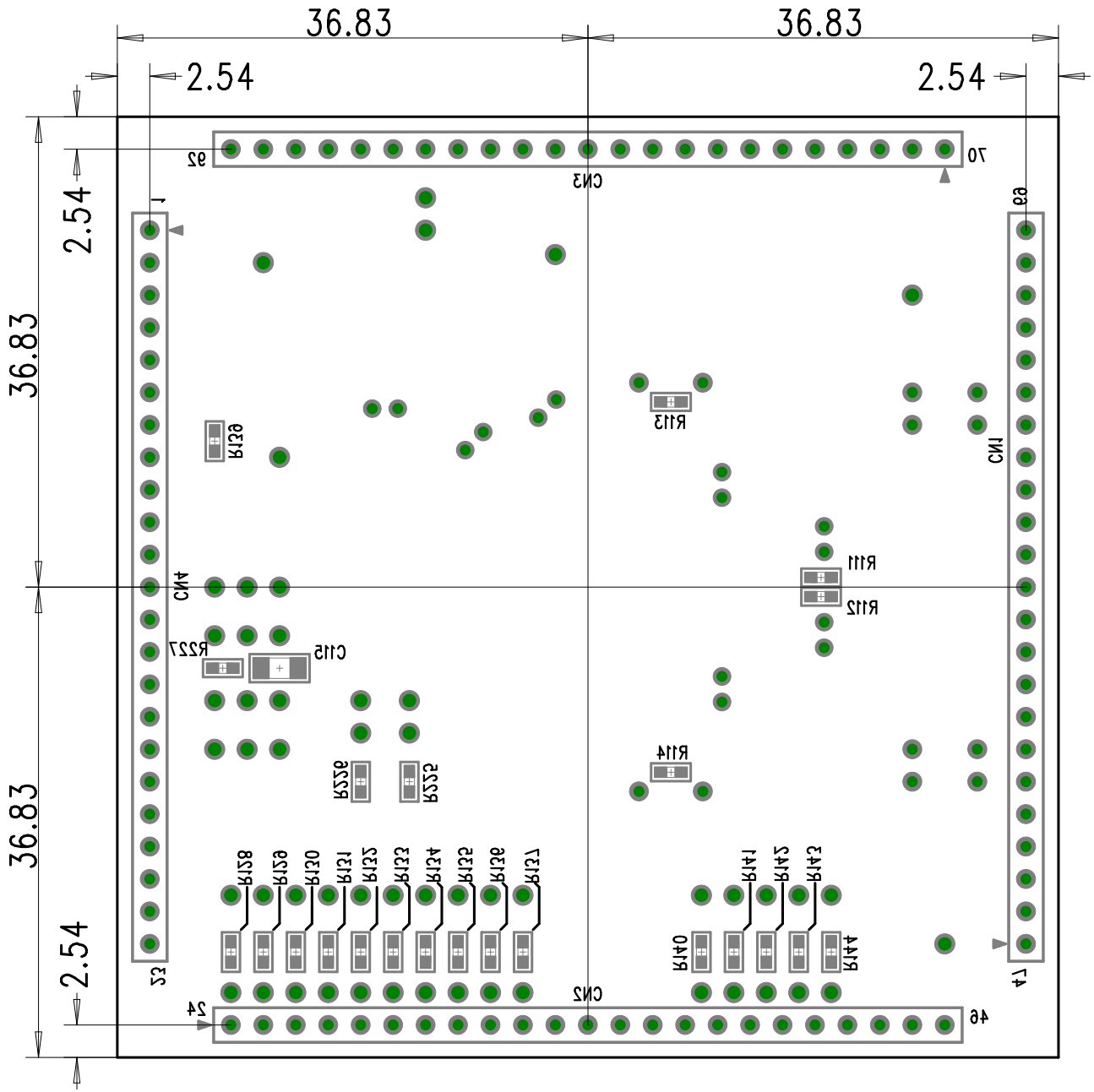
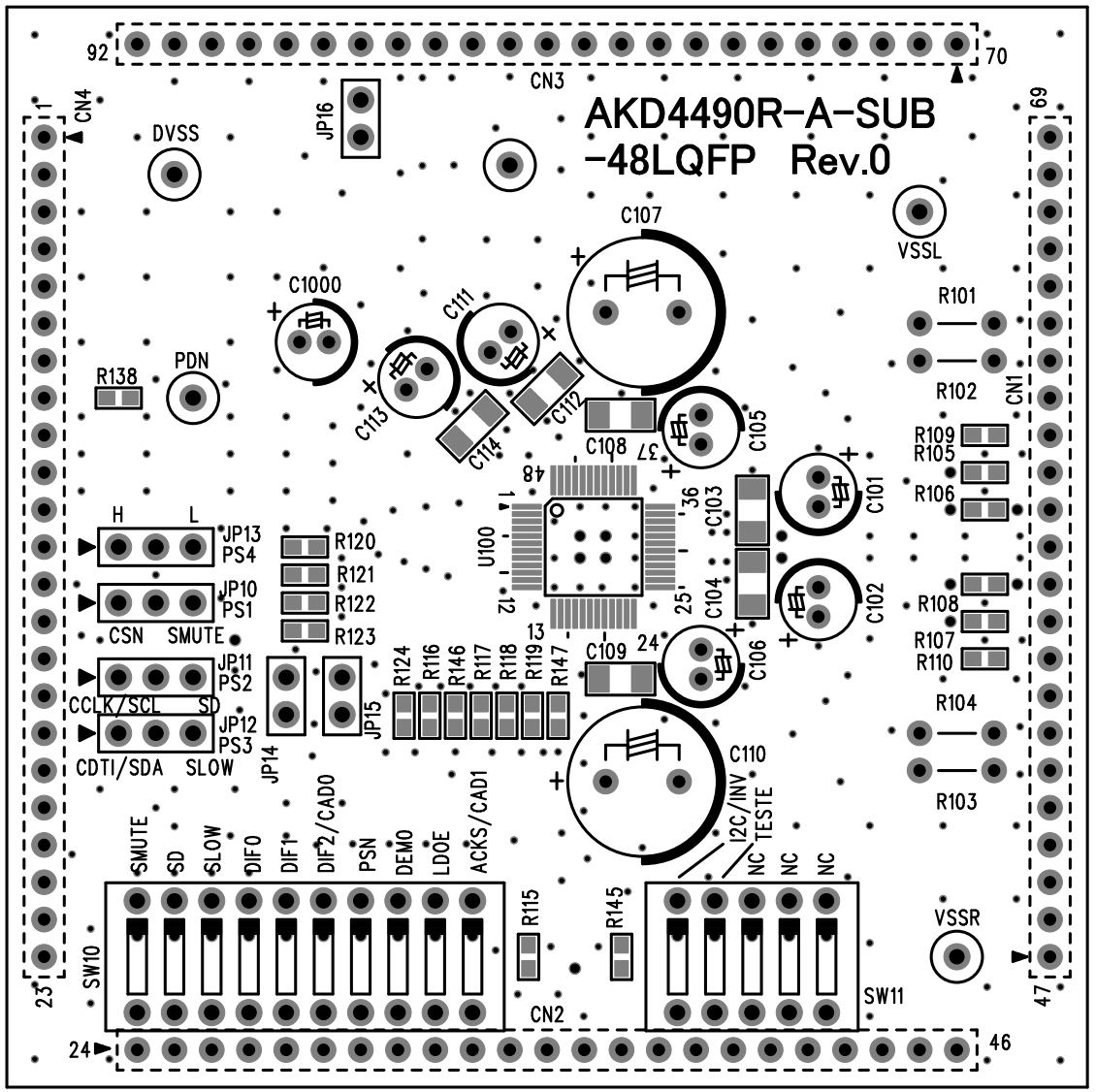


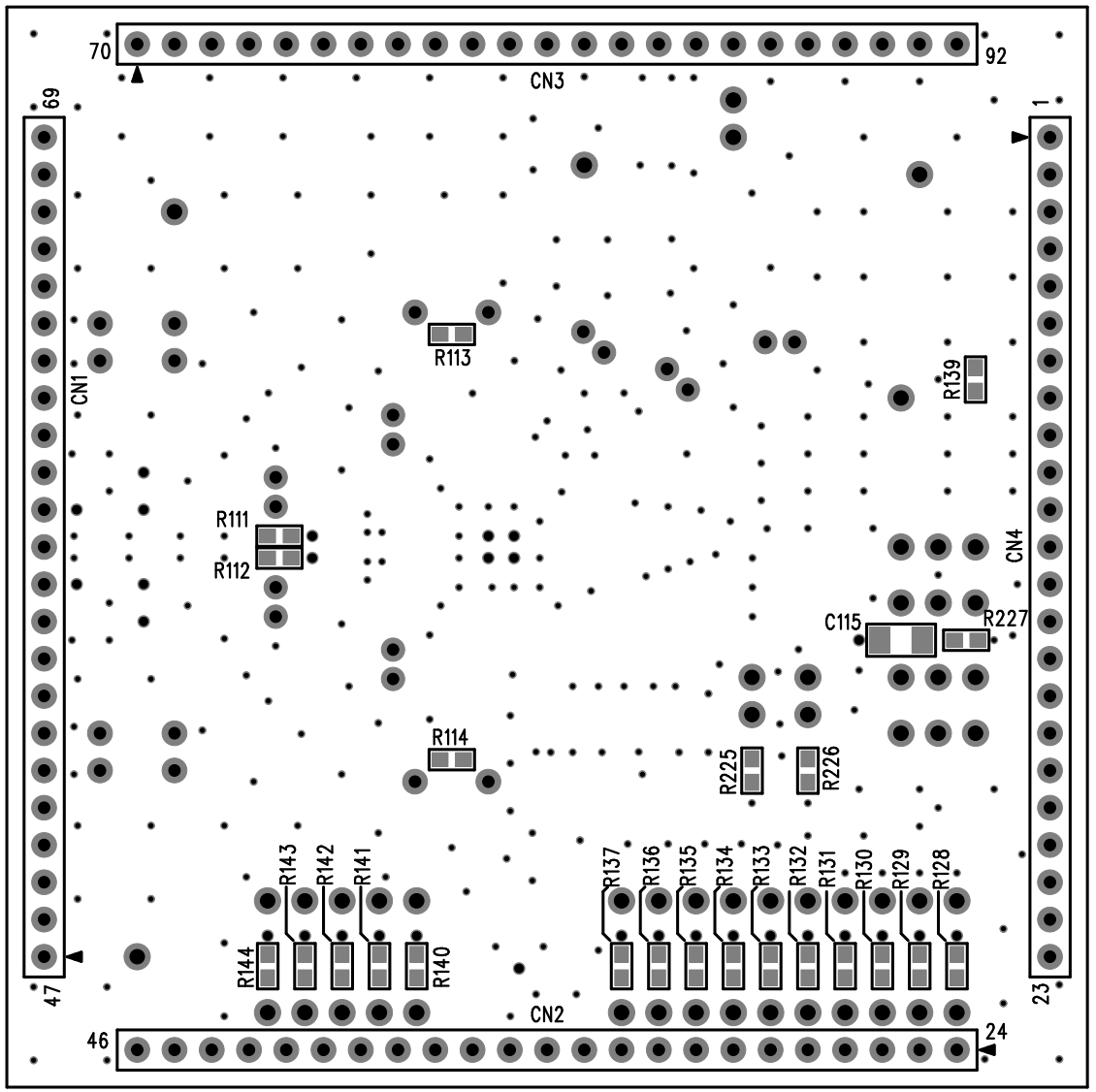
AKD4490R-A-SUB-48LQFP Rev.0 2021.6.25

Silk2 Assy2



AKD4490R-A-SUB-48LQFP Rev.0 2021.6.25

Silk1 Resist1

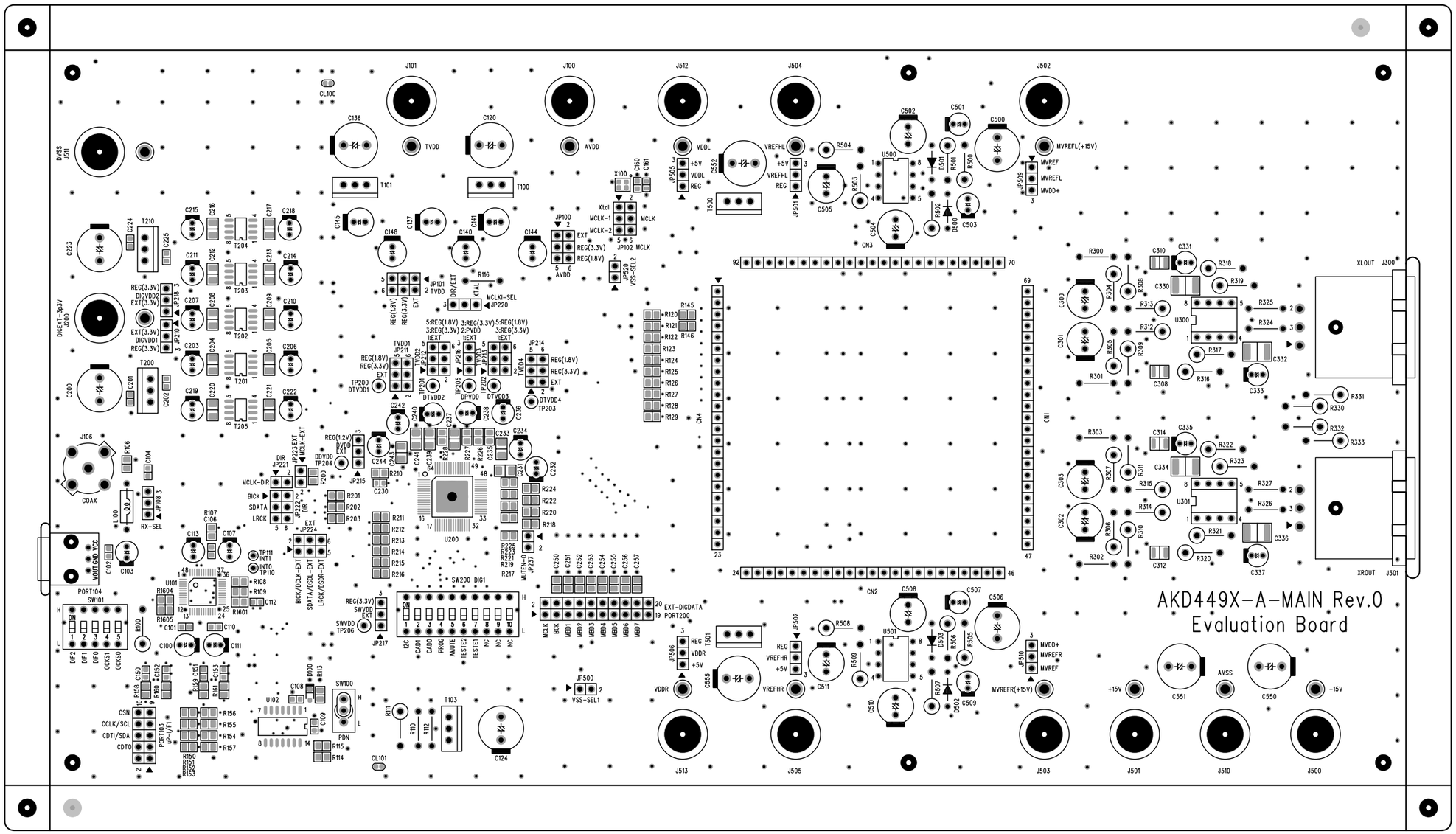


AKD4490R-A-SUB-48LQFP Rev.0 2021.6.25

Silk2 Resist2

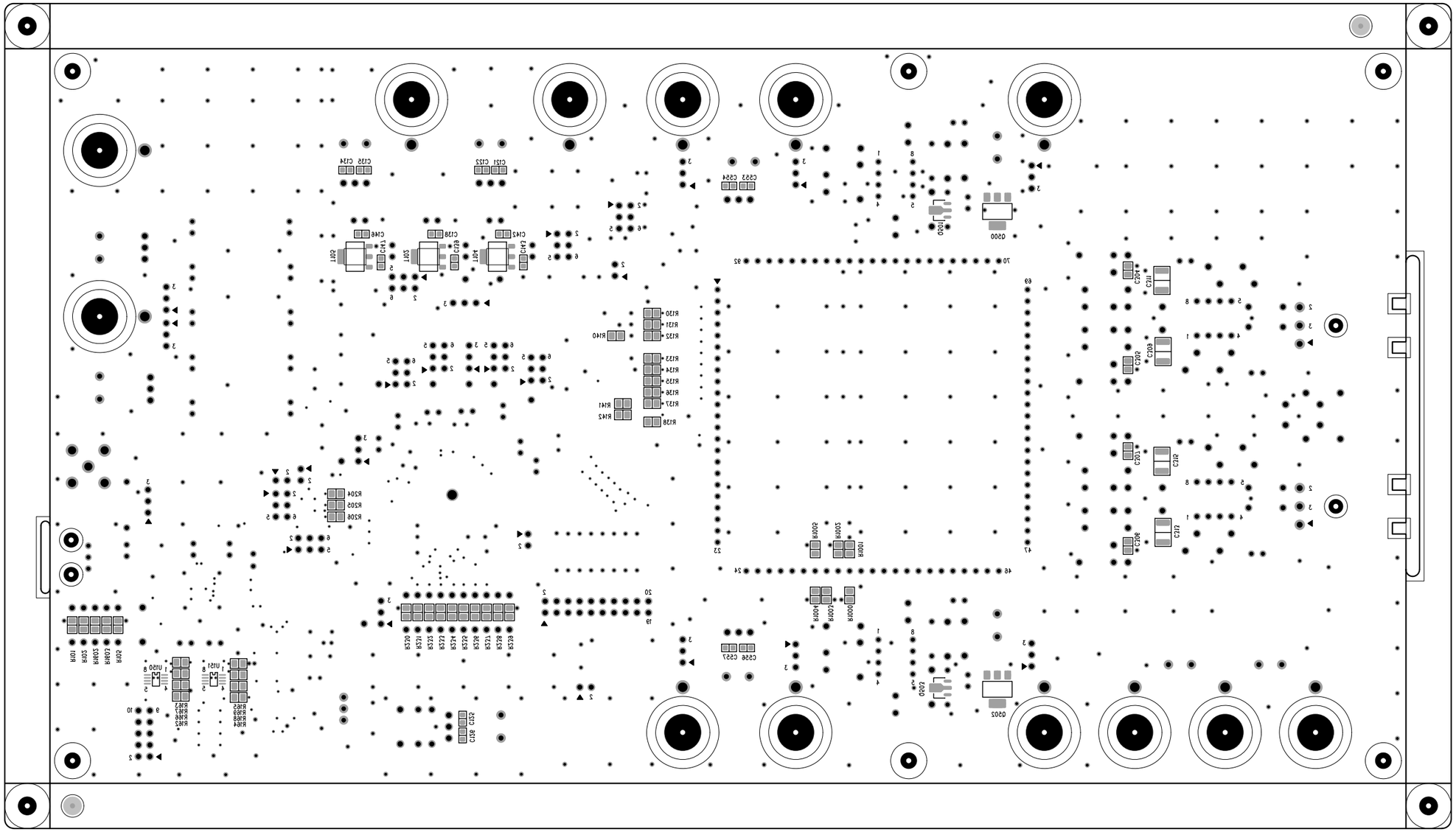
AKD449X-A-MAIN_Rev.0

部品面シルク図　　部品面透視図



AKD449X-A-MAIN_Rev.0

半田面シルク図　　部品面透視図



AKD449X-A-MAIN_Rev.0

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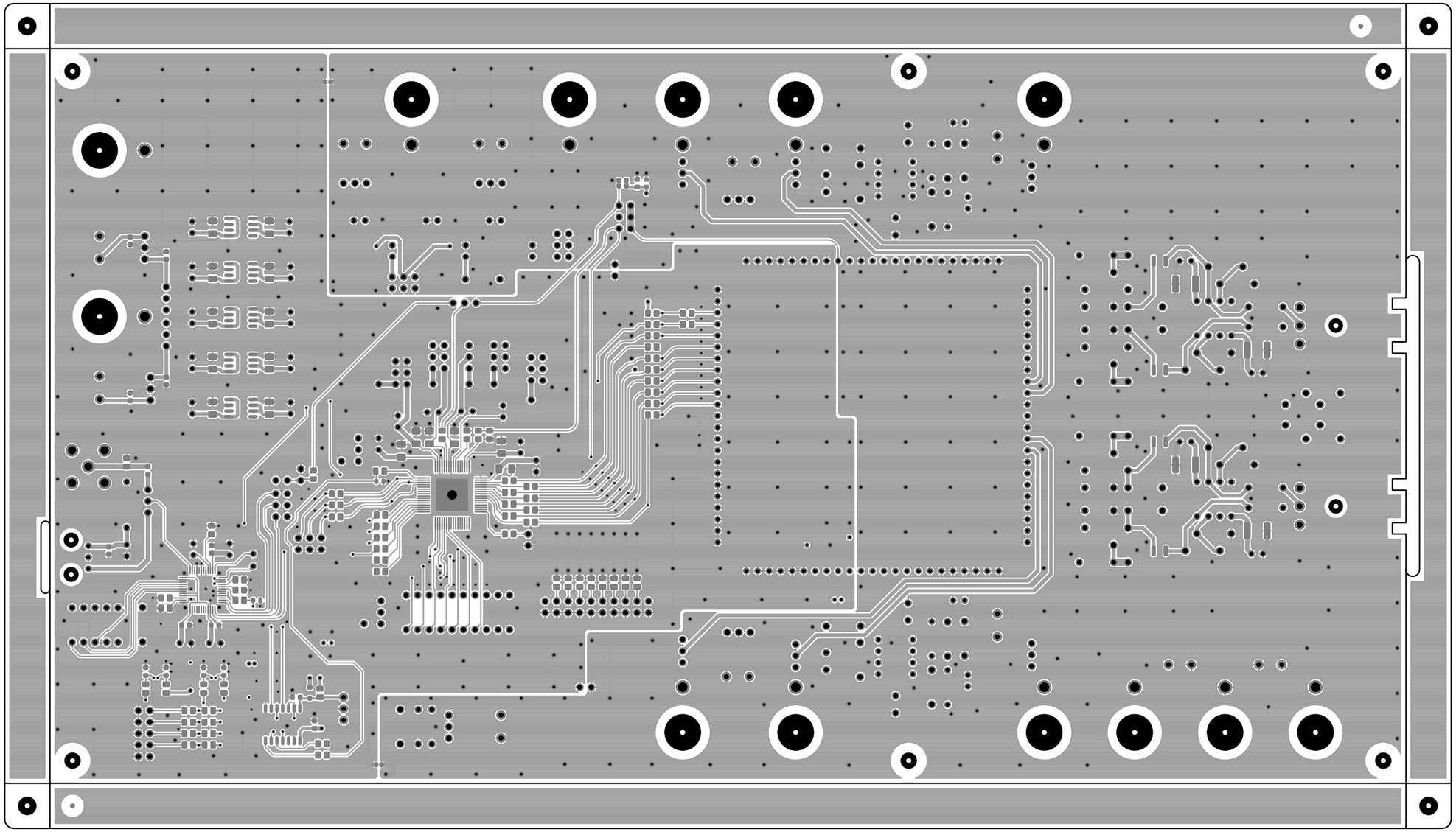

AKD449X-A-MAIN_Rev.0

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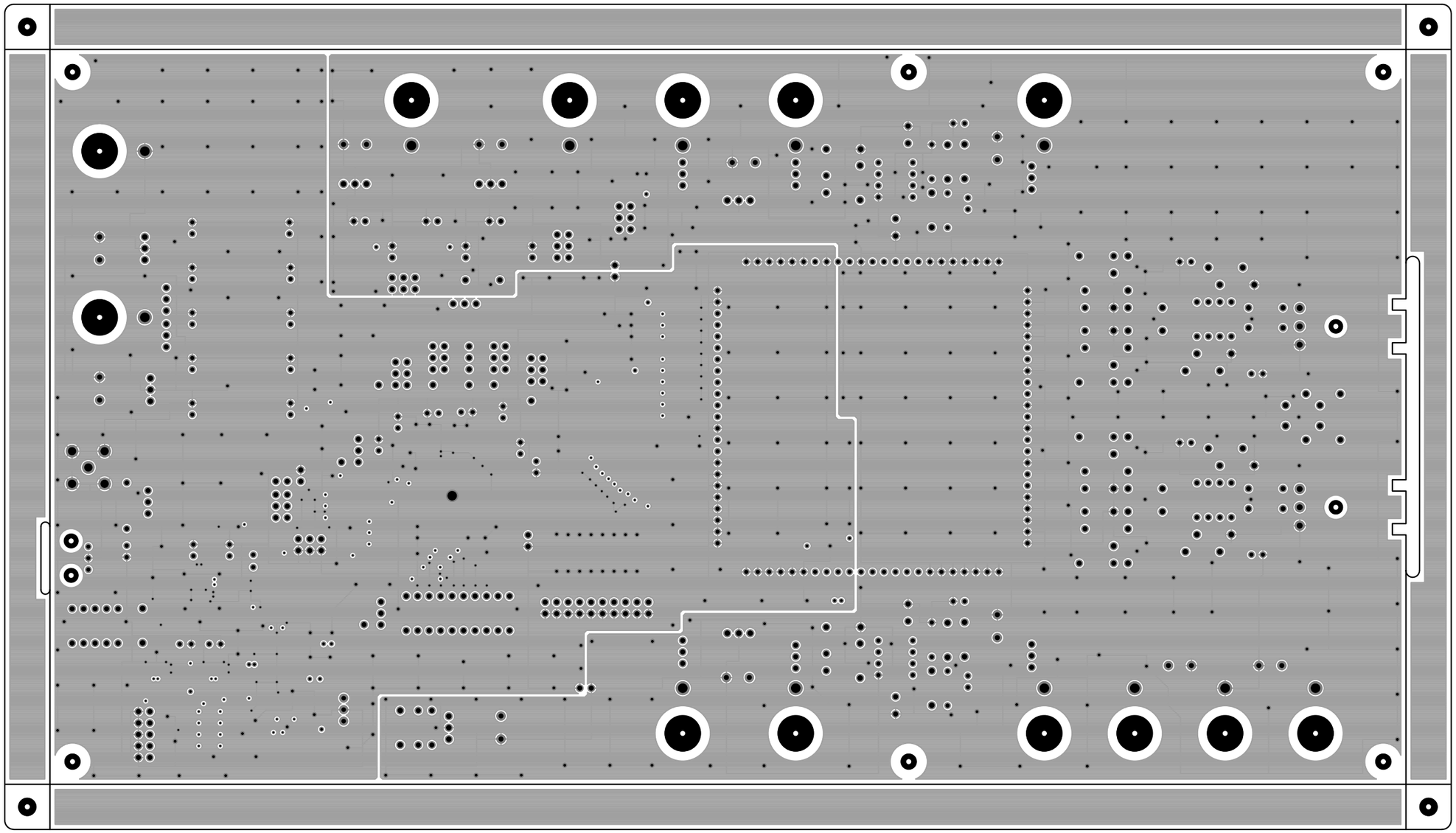

AKD449X-A-MAIN_Rev.0

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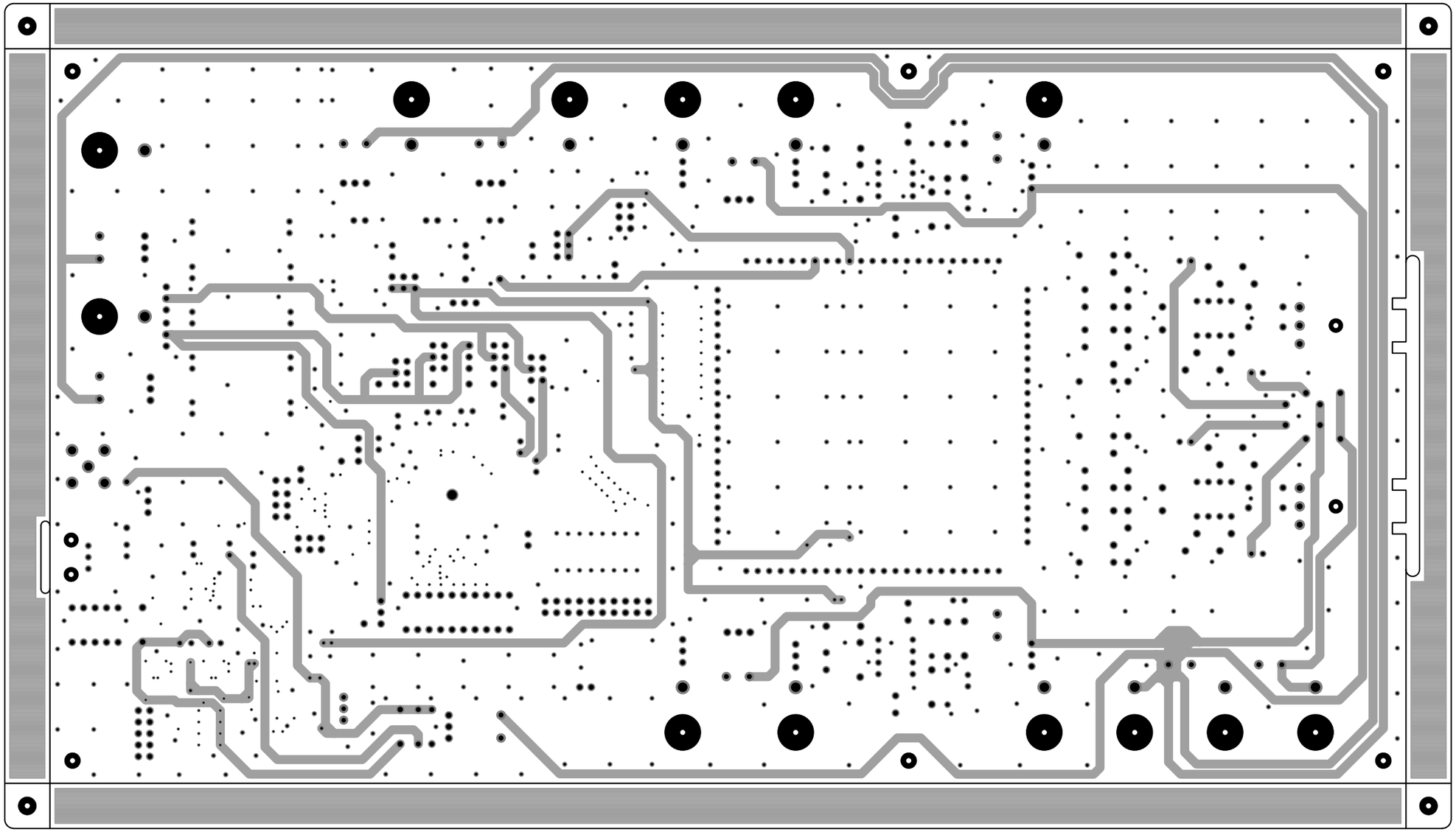
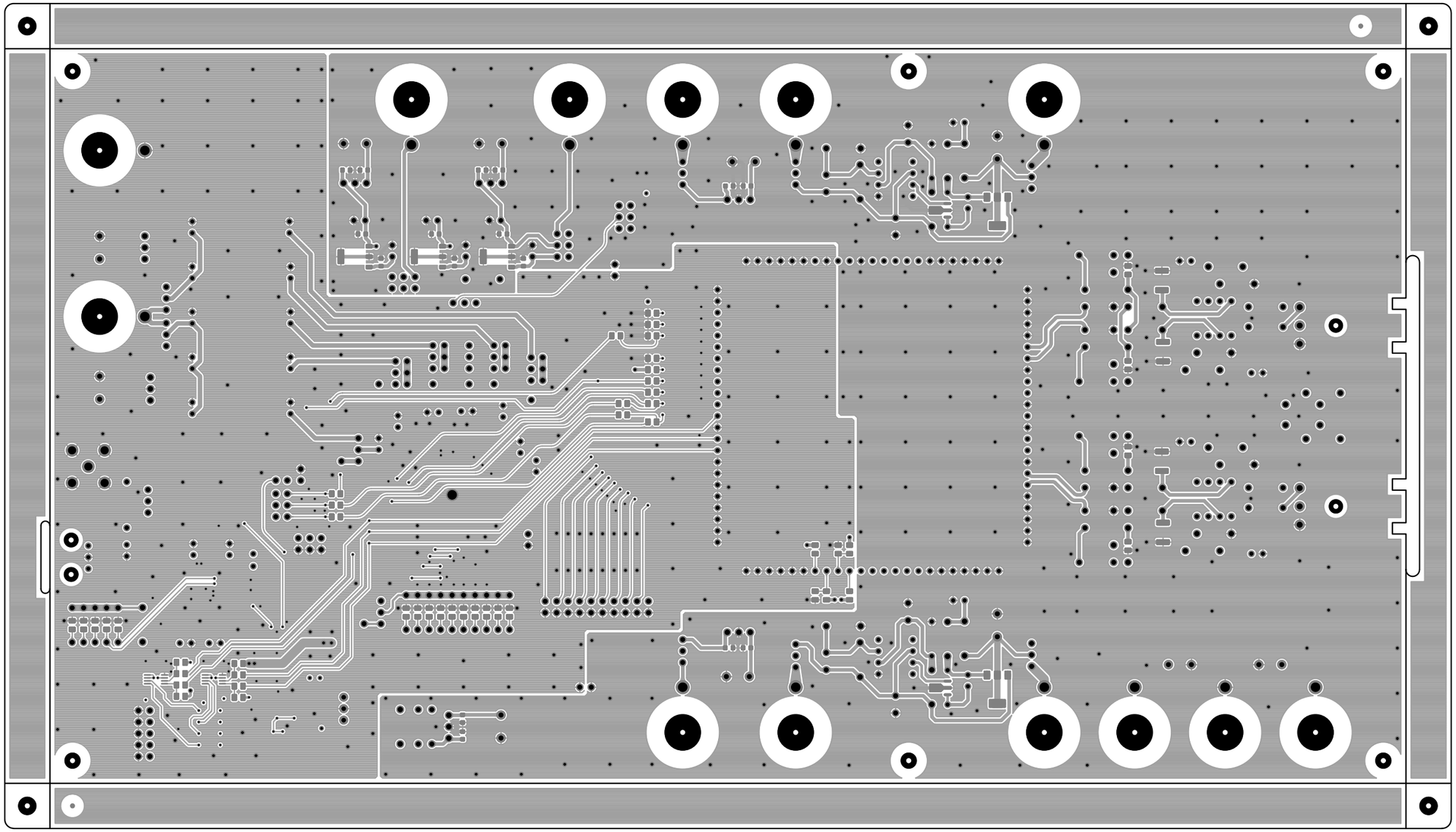


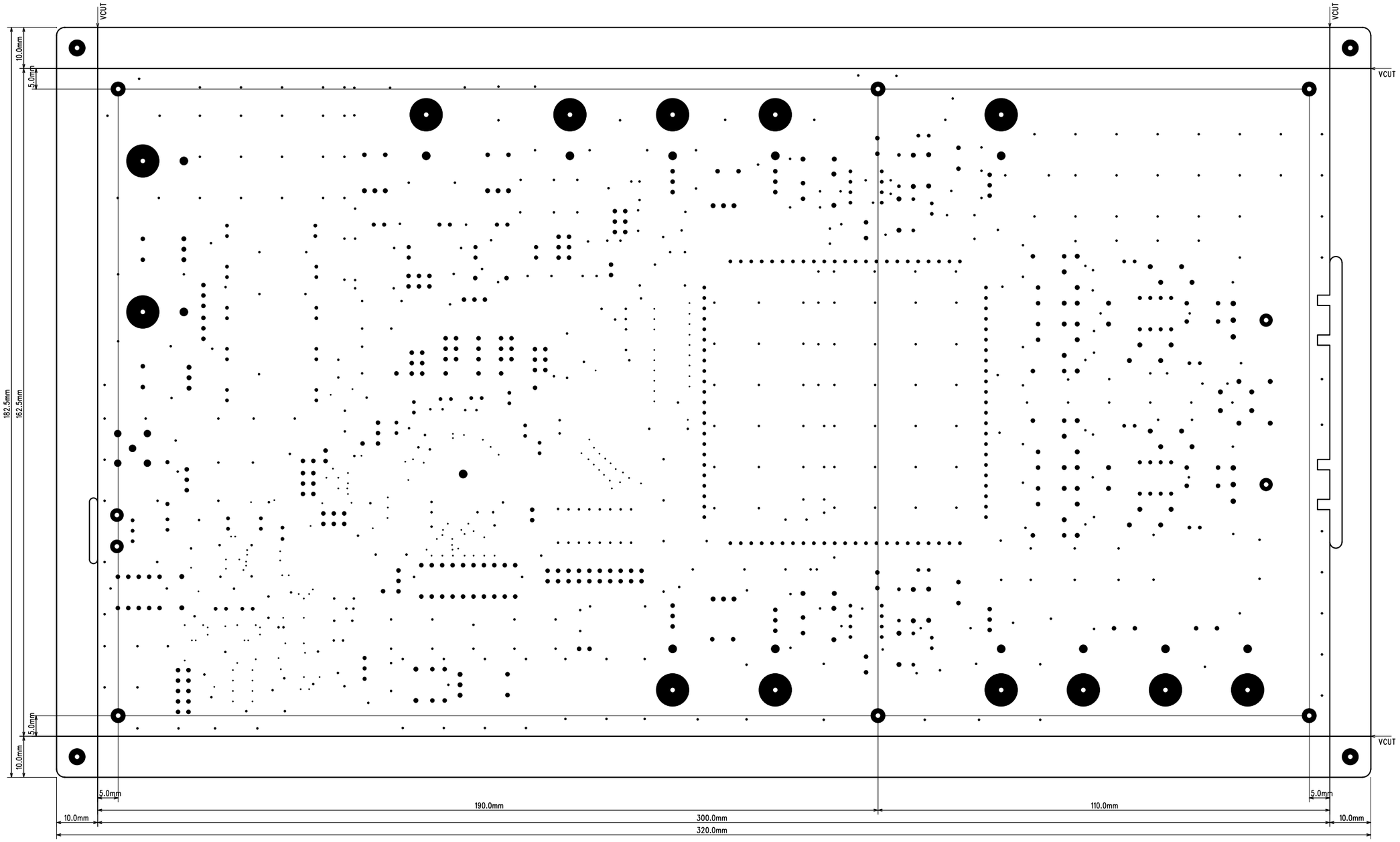
AKD449X-A-MAIN_Rev.0

半田面パターン図　　部品面透視図



AKD449X-A-MAIN_Rev.0

外形図、寸法図　　部品面透視図



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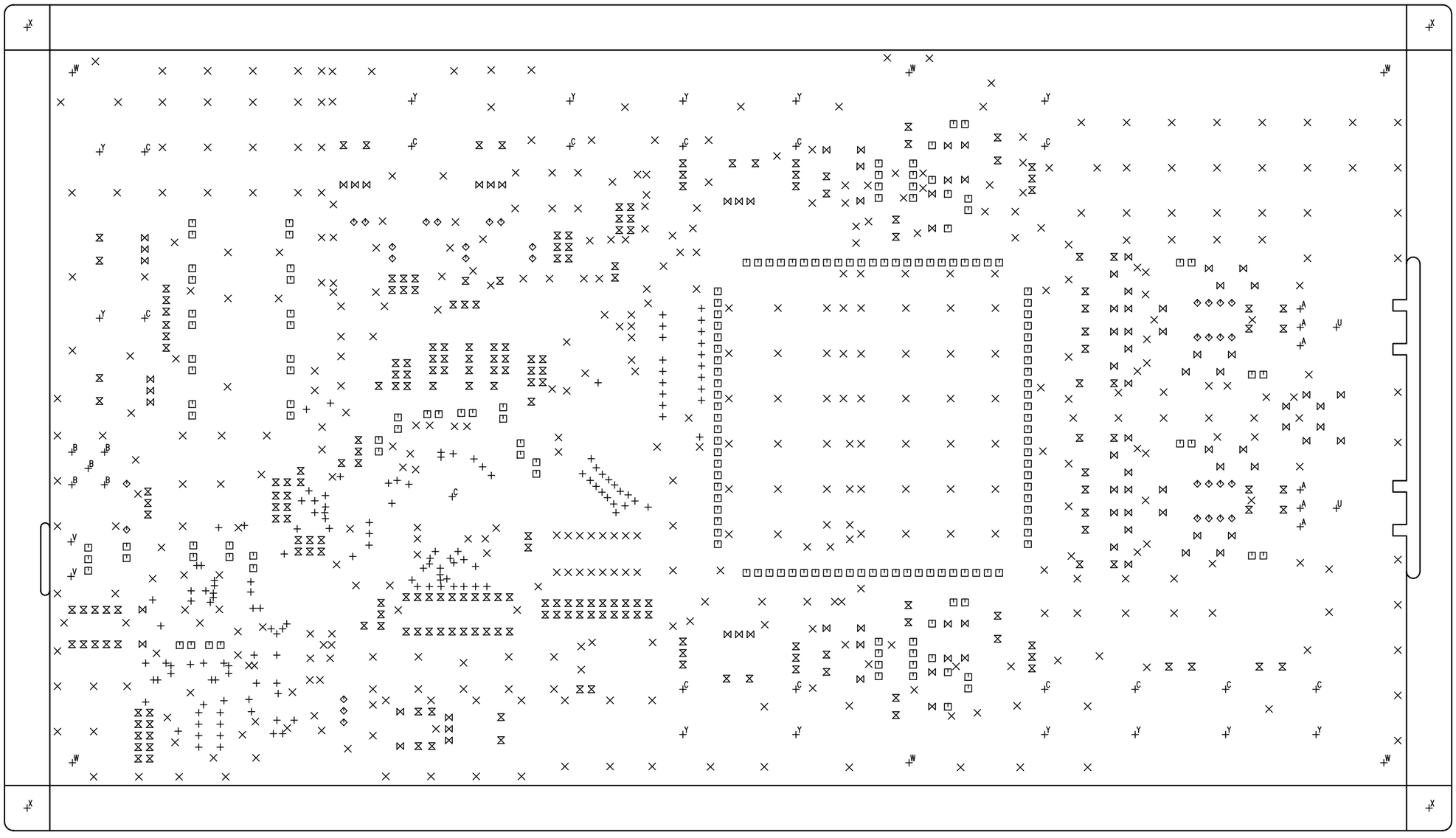
穴径図　　部品面透視図



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1.1	93	⋈	PLTD
1.2	6	A	PLTD
1.7	5	B	PLTD
2	14	C	PLTD
3.1	2	U	NPLTD
3.2	2	V	NPLTD
3.5	6	W	NPLTD
4	4	X	NPLTD
8	13	Y	NPLTD

※　ＰＬＴＤはスルーホールです。
※　ＮＰＬＴＤはノンスルーホールです。
※　穴径は全て仕上がり径でお願いいたします。
※　指示なき穴径公差は±0.05mm

AKD449X-A-MAIN_Rev.0

部品面透視図