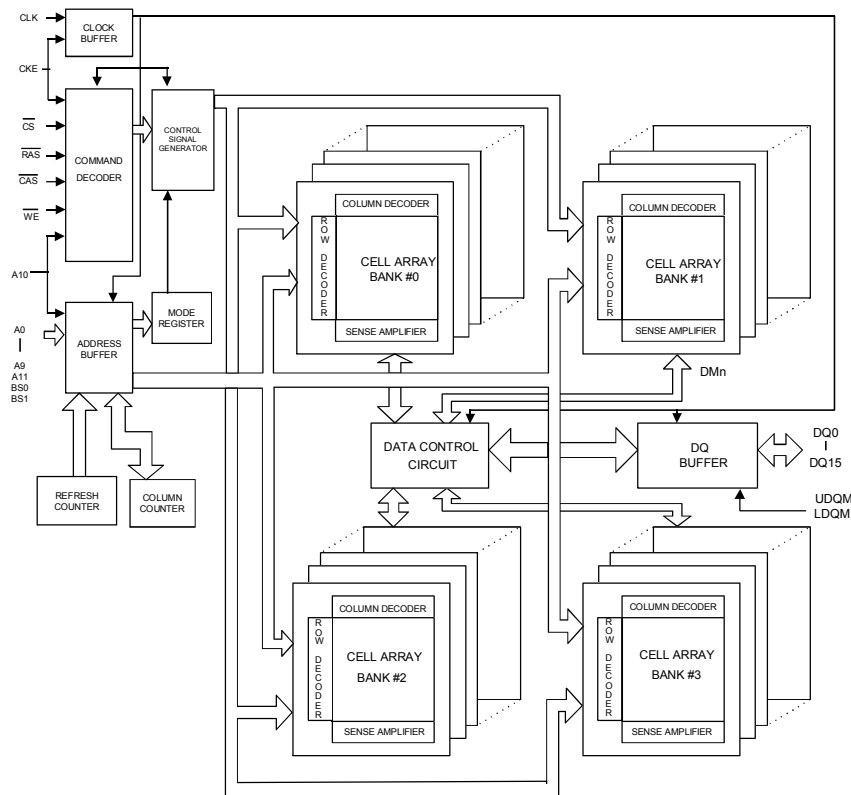
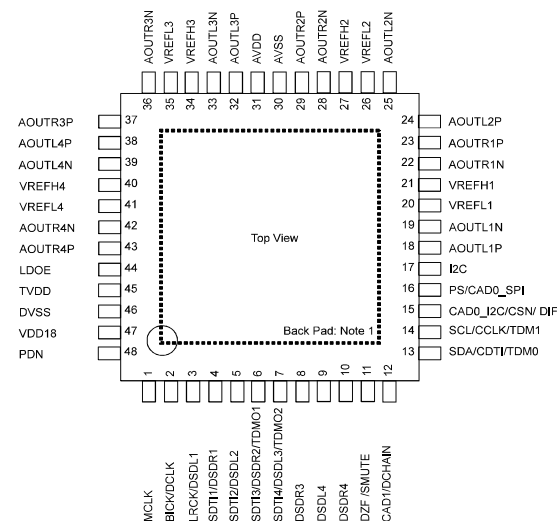


Block diagram



AK4458VN (INPUT : U1051, U1052)



Pin Function

| No. | Pin Name | I/O | Function | PD State |
|-----|----------|-----|---|----------|
| 1 | MCLK | I | External Master Clock Input Pin | Hi-Z |
| 2 | BICK | I | Audio Serial Data Clock Pin in PCM mode | Hi-Z |
| 3 | DCLK | I | DSD Clock Pin in DSD mode | Hi-Z |
| 4 | LRCK | I | Input Channel Clock Pin in PCM mode | Hi-Z |
| 5 | SDTL1 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 6 | SDTL2 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 7 | SDTL3 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 8 | SDTL4 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 9 | SDTL5 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 10 | SDTL6 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 11 | SDTL7 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 12 | SDTL8 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 13 | SDTL9 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 14 | SDTL10 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 15 | SDTL11 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 16 | SDTL12 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 17 | SDTL13 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 18 | SDTL14 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 19 | SDTL15 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 20 | SDTL16 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 21 | SDTL17 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 22 | SDTL18 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 23 | SDTL19 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 24 | SDTL20 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 25 | SDTL21 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 26 | SDTL22 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 27 | SDTL23 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 28 | SDTL24 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 29 | SDTL25 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 30 | SDTL26 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 31 | SDTL27 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 32 | SDTL28 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 33 | SDTL29 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 34 | SDTL30 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 35 | SDTL31 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 36 | SDTL32 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 37 | SDTL33 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 38 | SDTL34 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 39 | SDTL35 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 40 | SDTL36 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 41 | SDTL37 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 42 | SDTL38 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 43 | SDTL39 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 44 | SDTL40 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 45 | SDTL41 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 46 | SDTL42 | I | Audio Serial Data Input in PCM mode | Hi-Z |
| 47 | SDTL43 | I | Audio Serial Data Input in DSD mode | Hi-Z |
| 48 | SDTL44 | I | Audio Serial Data Input in PCM mode | Hi-Z |

| No. | Pin Name | I/O | Function | PD State |
|-----|----------|-----|--|----------|
| 15 | CAD0_I2C | I | Chip Address 0 Pin in I2C Bus serial control mode | Hi-Z |
| | CSN | I | Chip Select Pin in 3-wire serial control mode | |
| | DIF | I | Audio Data Format Select in Parallel control mode. "L": 32-bit MSB, "H": 32-bit I2S | |
| 16 | PS | I | (I2C pin = "H") Control Mode Select Pin "L": I2C Bus serial control mode, "H": Parallel control mode. | Hi-Z |
| | CAD0_SPI | I | (I2C pin = "L") Chip Address 0 Pin in 3-wire serial control mode | |
| 17 | I2C | I | Control Mode Select Pin "L": 3-wire serial control mode "H": I2C Bus serial control mode or Parallel control mode. | Hi-Z |
| 18 | AOUTL1P | O | Lch Positive Analog Output 1 Pin | Hi-Z |
| 19 | AOUTL1N | O | Lch Negative Analog Output 1 Pin | Hi-Z |
| 20 | VREFL1 | I | Negative Voltage Reference Input Pin, AVSS | Hi-Z |
| 21 | VREFH1 | I | Positive Voltage Reference Input Pin, AVDD | Hi-Z |
| 22 | AOUTR1N | O | Rch Negative Analog Output 1 Pin | Hi-Z |
| 23 | AOUTR1P | O | Rch Positive Analog Output 1 Pin | Hi-Z |
| 24 | AOUTL2P | O | Lch Positive Analog Output 2 Pin | Hi-Z |
| 25 | AOUTL2N | O | Lch Negative Analog Output 2 Pin | Hi-Z |
| 26 | VREFL2 | I | Negative Voltage Reference Input Pin, AVSS | Hi-Z |
| 27 | VREFH2 | I | Positive Voltage Reference Input Pin, AVDD | Hi-Z |
| 28 | AOUTR2N | O | Rch Negative Analog Output 2 Pin | Hi-Z |
| 29 | AOUTR2P | O | Rch Positive Analog Output 2 Pin | Hi-Z |
| 30 | AVSS | - | Analog Ground Pin | — |
| 31 | AVDD | - | Analog Power Supply Pin, 3.0V-5.5V | — |
| 32 | AOUTL3P | O | Lch Positive Analog Output 3 Pin | Hi-Z |
| 33 | AOUTL3N | O | Lch Negative Analog Output 3 Pin | Hi-Z |
| 34 | VREFH3 | I | Positive Voltage Reference Input Pin, AVDD | Hi-Z |
| 35 | VREFL3 | I | Negative Voltage Reference Input Pin, AVSS | Hi-Z |
| 36 | AOUTR3N | O | Rch Negative Analog Output 3 Pin | Hi-Z |
| 37 | AOUTR3P | O | Rch Positive Analog Output 3Pin | Hi-Z |
| 38 | AOUTL4P | O | Lch Positive Analog Output 4 Pin | Hi-Z |
| 39 | AOUTL4N | O | Lch Negative Analog Output 4 Pin | Hi-Z |
| 40 | VREFH4 | I | Positive Voltage Reference Input Pin, AVDD | Hi-Z |
| 41 | VREFL4 | I | Negative Voltage Reference Input Pin, AVSS | Hi-Z |
| 42 | AOUTR4N | O | Rch Negative Analog Output 4 Pin | Hi-Z |
| 43 | AOUTR4P | O | Rch Positive Analog Output 4 Pin | Hi-Z |
| 44 | LDOE | I | Internal LDO Enable Pin. "L": Disable, "H": Enable | Hi-Z |
| 45 | TVDD | - | Digital Power Supply Pin, 3.0V-3.6V | — |
| 46 | DVSS | - | Digital Ground Pin | — |
| 47 | VDD18 | O | LDO Output Pin (LDOE pin = "H") This pin should be connected to DVSS with 1.0μF. | (Note 4) |
| | | I | 1.8V Power Input Pin (LDOE pin = "L") | |
| 48 | PDN | I | Power-Down & Reset Pin When this pin is "L", the AK4458 is powered-down and the control registers are reset to default state. | Hi-Z |

Note 2. All input pins except internal pull-up/down pins should not be left floating.

Note 3. PCM mode and DSD mode are controlled by registers. Daisy Chain mode is controlled by both registers and pins.

Note 4. This pin outputs DVSS when the LDOE pin = "H" and Hi-z when the LDOE pin = "L".

FUNCTIONAL BLOCK DIAGRAM

