

### GENERAL DESCRIPTION

The AKD4440-A is an evaluation board for the AK4440, 24bit DAC with 2Vrms line output for cost and performance based audio systems. The AKD4440-A has the interface with AKM's A/D converter evaluation boards and the interface with digital audio systems via optical connector. Therefore, it is easy to evaluate the AK4440.

### ■ Ordering guide

AKD4440-A --- AK4440 Evaluation Board

### FUNCTION

- Compatible with 2 types of input data interface
  - Direct interface with AKM's A/D converter evaluation boards via 10-pin header
  - On-board AK4118 as DIR, which accepts optical or BNC Inputs
- Optical output for internal DIT
- BNC connector for an external clock input
- BNC connector for DAC output

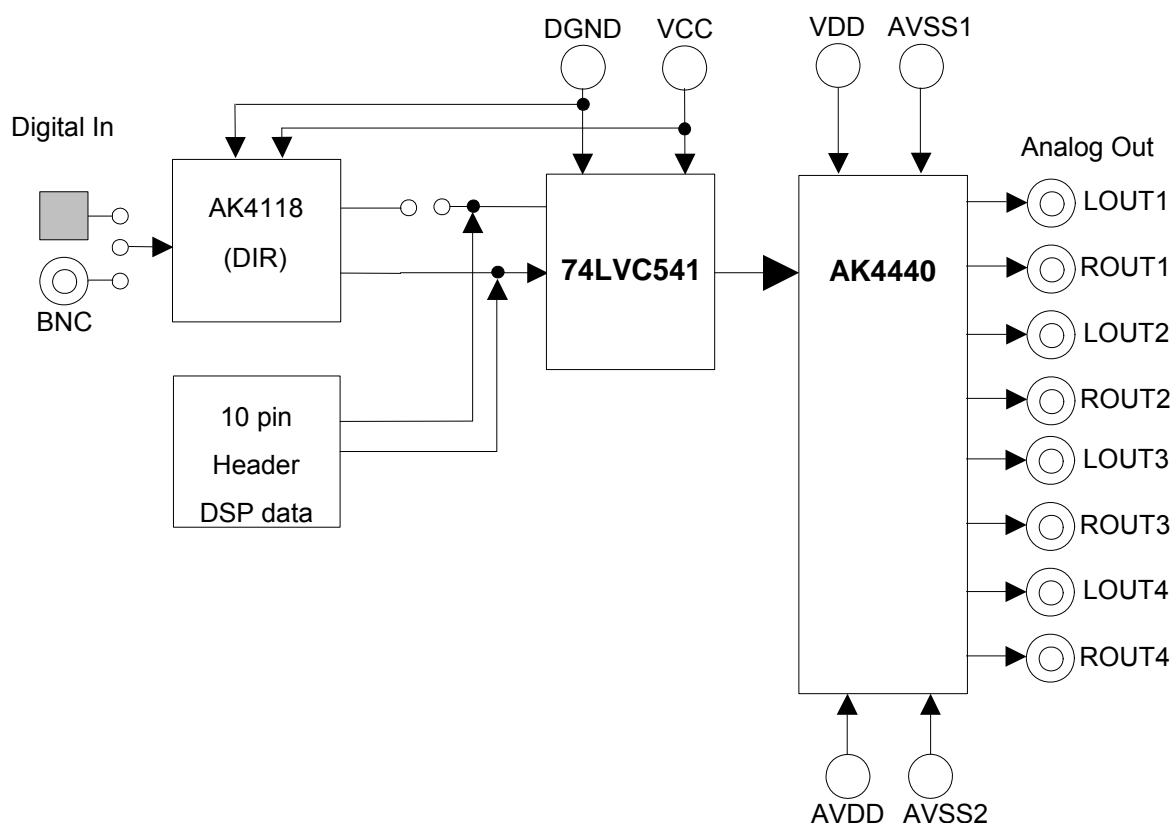


Figure 1. AKD4440-A Block Diagram

## ■ Operation sequence

### 1) Set up the power supply lines.

[VDD]	(Red)	= 4.5 ~ 5.5V (typ. 5.0V, for AK4440)
[VCC]	(Red)	= 2.7 ~ 3.6V (typ. 3.3V, for AK4118, for 74LVC541 and for logic)
[AVDD]	(Red)	= 4.5 ~ 5.5V (typ. 5.0V, AK4440)
[AVSS1]	(Black)	= 0V
[AVSS2]	(Black)	= 0V
[DGND]	(Black)	= 0V

Each supply line should be distributed from the power supply unit.

### 2) Set-up the evaluation modes, jumper pins and DIP switches (See the followings.)

### 3) Power on.

When AK4118 is used, The AK4118 should be reset once by bringing SW2 “L” upon power-up.

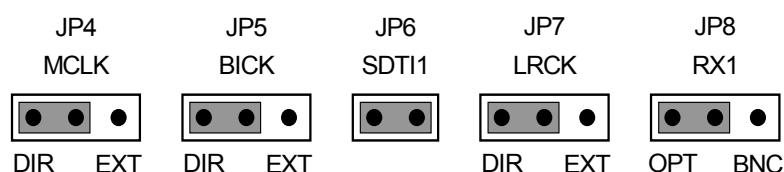
## ■ Evaluation mode

### 1) D/A part evaluation using optical or S/PDIF input <Default>

Use PORT1 (RX3: OPT) or J2 (RX3: BNC).

The AK4118 (DIR) generates MCLK, BICK, LRCK and SDTI from the received data through Optical connector (TORX141) or BNC connector. This evaluation mode should be used for the evaluation using CD test disk.

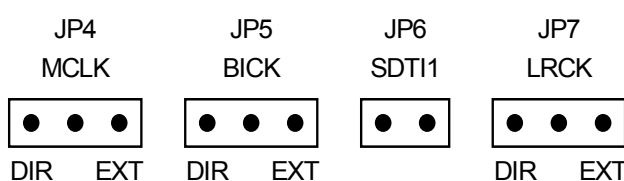
Nothing should be connected to PORT3 (DSP). The selection of OPT and BNC should be done by JP8 (RX1)



### 2) D/A part evaluation using 10-pin connector on the AKM's A/D evaluation board

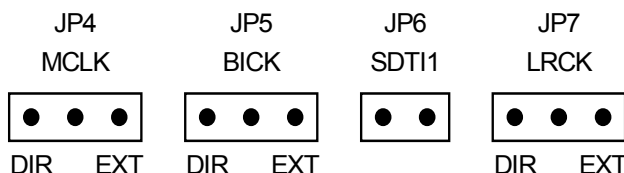
Use PORT3 (DSP).

It is able to evaluate the AK4440, connecting the 10-pin connector on the AKM's A/D evaluation board and PORT3 (DSP) via 10-line flat cable. MCLK, BICK, LRCK and SDTI are sent from the A/D converter evaluation board to the AKD4440 through PORT3 (DSP) via 10-line flat cable.



### 3) D/A part evaluation using PORT3 (DSP), and supplying all interface signals from external equipments

In case of using PORT3 (DSP), and supplying signals (MCLK, BICK, LRCK, SDTI) that is needed for the AK4440 from external equipments, set up as following.



## ■ Other Jumper pins set up

- (1) JP1 (SDTI1): Select the input of SDTI2 pin  
 OPEN: Separated  
 SHORT: <Default>
- (2) JP2 (SDTI1): Select the input of SDTI3 pin  
 OPEN: Separated  
 SHORT: <Default>
- (3) JP3 (SDTI1): Select the input of SDTI4 pin  
 OPEN: Separated  
 SHORT: <Default>
- (4) JP14 (VDD): VDD and VCC  
 OPEN: Separated <Default>  
 SHORT: Prohibition
- (5) JP15 (VDD): VDD and AVDD  
 OPEN: Separated <Default>  
 SHORT: Prohibition
- (6) JP16 (GND): Analog ground and Digital ground  
 OPEN: Separated <Default>  
 SHORT: Prohibition

## ■ DIP Switch set up

[S1]: AK4118 Setting

No.	Pin	L	H	Default
1	DIF1	Setting of AK4118 Audio Interface Format (Refer Table 2.)		L
2	DIF0			L
3	OCKS1	Selection of AK4118 Master Clock Output frequency (Refer Table 3.)		H
4	OCKS0			L

Table 1. Set up modes of AK4118

Mode	DIF1	DIF0	SDTO	(Default)
4	L	L	24bit, Left justified	(Default)
5	L	H	24bit, I <sup>2</sup> S	

Table 2. Audio Data Format of AK4118

OCKS1	OCKS0	MCKO1	fs (max)	(Default)
L	L	256fs	96kHz	(Default)
H	L	512fs	48kHz	
H	H	128fs	192kHz	

Table 3. MCLK Frequency of AK4118

[SW2]: AK4440 Setting

No.	Pin	OFF (L)	ON (H)	Default
1	SMUTE	Soft Mute Pin in parallel mode : “Disable”	Soft Mute Pin in parallel mode : “Enable”	OFF
2	ACKS	Normal Speed Mode (Parallel control mode)	Auto setting mode (Parallel control mode)	OFF
3	DIF0	24-bit MSB (Parallel control mode)	24-bit I <sup>2</sup> S (Parallel control mode)	OFF
4	TDM0B	TDM256 mode (Parallel control mode)	Normal mode (Parallel control mode)	ON
5	DEM0	De-emphasis Filter Enable Pin in parallel mode. This pin is valid in parallel mode. (Refer Table 5.)		ON
6	DEM1/I2S	De-emphasis Filter Enable Pin in parallel mode. This pin is valid in parallel mode. (Refer Table 5.)		OFF
7	P/S	Serial control mode	Parallel control mode	OFF

Table 4. SW2 set-up

DEM1 pin	DEM0 pin	Mode	(Default)
0	0	44.1kHz	(Default)
0	1	OFF	
1	0	48kHz	
1	1	32kHz	

Table 5. De-emphasis Filter Control (Normal Speed Mode)

## ■ Toggle switch

[SW2] AK4118-PDN:

Switch for power down reset of AK4118. Keep “H” during operation of AK4118.

Power down reset of AK4118 will be done by setting SW2 to “L” once, after power on.

## ■ Register control

AKD4440 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (uP-I/F) to PC by 10-line flat cable packed with this. Take care of the direction of connector. There is a mark at connector. Connect the mark of 10-pin connector to pin1 of PORT3. (Figure 2.)

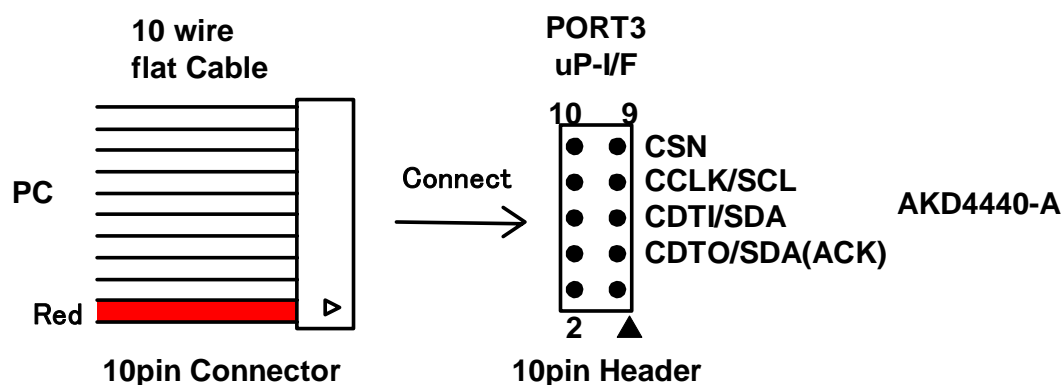


Figure 2. PORT3 pin layout

## ■ Analog Output Circuit

The DAC of AK4440 outputs analog audio signals through J3 and J4.

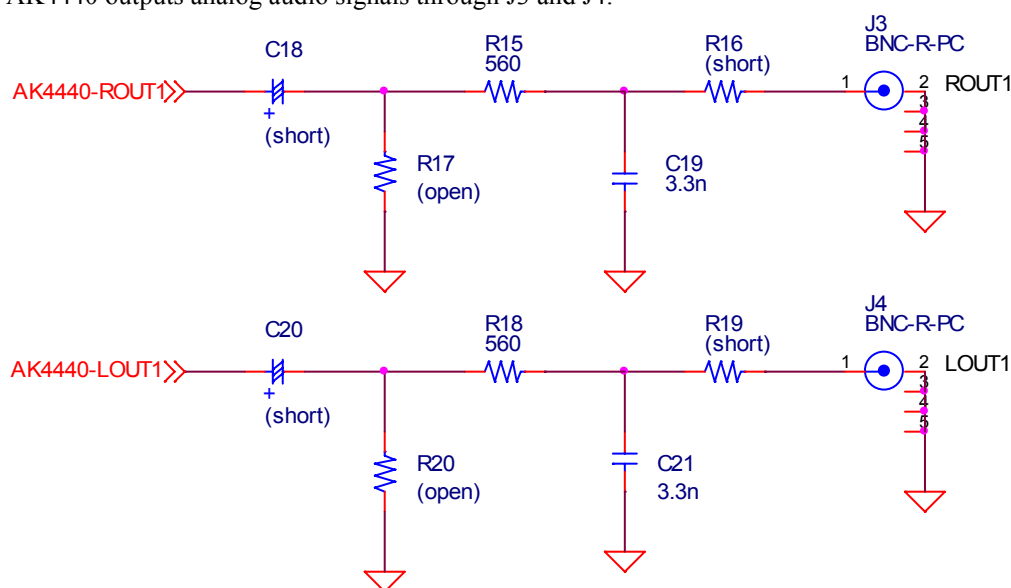


Figure 3. LOUT/ROUT Output circuit

\* AKM assumes no responsibility for the trouble when using the above circuit examples.

## Control Soft Manual

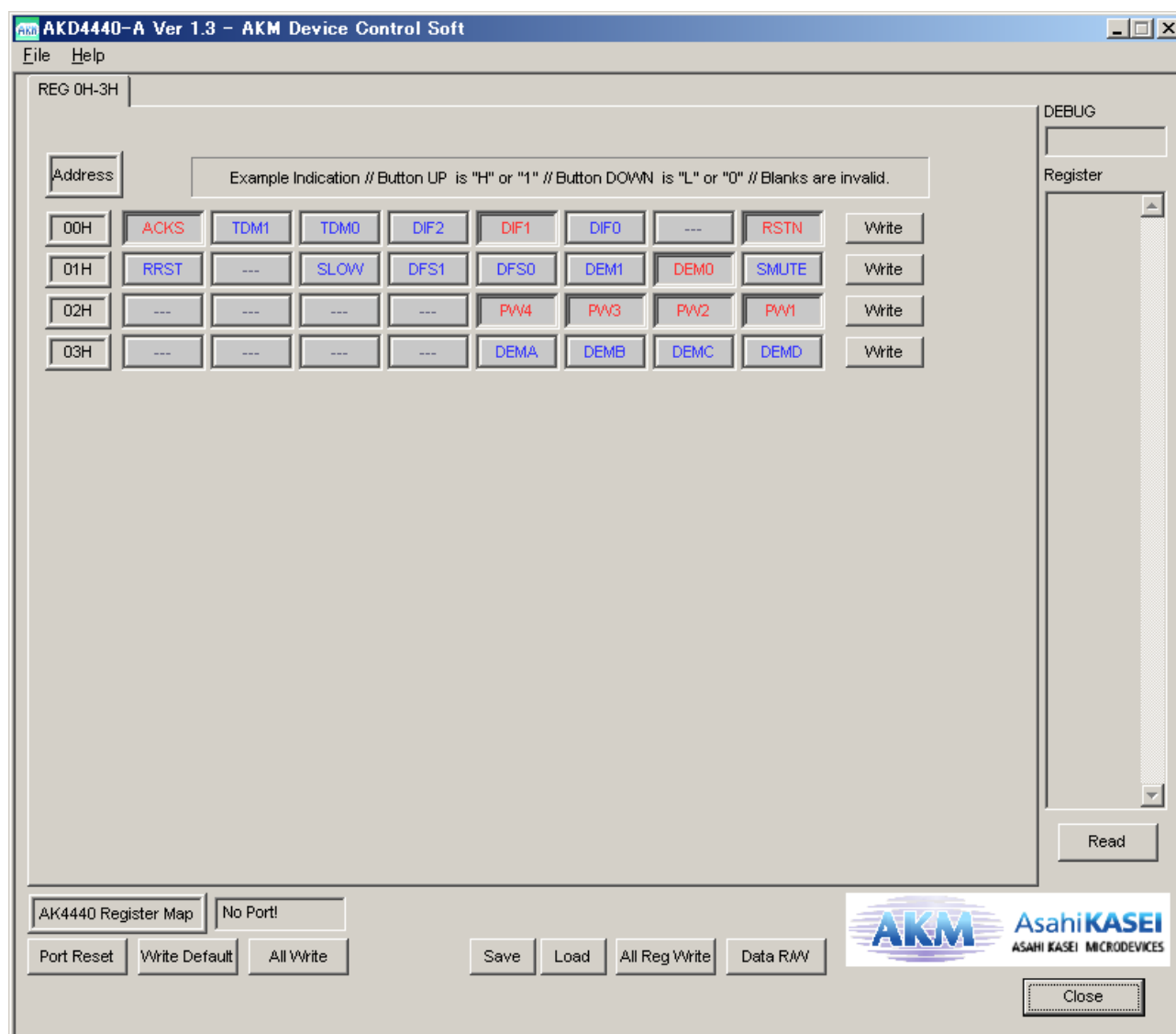
### ■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

### ■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.



## ■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)  
Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default]: Register Initializing  
When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write]: Executing write commands for all registers displayed.
4. [Save]: Saving current register settings to a file.
5. [Load]: Executing data write from a saved file.
6. [All Req Write]: “All Req Write” dialog box is popped up.
7. [Data R/W]: “Data R/W” dialog box is popped up.
8. [Read]: Reading current register settings and display on to the Register area (on the right of the main window).  
This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

## ■ Tab Functions

### 1. [REG]: Register Map

This tab is for a register writing and reading.

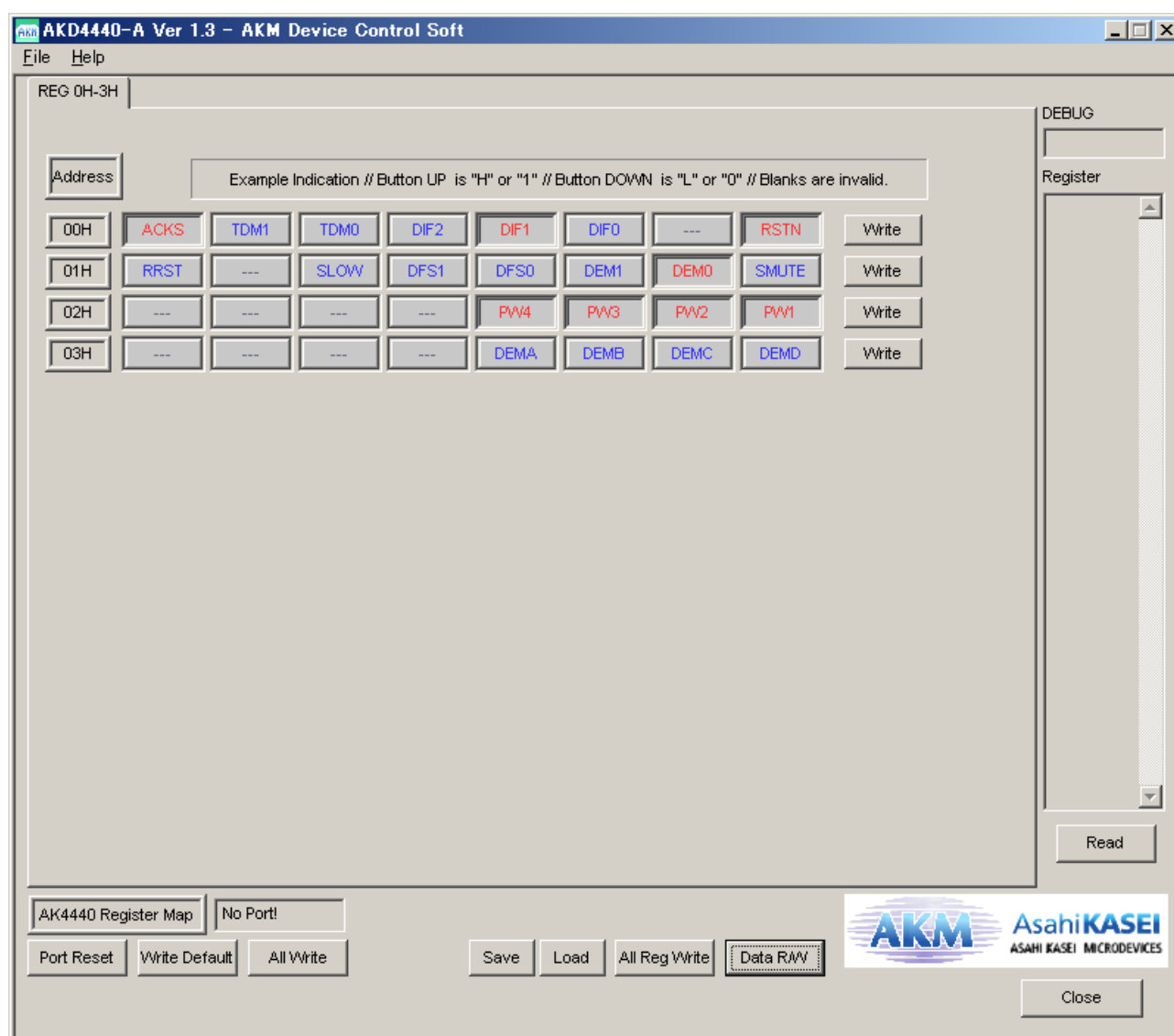
Each bit on the register map is a push-button switch.

Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).

Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.



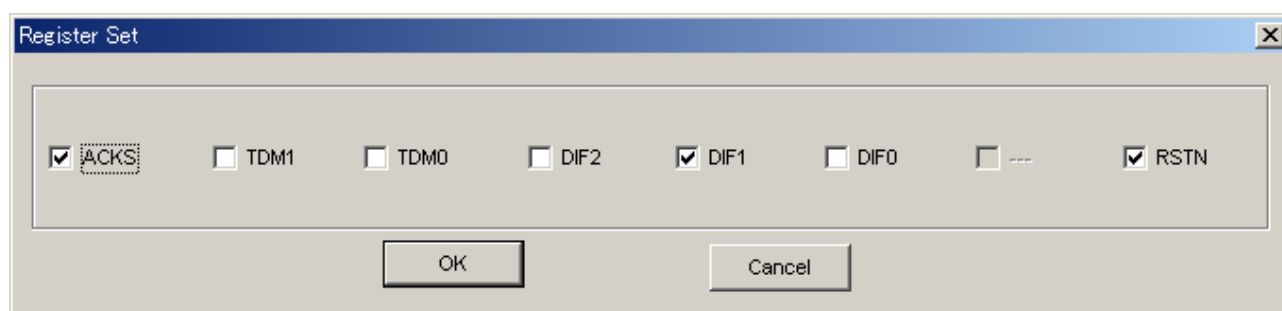


**[Write]: Data Writing Dialog**

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or “0”.  
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

**[Read]: Data Read**

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.

Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).

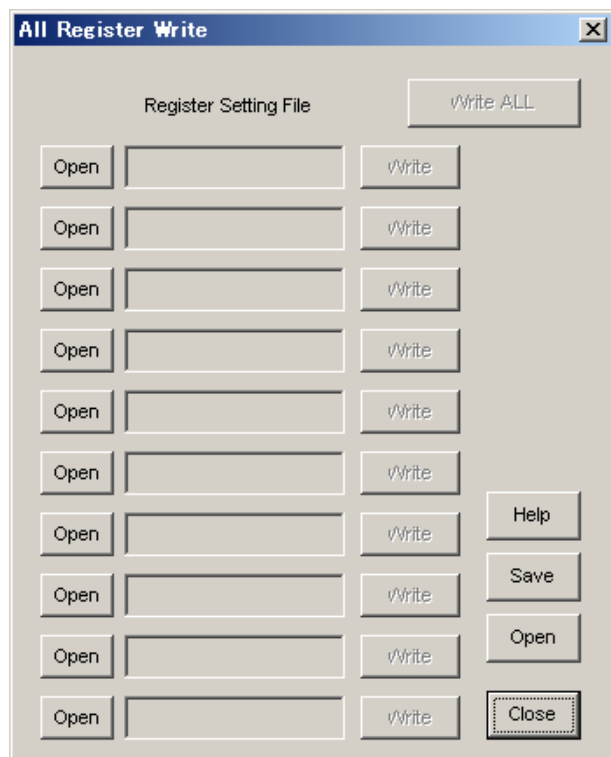
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

## ■ Dialog Boxes

### 1. [All Reg Write]: All Reg Write dialog box

Click [All Reg Write] button in the main window to open register setting files.  
Register setting files saved by [SAVE] button can be applied.



[Open (left)]: Selecting a register setting file (\*.akr).

[Write]: Executing register writing.

[Write All]: Executing all register writings.

Writings are executed in descending order.

[Help]: Help window is popped up.

[Save]: Saving the register setting file assignment. The file name is "\*.mar".

[Open (right)]: Opening a saved register setting file assignment "\*.mar".

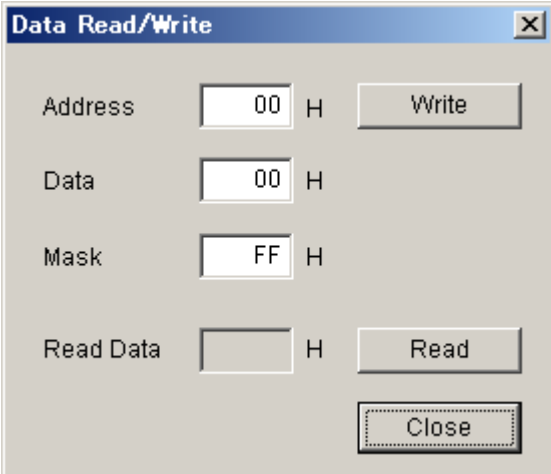
[Close]: Closing the dialog box and finish the process.

#### \*Operating Suggestions

- (1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "\*.mar" should be stored in the same folder.
- (2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

## 2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.  
Data write is available to specified address.

The image shows a 'Data Read/Write' dialog box with a title bar and a close button. It contains four input fields: 'Address' with '00' and 'H', 'Data' with '00' and 'H', 'Mask' with 'FF' and 'H', and 'Read Data' which is empty and followed by 'H'. To the right of the 'Address' field is a 'Write' button. To the right of the 'Read Data' field is a 'Read' button. At the bottom center is a 'Close' button.

Address Box: Input data address in hexadecimal numbers for data writing.

Data Box: Input data in hexadecimal numbers.

Mask Box: Input mask data in hexadecimal numbers.

This is "AND" processed input data.

[Write]: Writing to the address specified by "Address" box.

[Read]: Reading from the address specified by "Address" box.

The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Closing the dialog box and finish the process.

Data writing can be cancelled by this button instead of [Write] button.

\*The register map will be updated after executing [Write] or [Read] commands.

<b>Measurement Results</b>
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## [Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs, 256fs, 128fs
- BICK : 64fs
- Fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : VDD=AVDD=5V
- Interface : DIR
- Temperature : Room

**Table Data (DAC1 ON)**

MCLK=512fs, fs=44.1kHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	20kHz LPF	93.7	93.2
DR	1kHz, -60dB	20kHz SPCL, A-weighted	105.5	105.3
S/N	“0” data	20kHz SPCL, A-weighted	105.5	105.5

MCLK=256fs, fs=96kHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	20kHz LPF	92.8	92.1
DR	1kHz, -60dB	40kHz SPCL A-weighted	105.2	105.1
S/N	“0” data	40kHz SPCL A-weighted	105.5	105.5

MCLK=128fs, fs=192kHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	92.3	92.1
DR	1kHz, -60dB	40kHz SPCL A-weighted	103.3	103.3
S/N	“0” data	40kHz SPCL A-weighted	105.3	105.3

## Plot Data

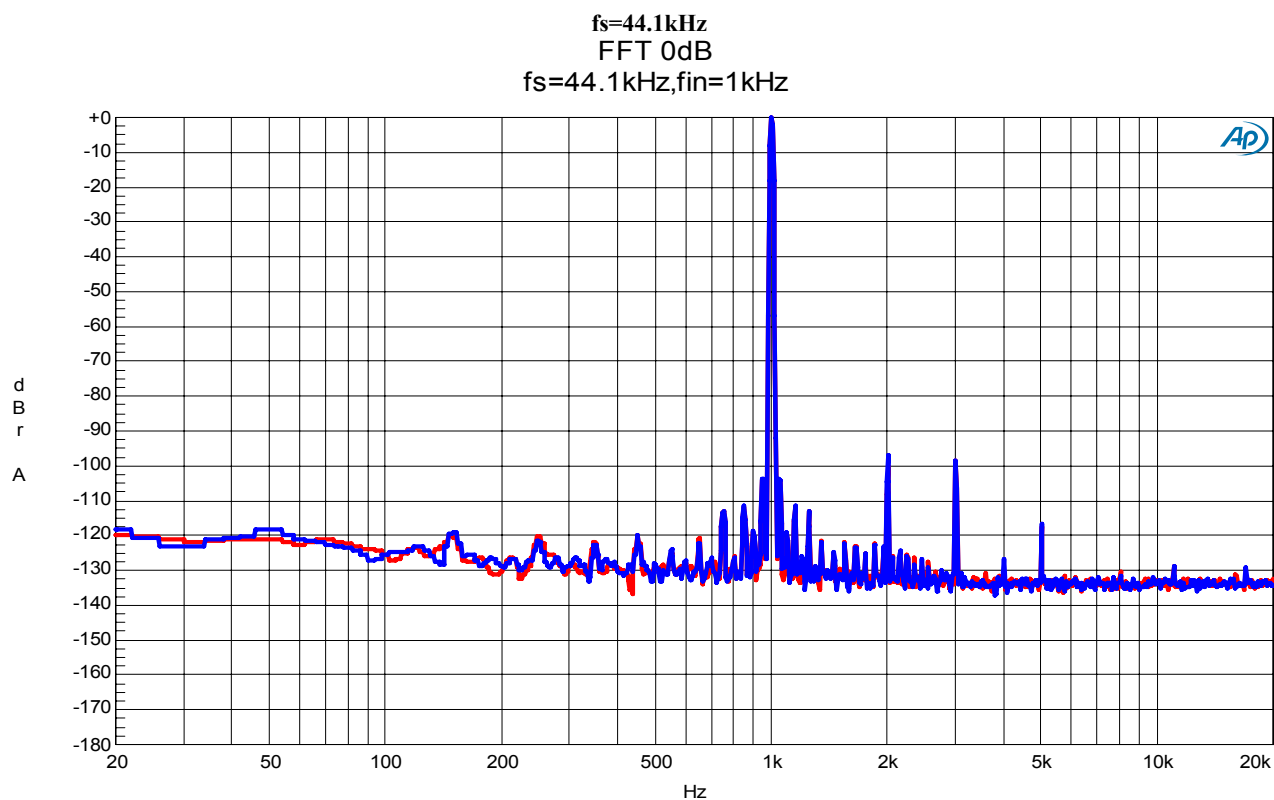


Figure 4. FFT (0dB)

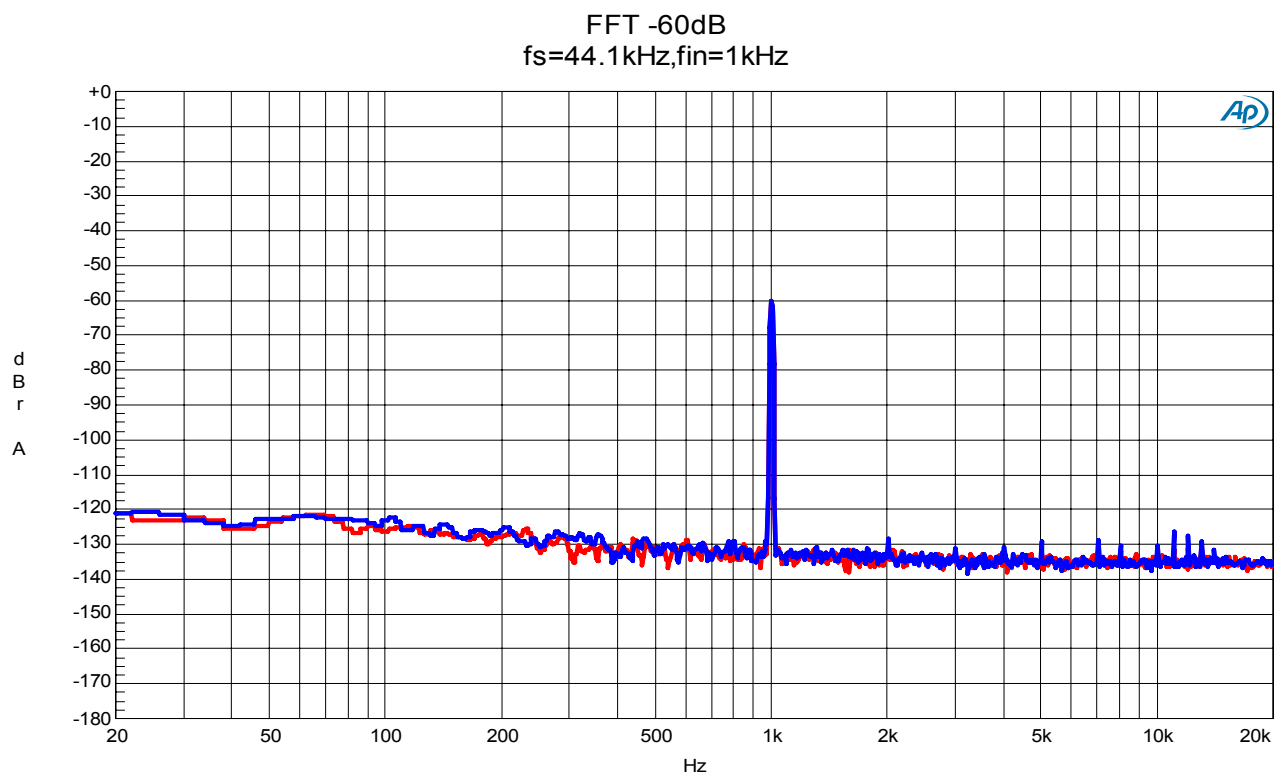


Figure 5. FFT (-60dB)

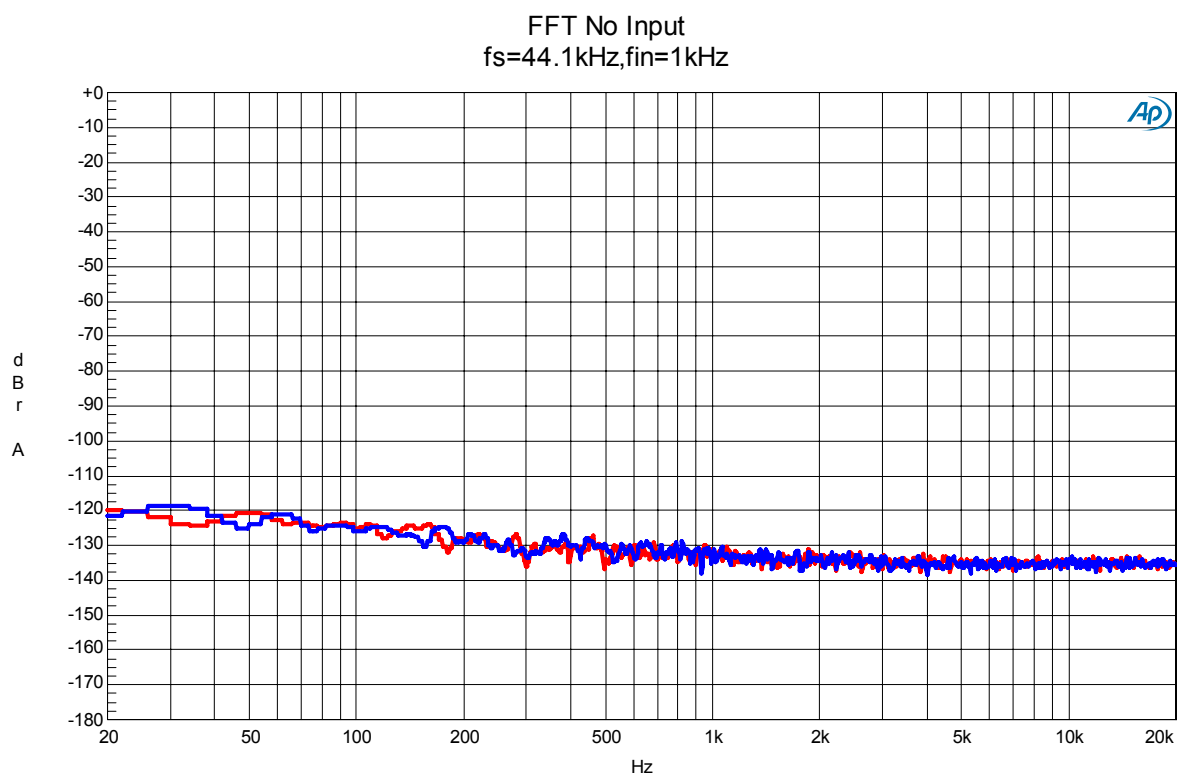


Figure 6. FFT (No Signal)

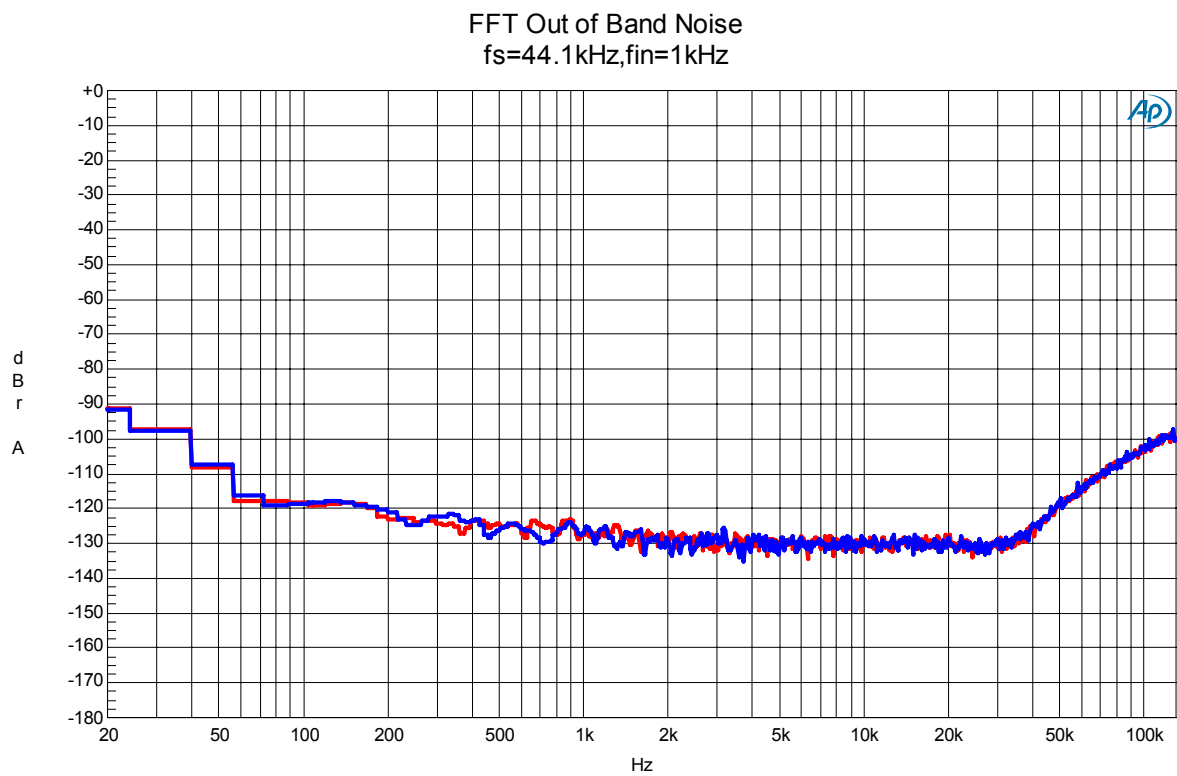


Figure 7. FFT (Out of Band Noise)

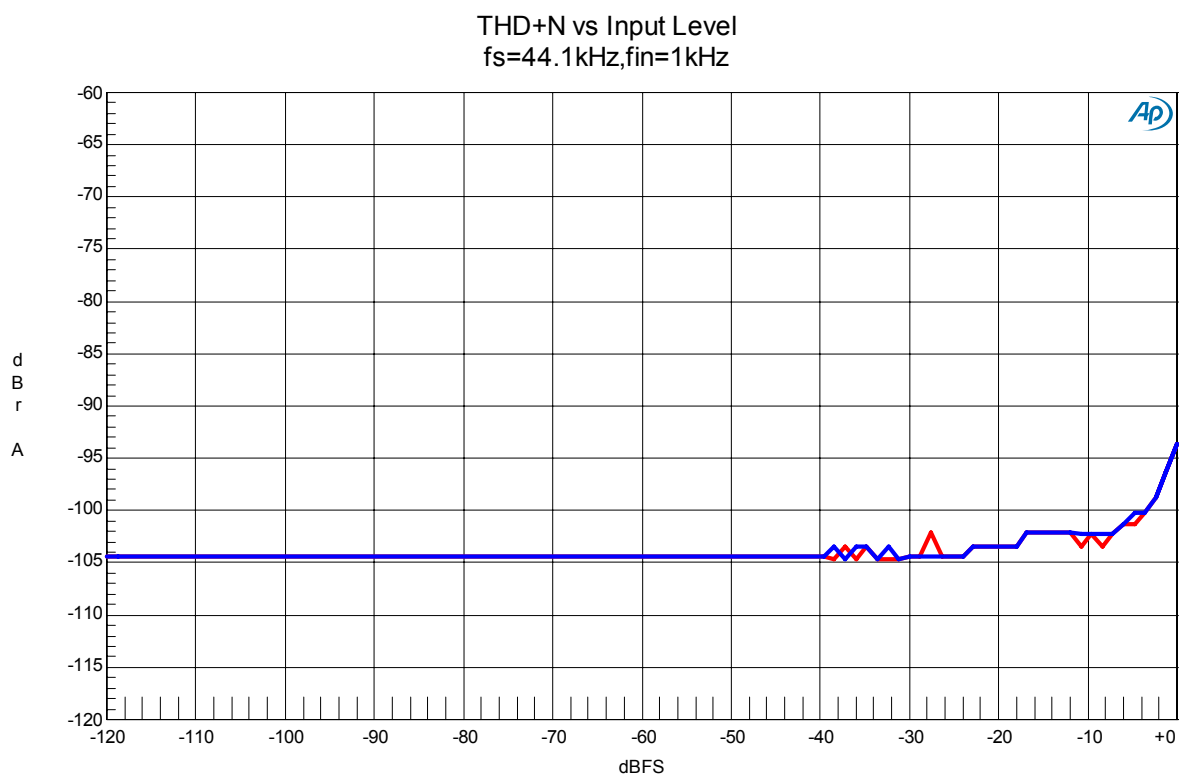


Figure 8. THD + N vs Input Level

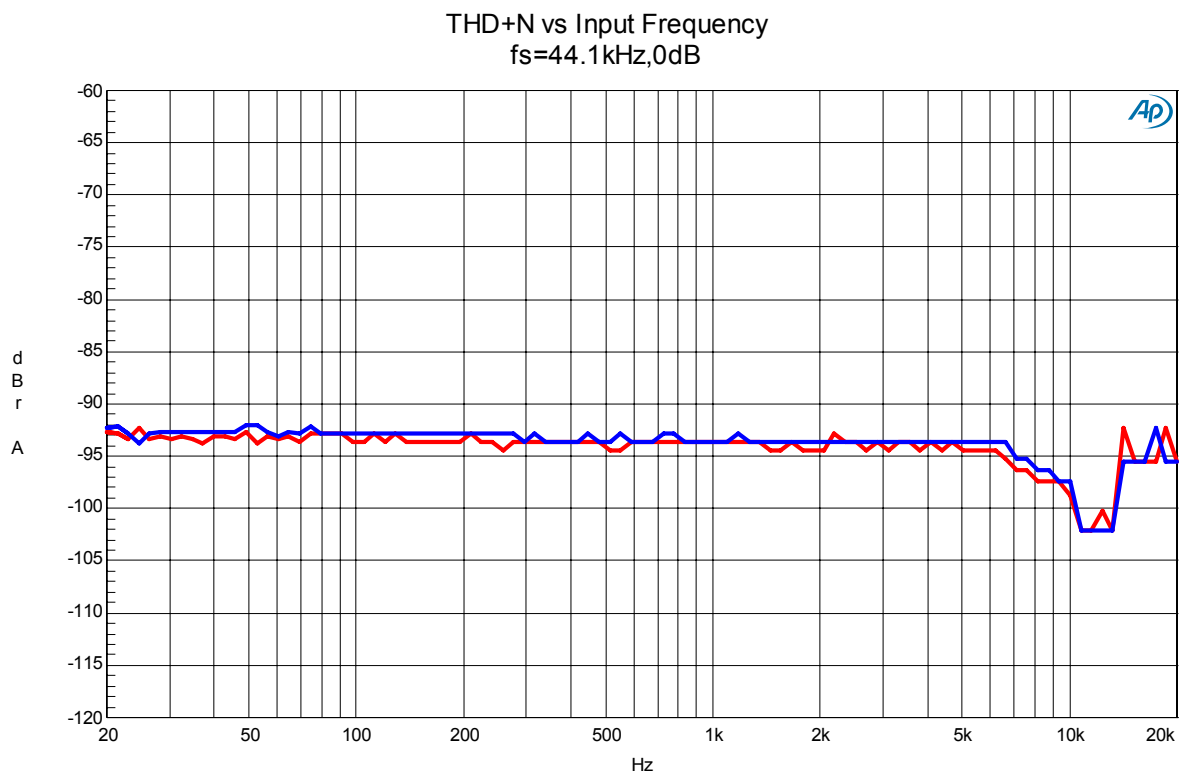


Figure 9. THD + N vs Input Frequency

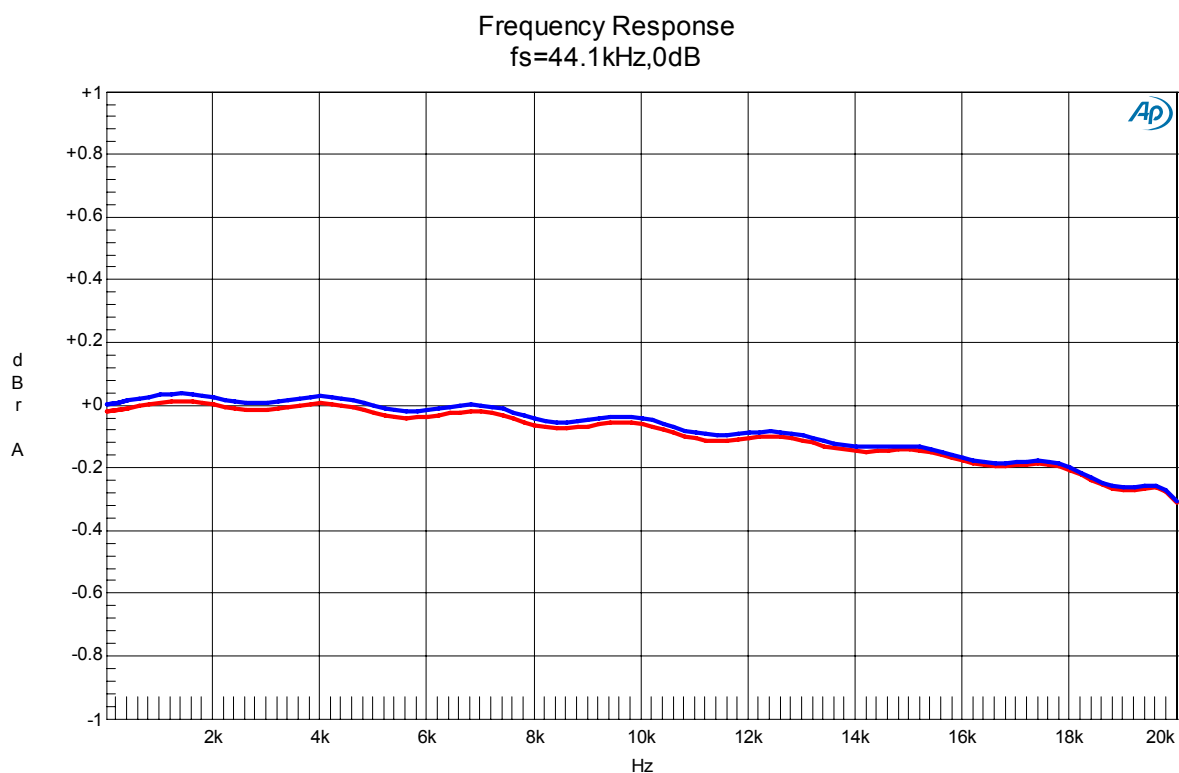


Figure 10. Frequency Response

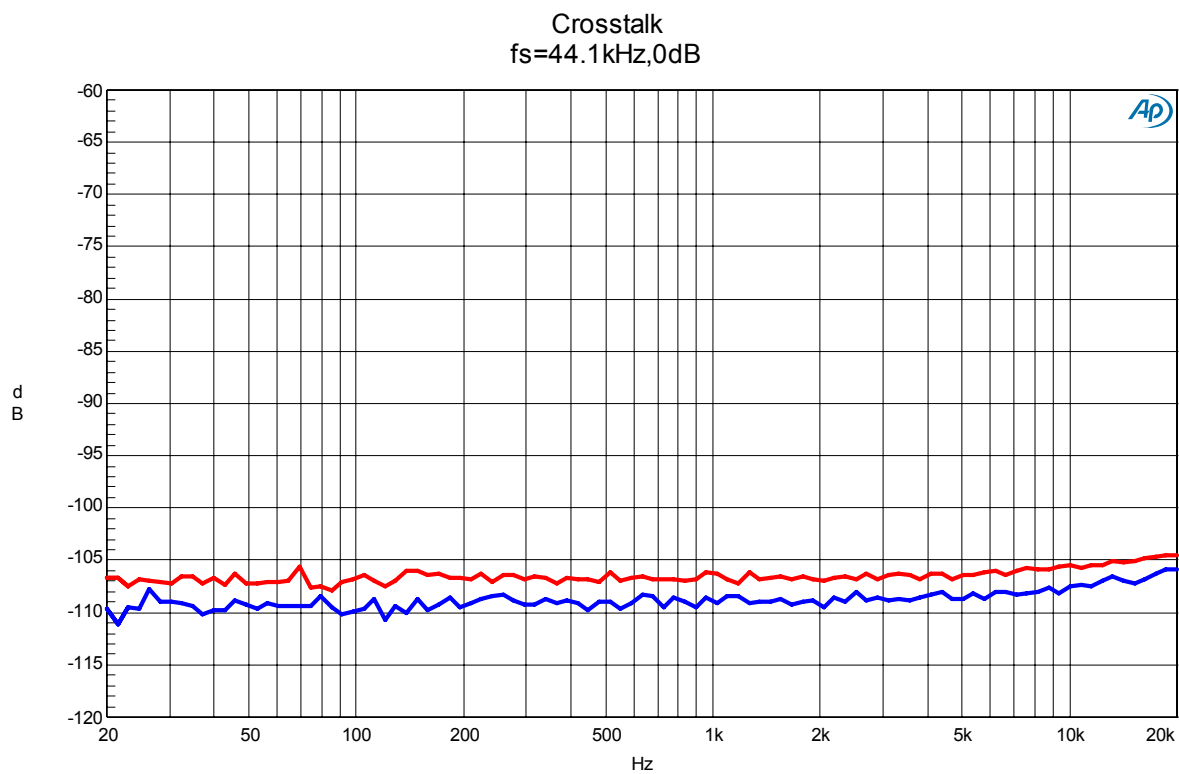


Figure 11. Crosstalk



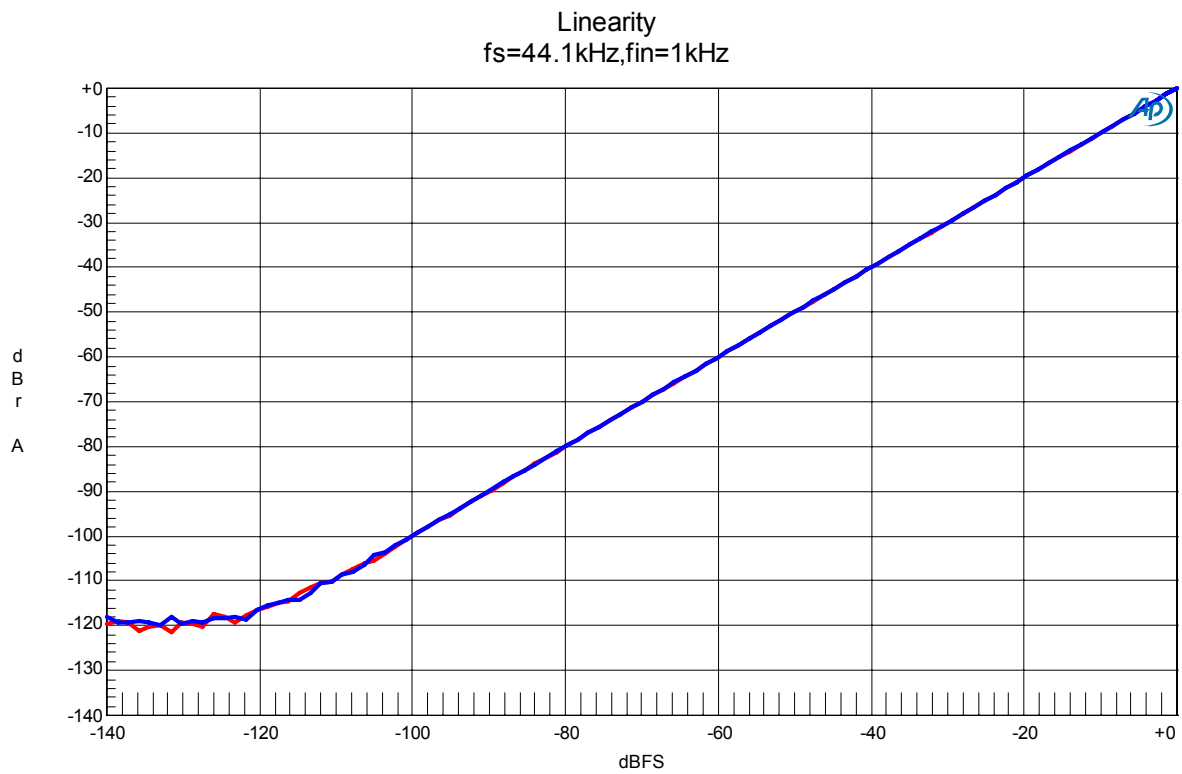


Figure 12. Linearity

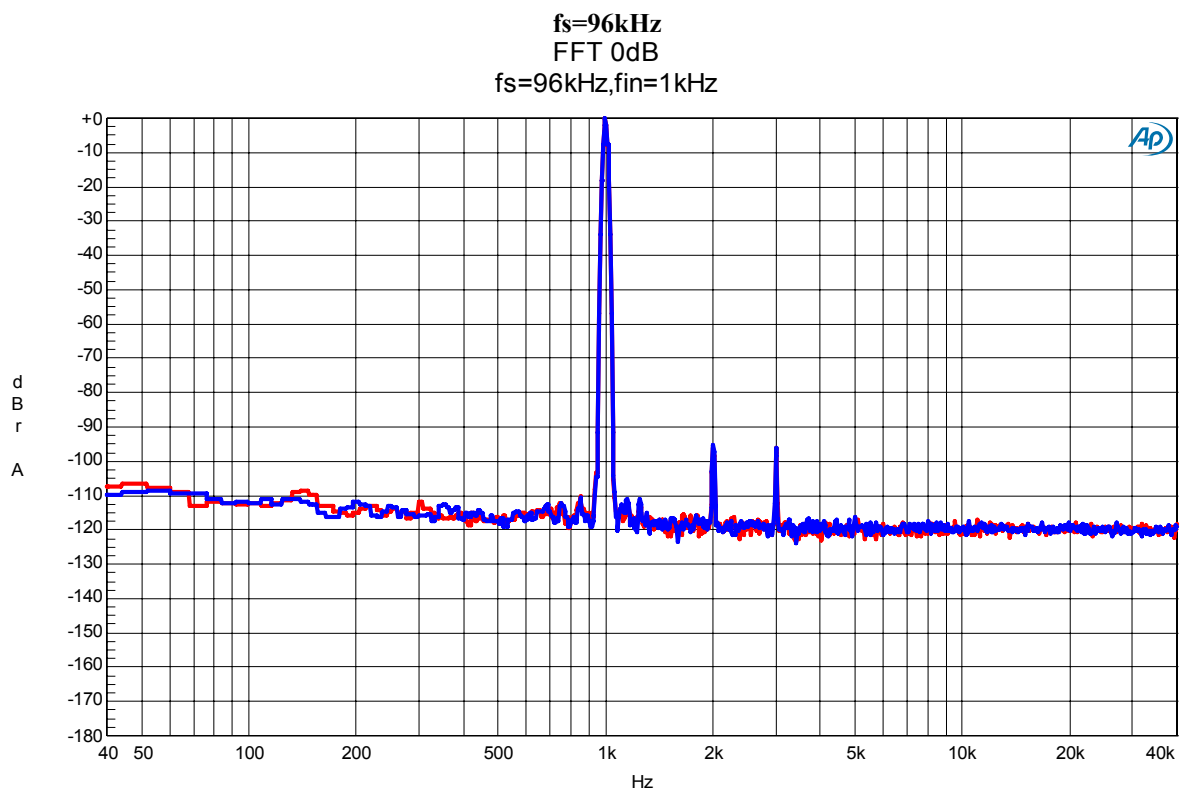
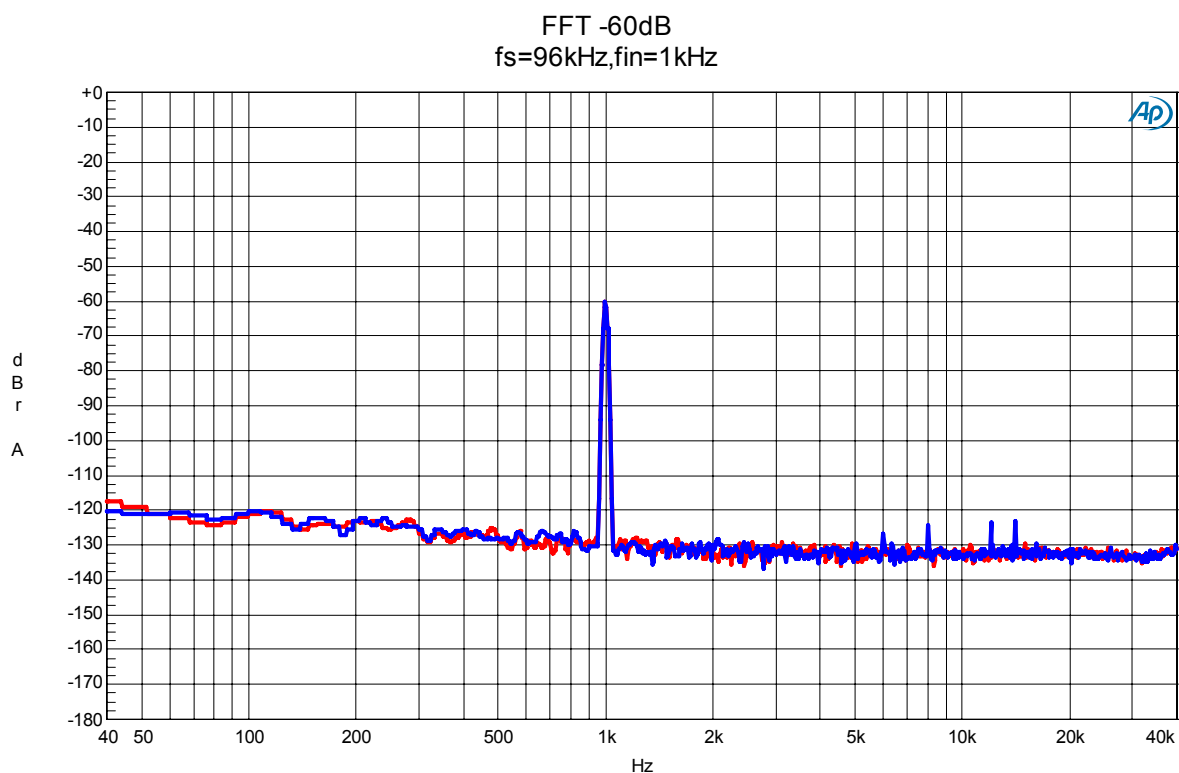
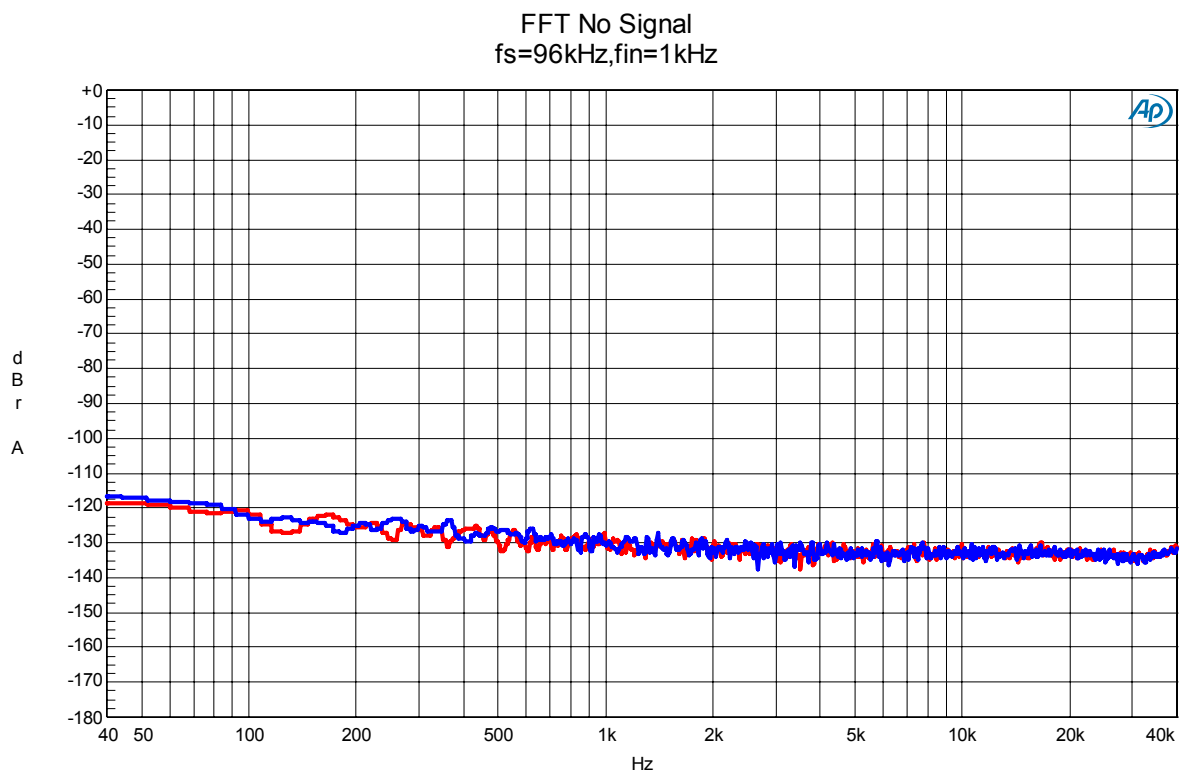


Figure 13.FFT(0dB)

**Figure 14. FFT (-60dB)****Figure 15.FFT(No Signal)**

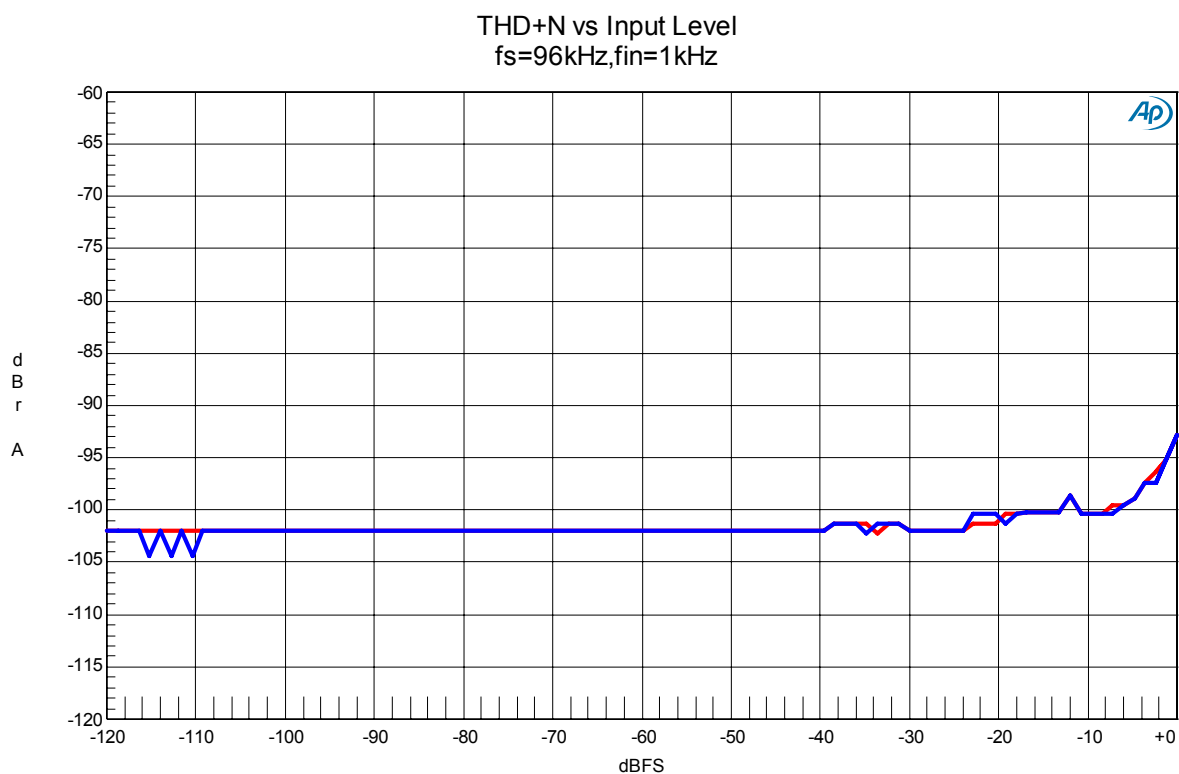


Figure 16. THD+N vs Input Level

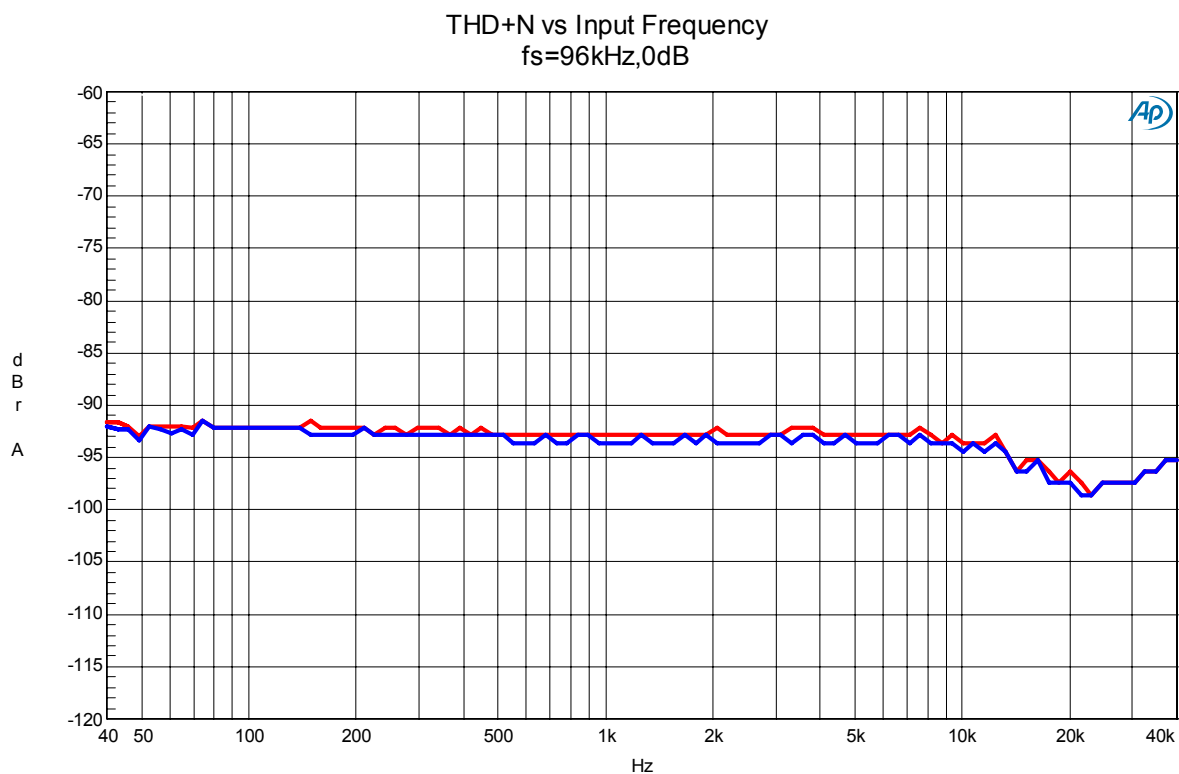
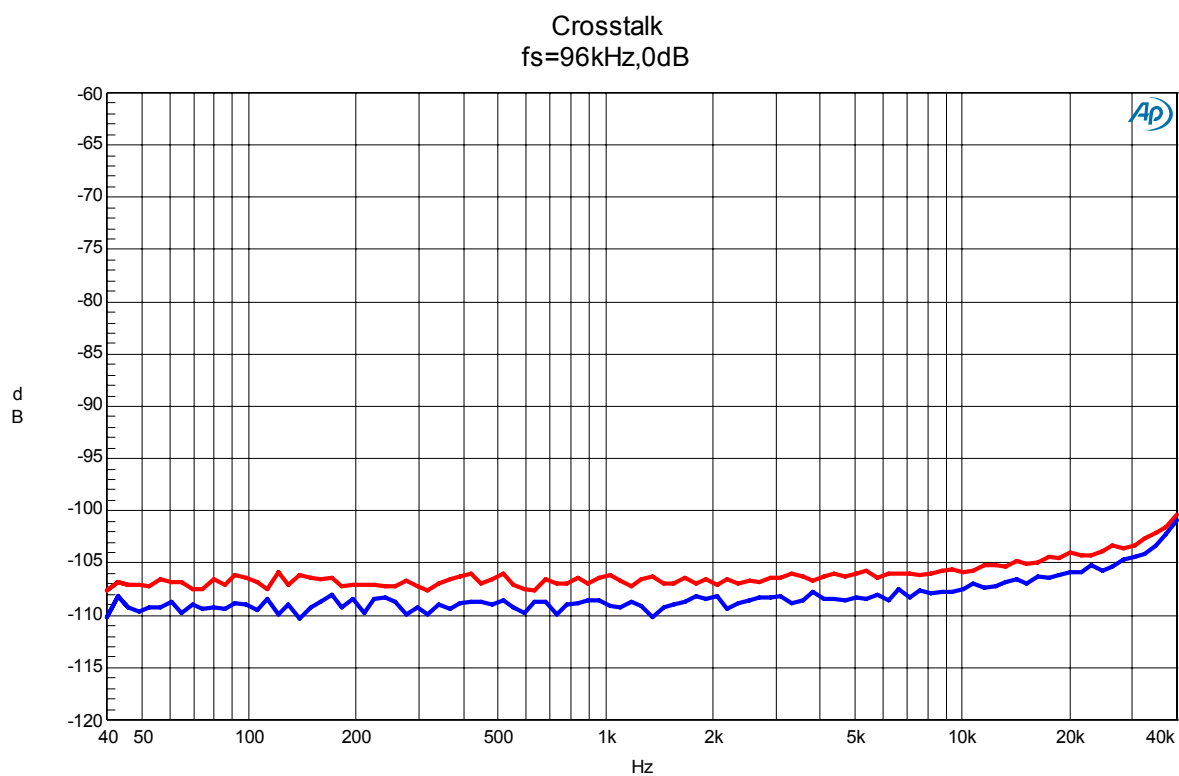
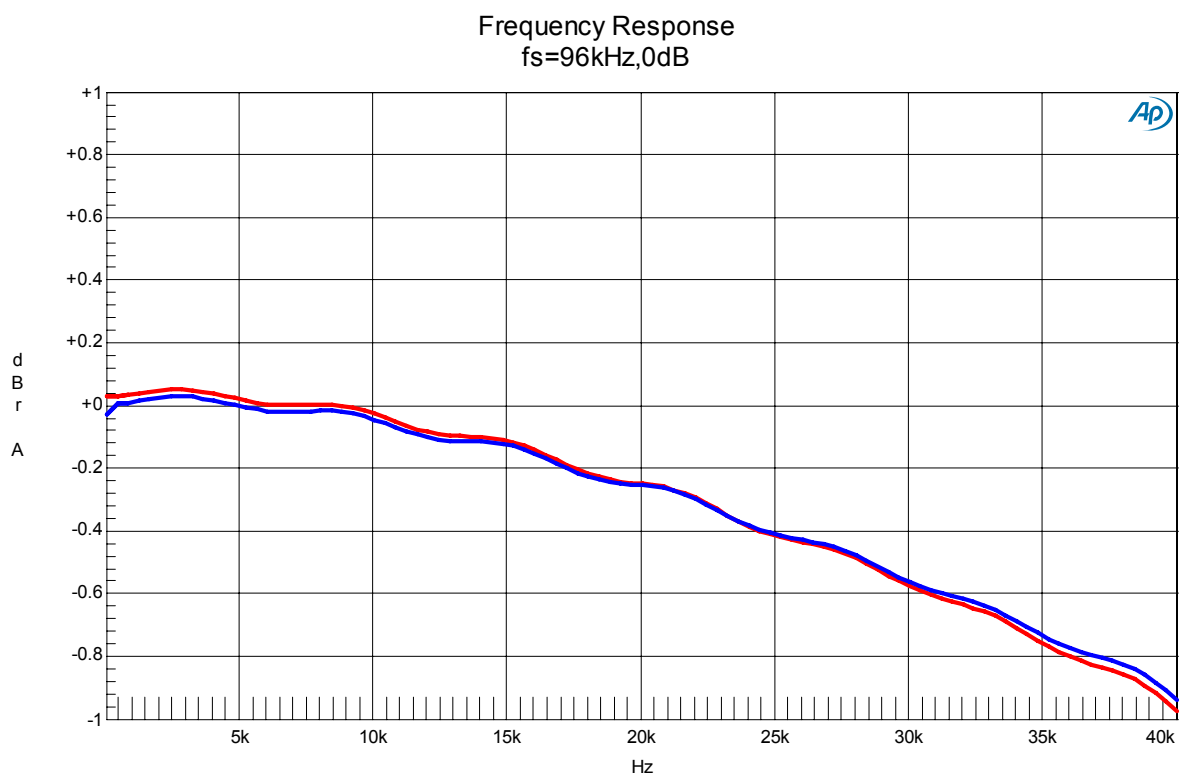


Figure 17. THD+N vs Input Frequency

**Figure 18. Crosstalk****Figure 19. Frequency Response**

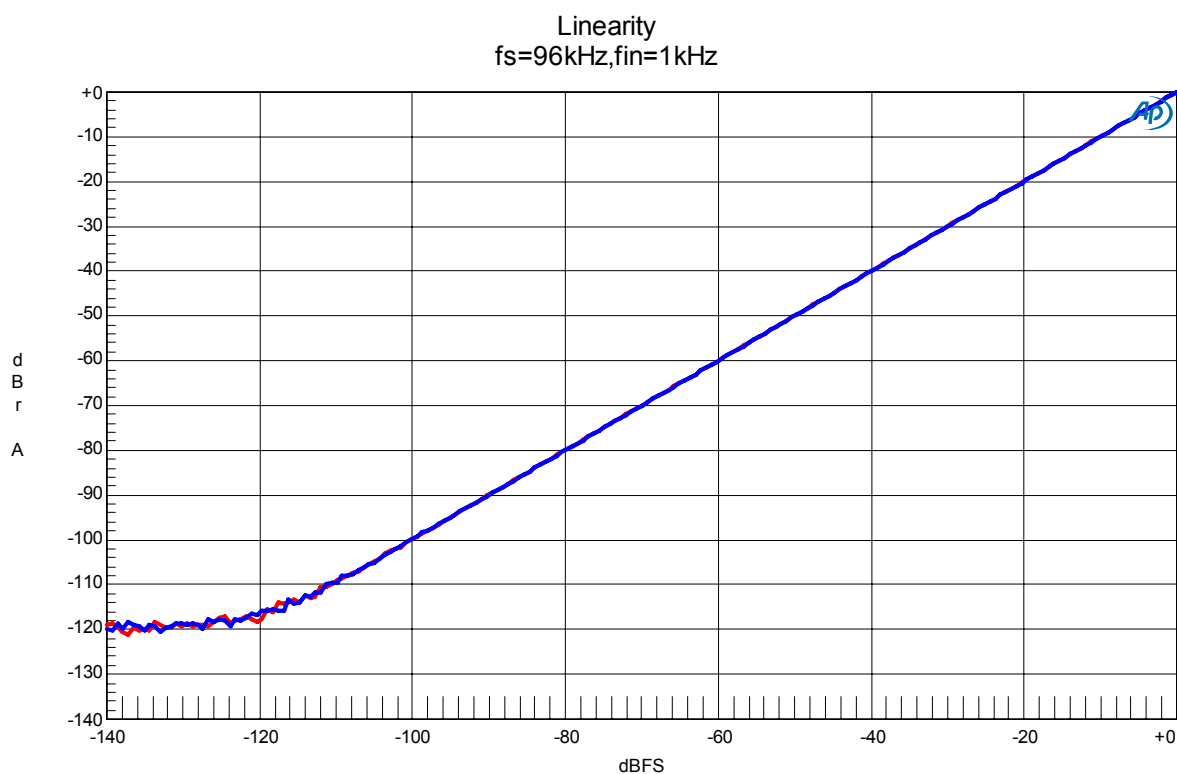


Figure 20. Linearity

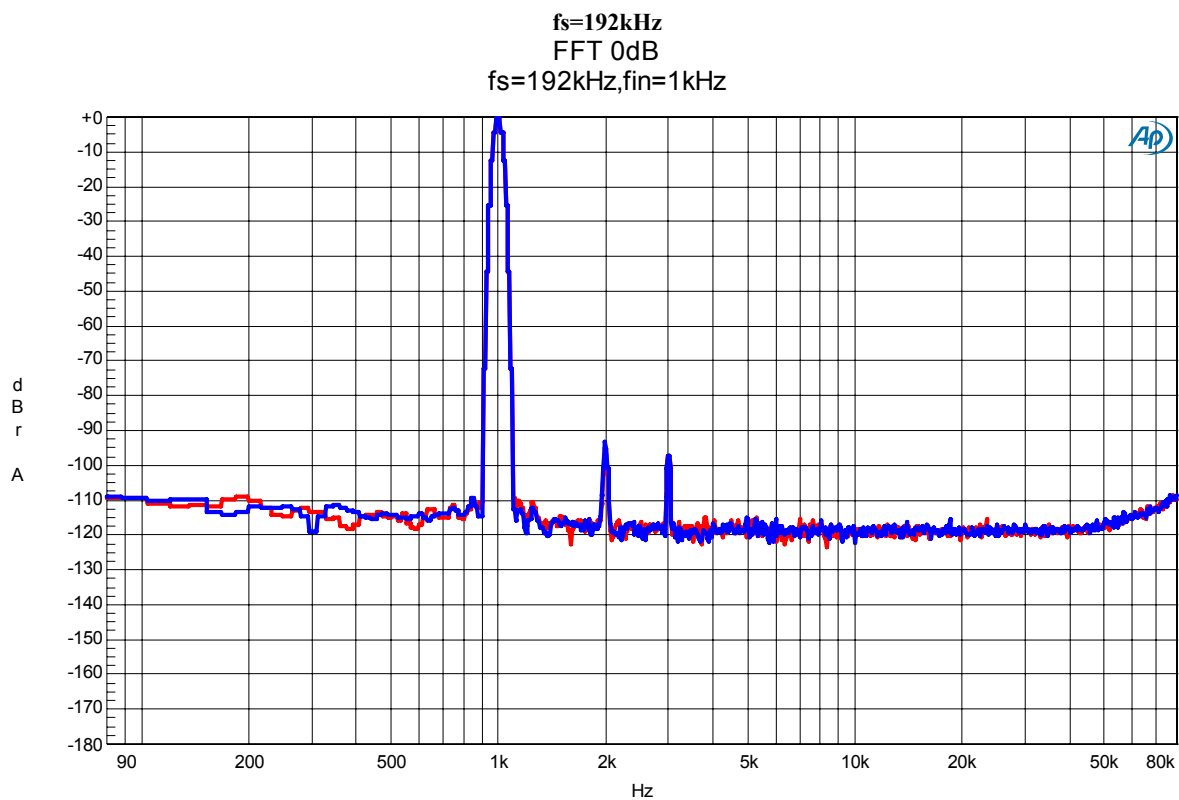


Figure 21.FFT(0dB)

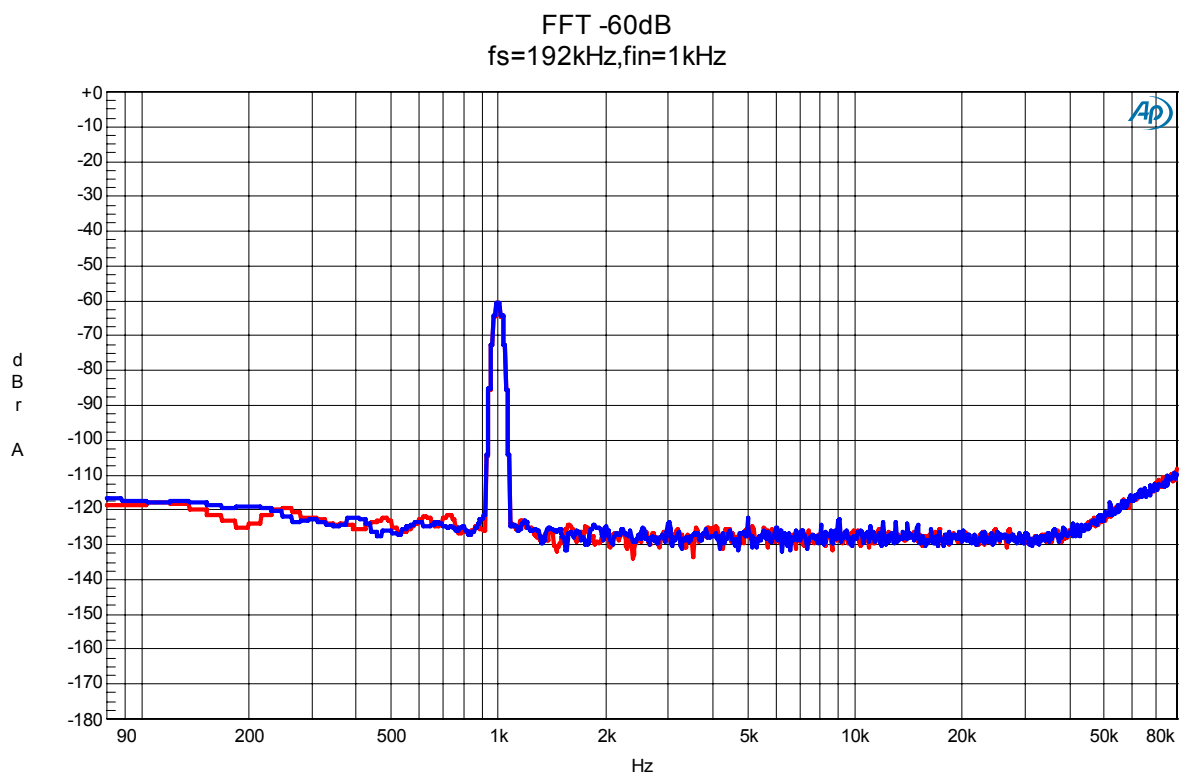


Figure 22.FFT(-60dB)

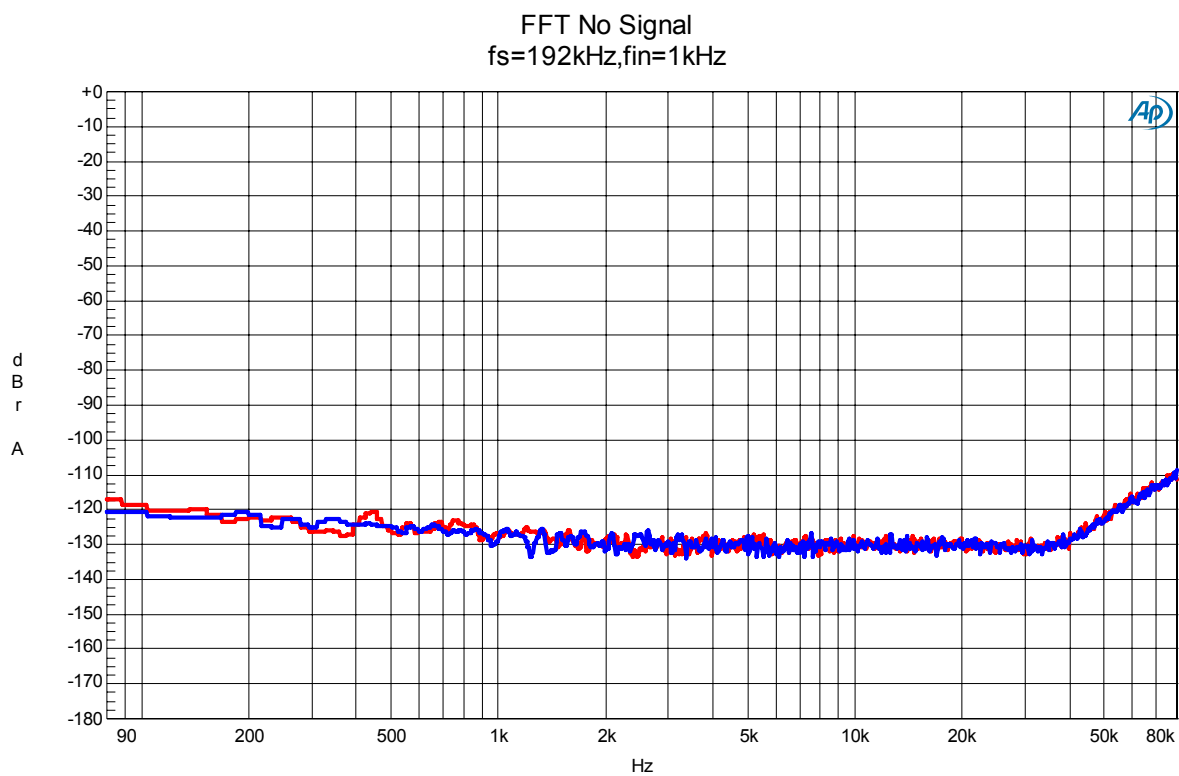


Figure 23.FFT(No Signal)

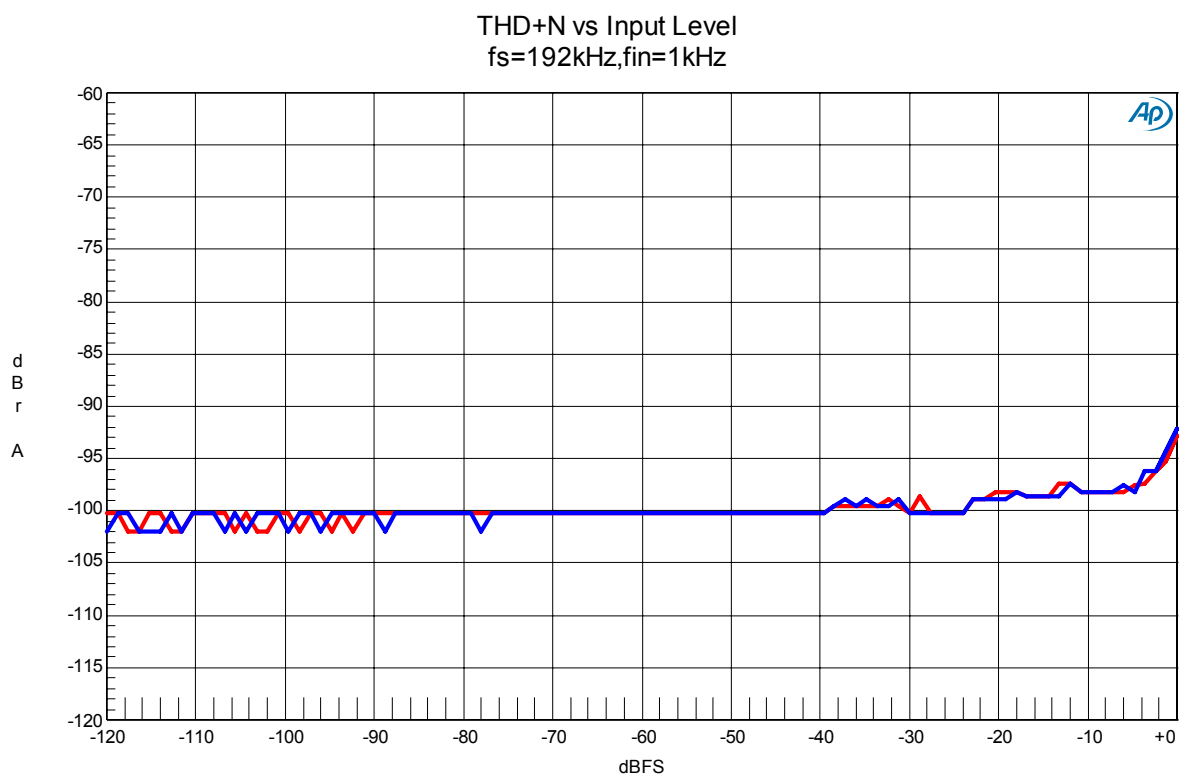


Figure 24. THD+N vs Input Level

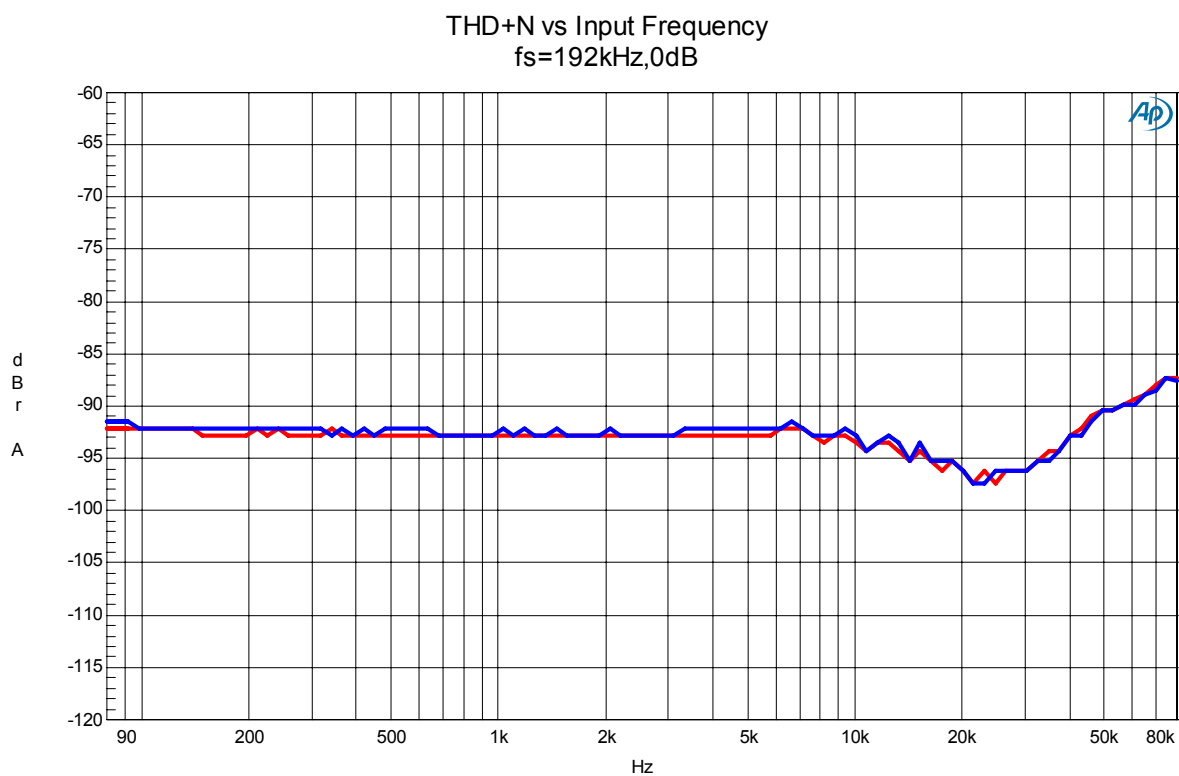


Figure 25. THD+N vs Input Frequency

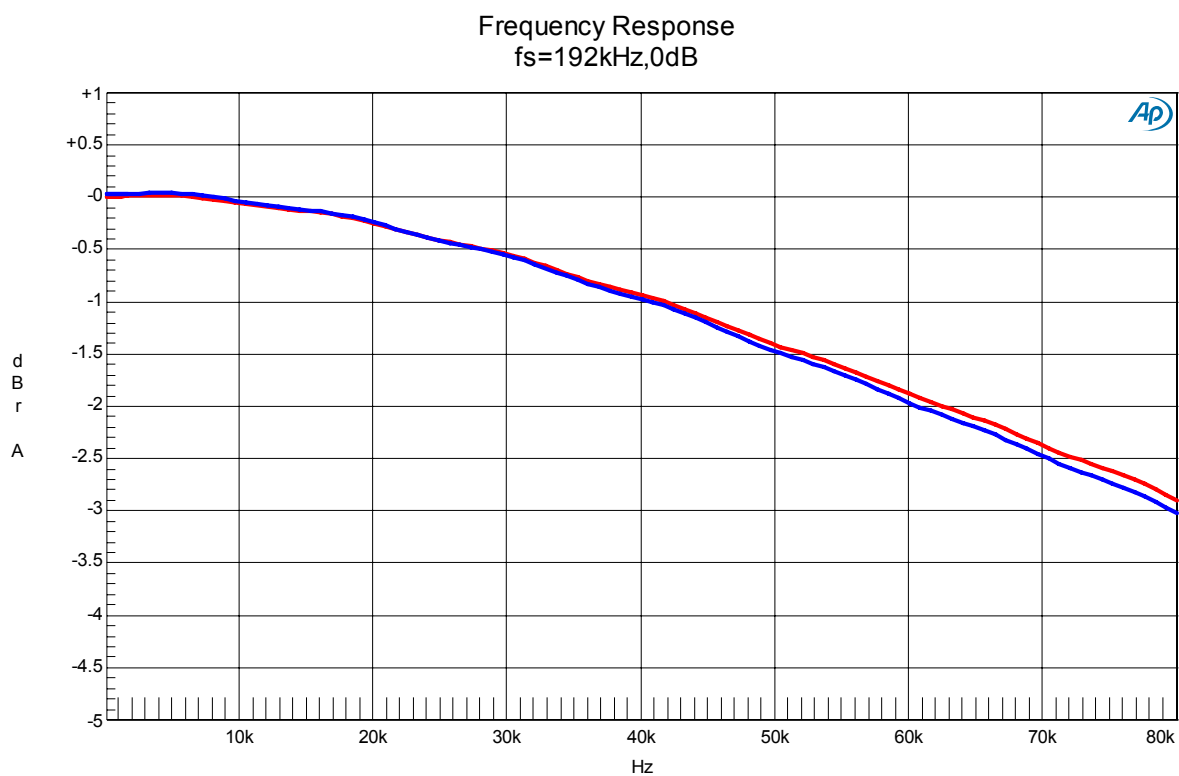


Figure 26. Frequency Response

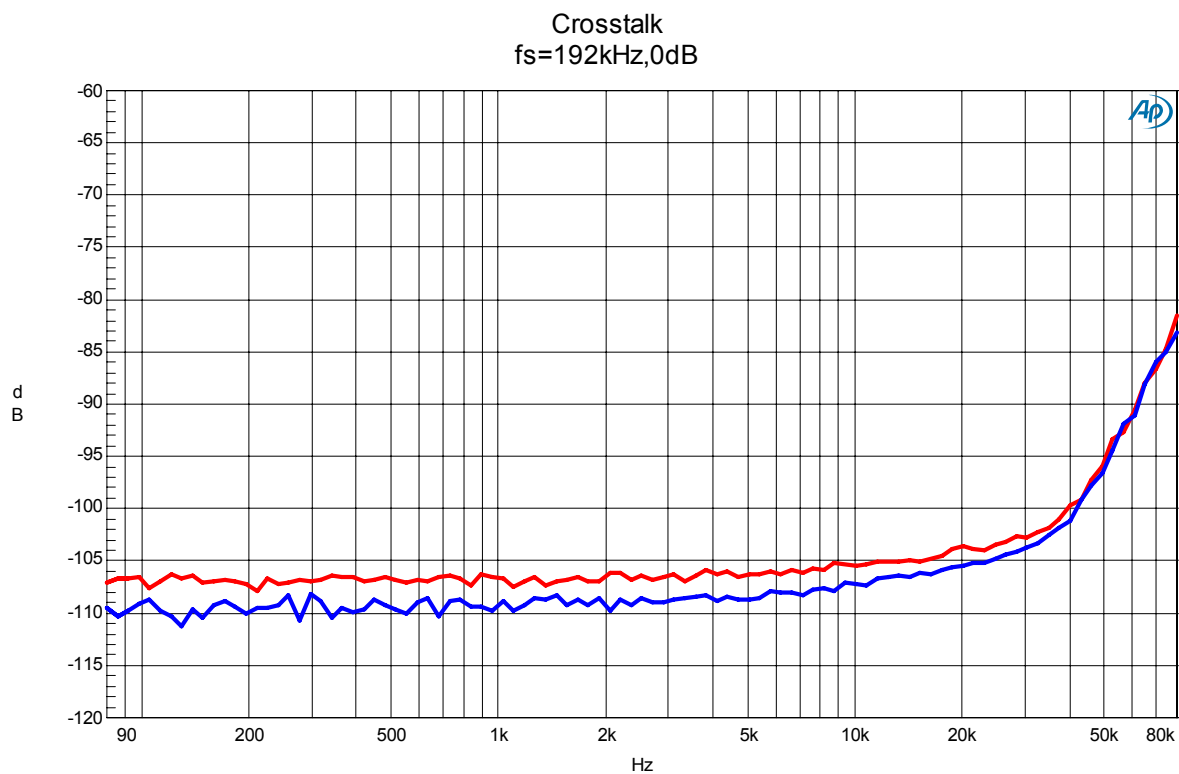


Figure 27. Crosstalk



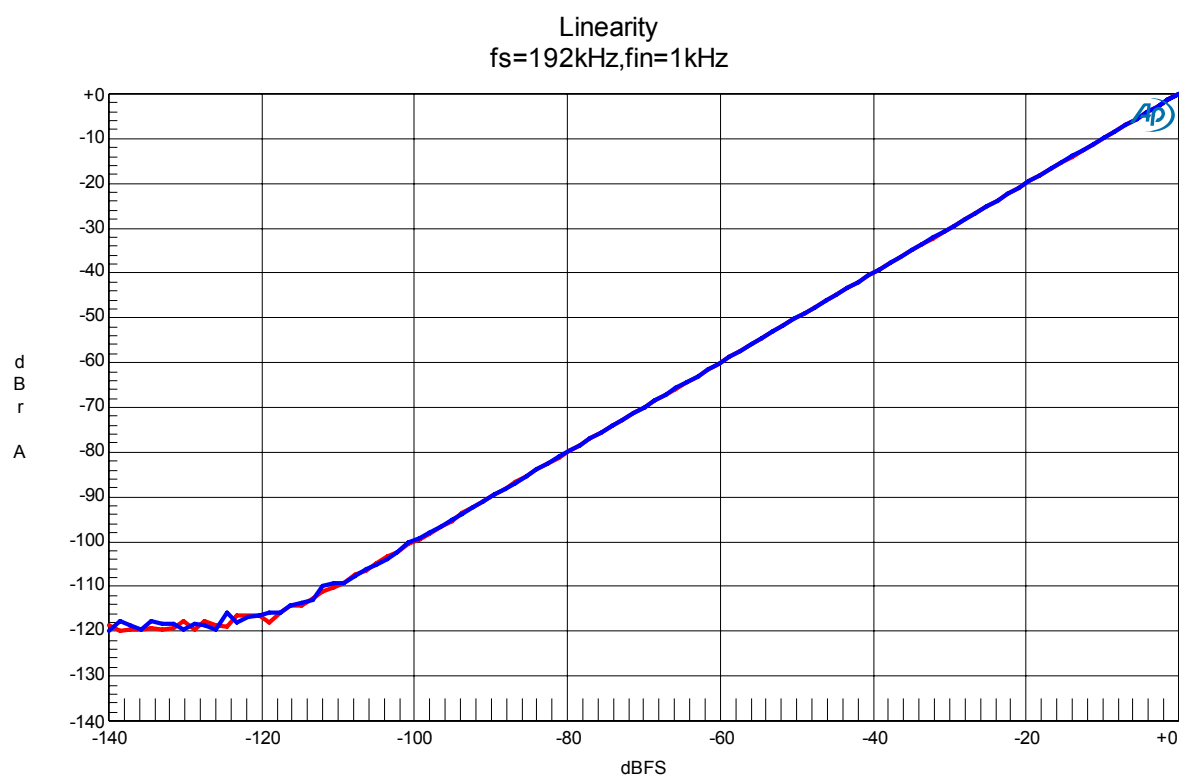


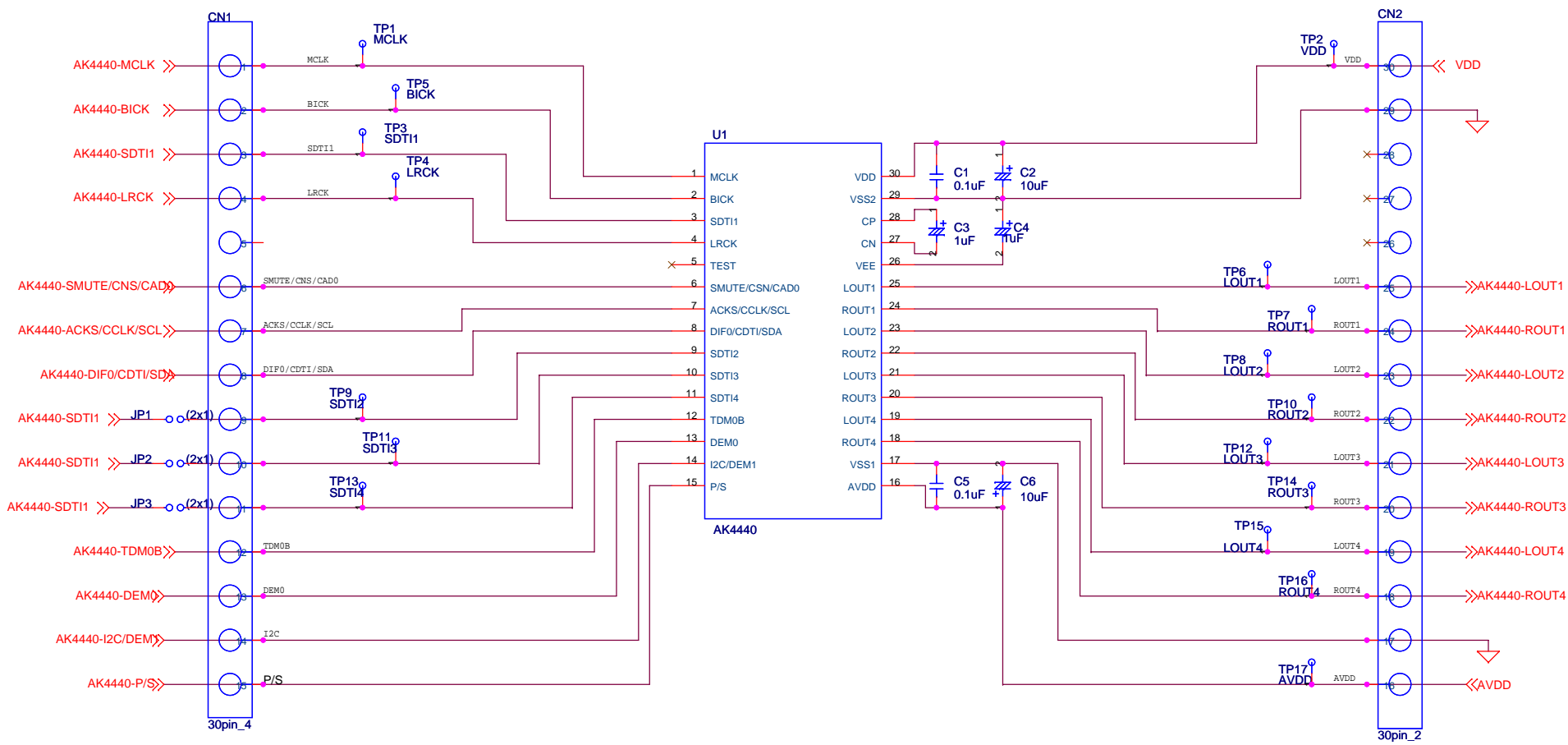
Figure 28. Linearity

## Revision History

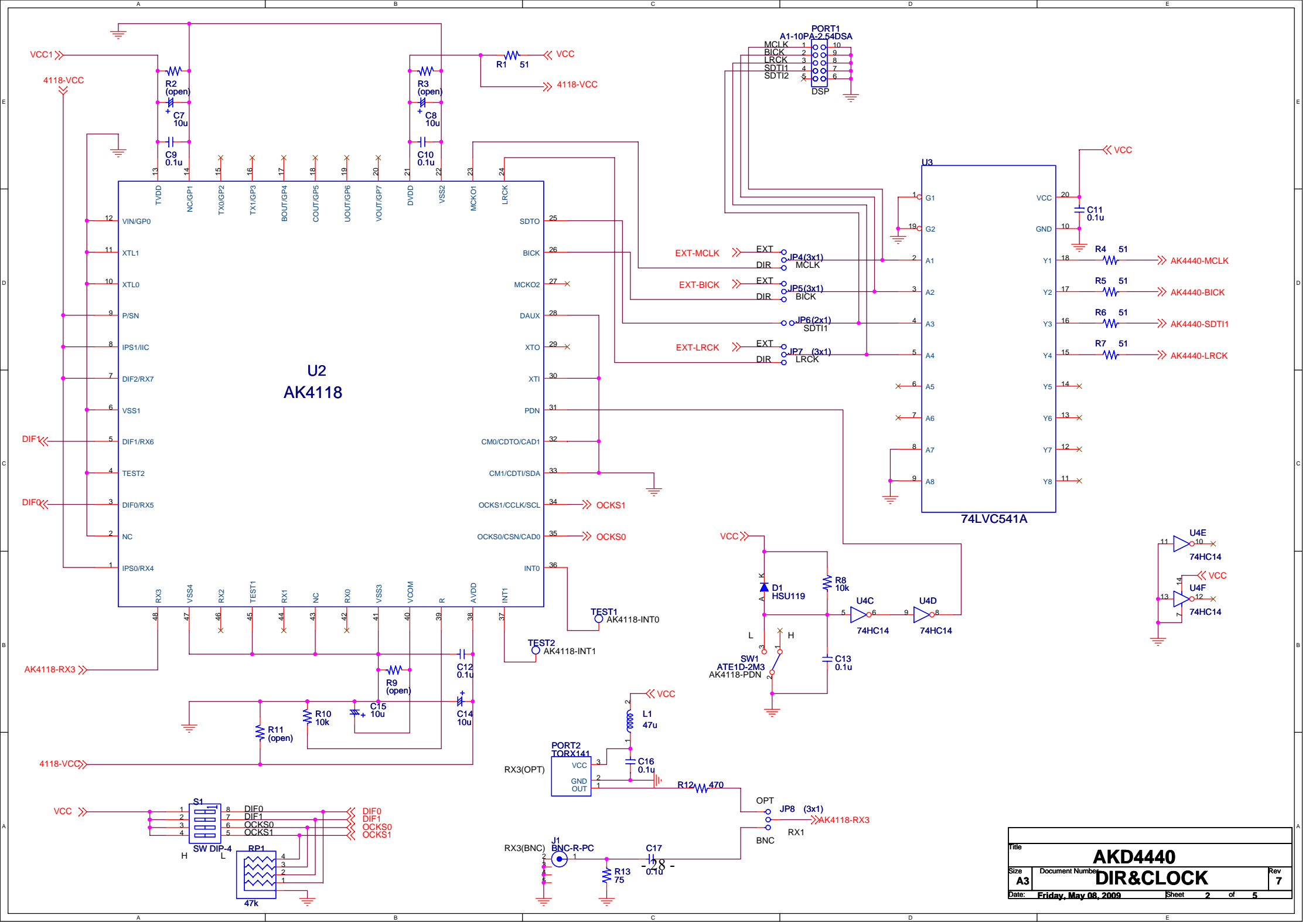
Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
08/11/13	KM097200	0	First Edition		
08/12/01	KM097201	0	Correction	5	AK4118 Setting Change:  Table 3. Audio Data Format of AK4118=> Table 2. Audio Data Format of AK4118, (24bit, I <sup>2</sup> S=>24bit, Left justified)  Selection of AK4114 Master Clock Output frequency (Refer Table 4.) => Selection of AK4118 Master Clock Output frequency (Refer Table 3.)
				16	Addition of circuit chart around AK4440
08/12/03	KM097201	0	Correction	6	Change in Control Soft Manual
09/01/13	KM097202	1	Correction	5	Change in Analog output
09/04/07	KM097203	2	Correction	1	Board Revision: Rev.1 → Rev.2
				12~17	Device Revision Change: Rev.A→Rev.B The addition of Table Data and plot data
09/05/08	KM097204	3	Correction	6,8	Change in Control Soft Manual
				22	Circuit Change : PORT3
09/08/26	KM097205	3	Modification	12~25	Update of measurement results and Plots. (fs=44.1kHz,fs=96kHz,fs=192kHz)

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 Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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Title			
AKD4440			
Size	Document Number		Rev
A3	AK4440		7
Date:	Friday, May 08, 2009		Sheet 1 of 5



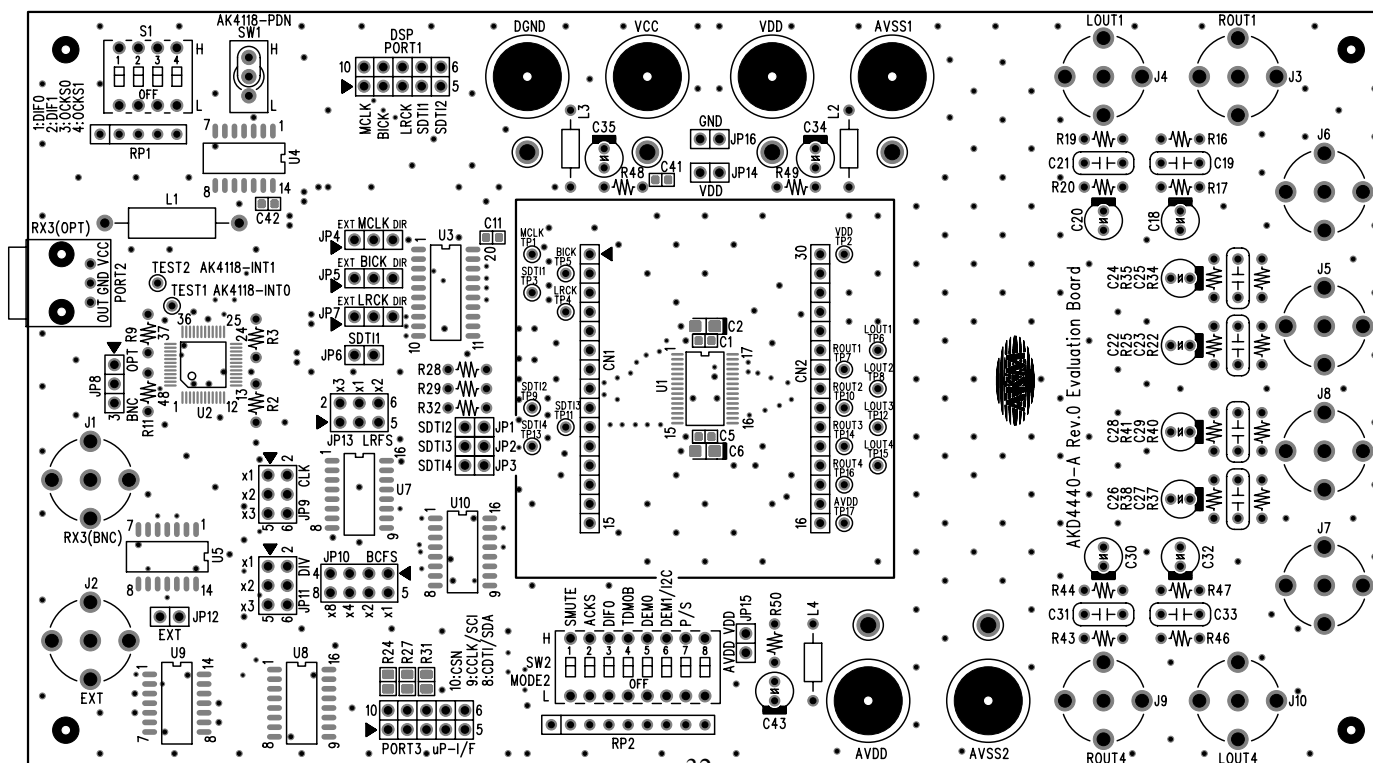
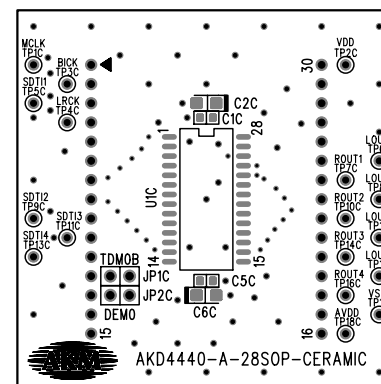
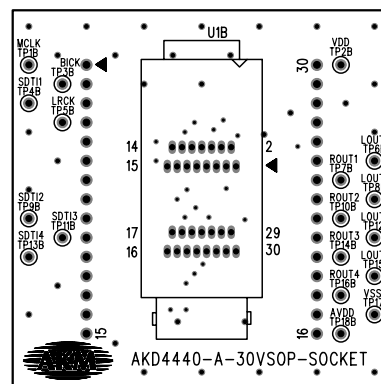
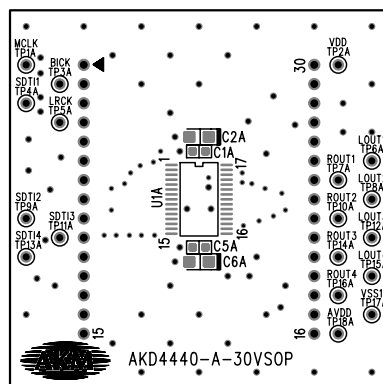






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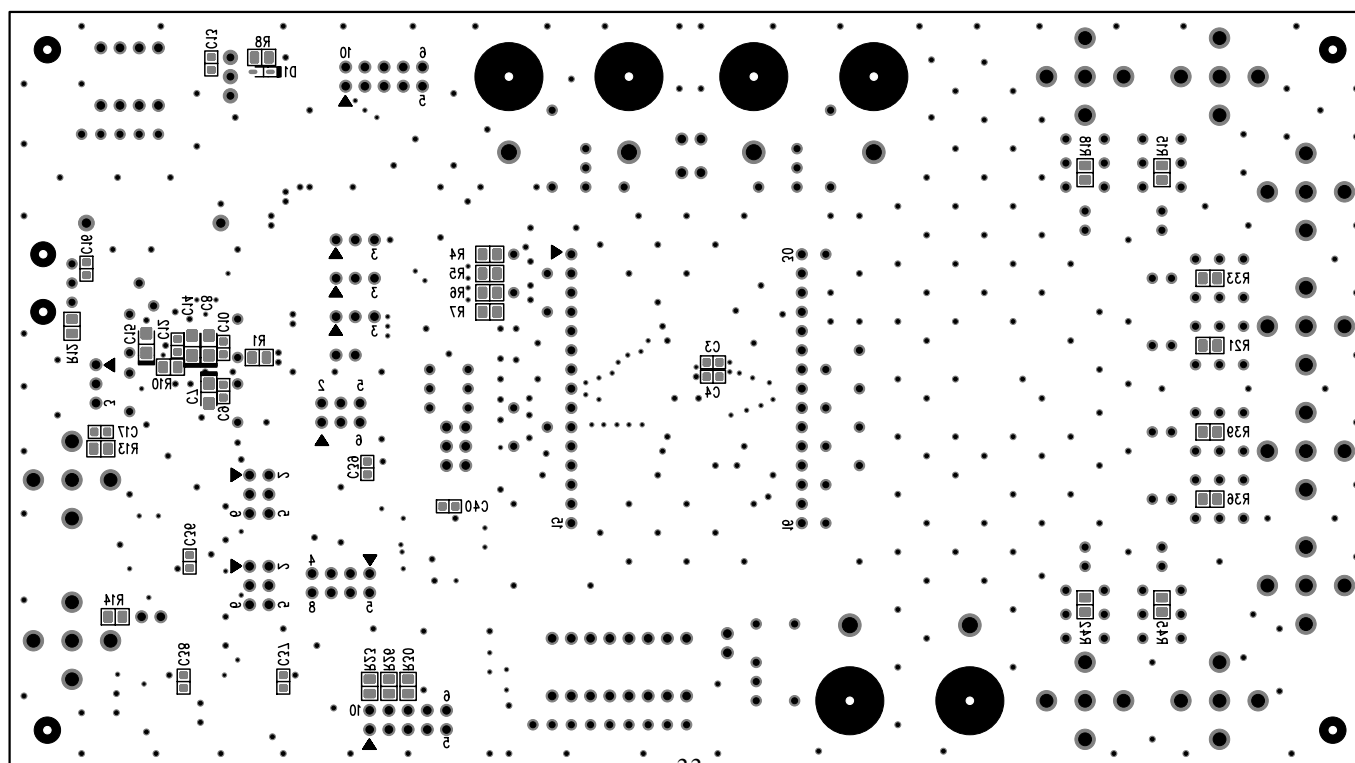
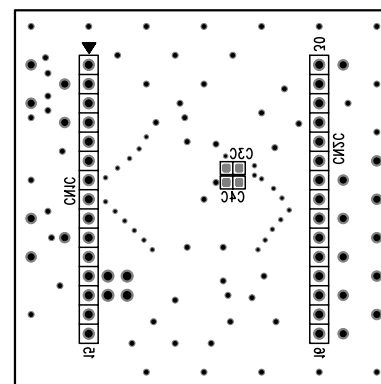
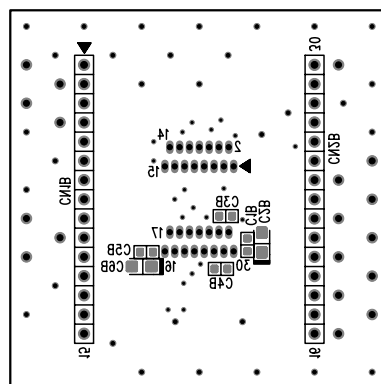
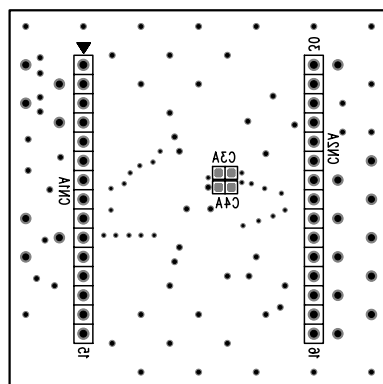
## 部品面シルク図





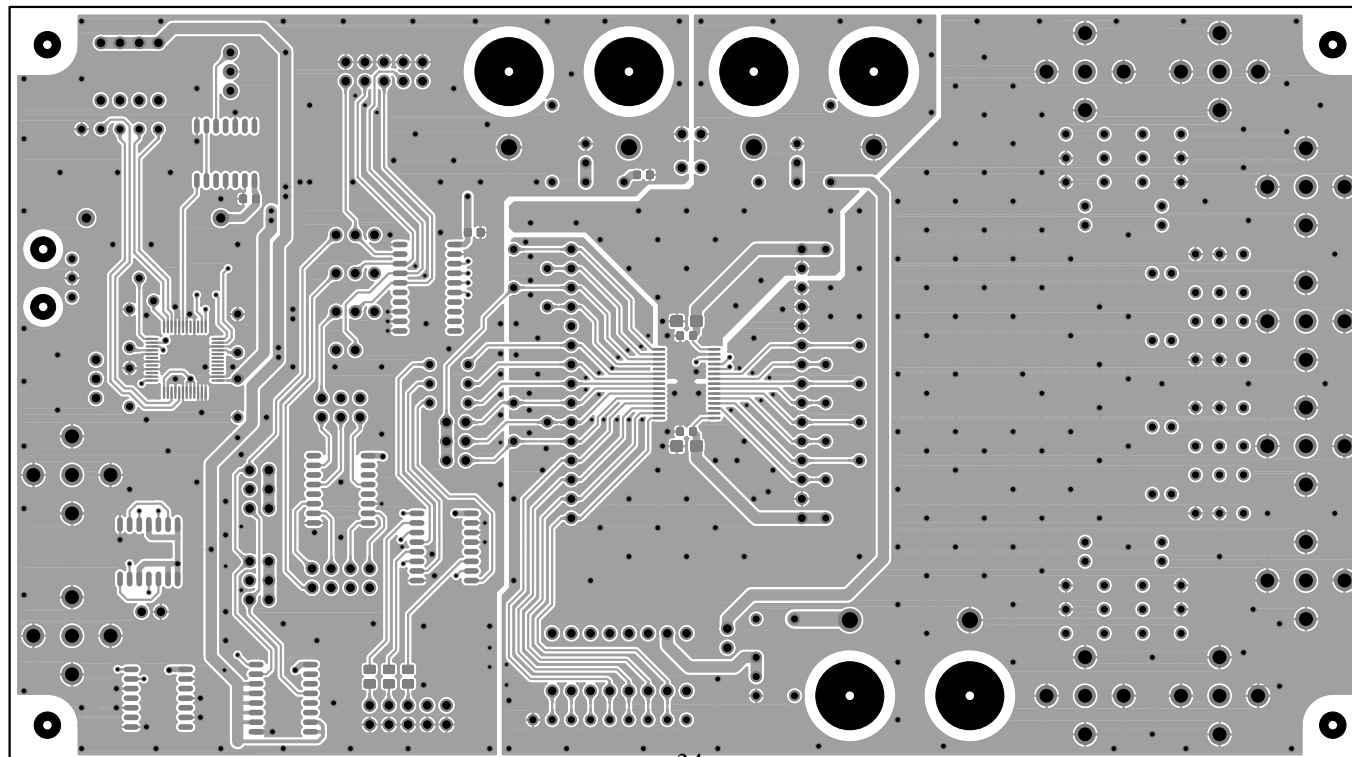
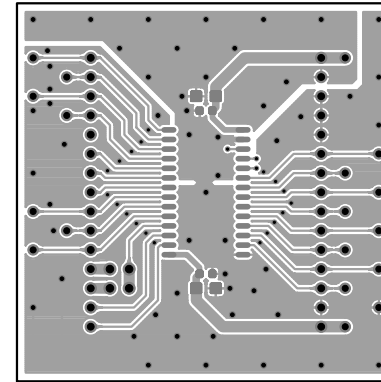
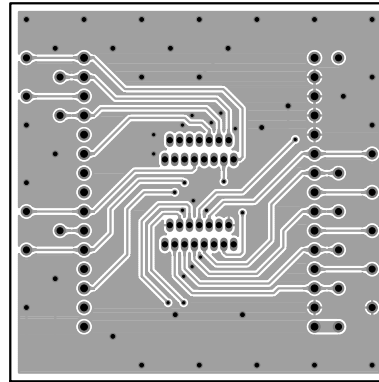
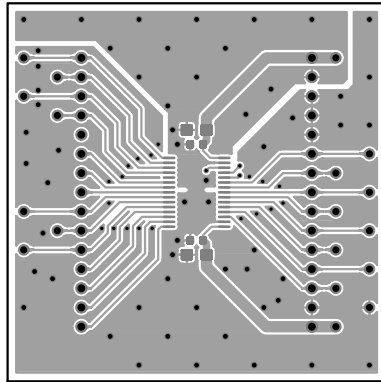
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## 半田面シルク図



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部品面パターン図



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半田面パターン図

