REDUCTION OF POWER STAGE THD BY ADDING OUTPUT CAPACITANCE

Gaël Pillonnet[12], Nacer Abouchi[1], Philippe Marguery[2]

[1]*CPE Lyon-AEME LPM UMR CNRS 5551, Lyon, France*

[2]*ST Microelectronics, Grenoble, France*

Correspondence should be addressed to Gaël Pillonnet (gael.pillonnet@st.com)

ABSTRACT

Audio class D converter has nonlinear distortion provided by power stage. In fact, the PWM inverter is influenced by the switching dead time introduced by power output control system. If output capacitance is added, the audio quality is improved. In this paper, the interaction between the dead time effect and the output stage capacitance is investigated. At first, each effect is investigated separately. Then, the sum of the effects is analysed to predict the improvement of audio quality. Finally, the calculated results are compared with low level simulation in order to confirm the validity of the analysis.

1. INTRODUCTION

The pulsewith-modulated (PWM) H-bridge inverter is widely used in various industrial applications such as audio digital analog converter. Despite a good PWM digital modulator, power stage introduces deviation errors due to the nonideal switching devices.

For avoiding the cross conduction between the upper and the lower transitors, it is essantial to insert a time delay in the control signal. This delay guarantees a safe operation, but it affects the audio performance of the inverter. Its detrimental effect may become significant when it operates in high switching frequency.

Recently, fast switching devices require a small dead time to avoid the cross conduction. Design of new audio converters underlines the no negligible effect of output capacitances on distortion level. Therefore, with the decrease of dead time, the charge and the discharge of output capacitances have a no negligible effect on the behaviour of power output voltage. It is shown that distortion level is strongly dependent on capacitances value.

In this paper, parasitic capacitance effect of the power stage is analysed to underline its opposite effect with dead time. Output capacitances are added to output power stage to compensate dead time effect and decrease distortion.

The subject of this paper is the quantitative prediction of dead time and output capacitances effects. It permit to underline the inter compensation between these effects. Calculated results are compared with low level simulation in order to confirm the validity of this analysis.

Moreover, audio quality caracterizations in transitor level simulation take many time because it requires a large transient analysis to process fourier transform. A high level modelization could help to decrease design time. Futhermore, the understanding of these effects is important to improve the performance of PWM inverters.

2. ANALYSIS OF THE DISTORTION

The output voltage of PWM power inverters shows harmonic distortion due to several causes. The main ones are the dead time and the output capacitances effects. The following part analyses these two effects. At first, the output voltage deviation is explained without output capacitances effect to identify clearly each effect.

2.1. Dead time effect

To evaluate the dead time effect, the capacitive effect of the switching elements is not considered.

Dead time are introduced at the beginning of each switching to delay the turning on until the other switch of the same leg turning off. Distortion due to dead time has been studied [2][3][4][5]. The following analysis sum up these pubications and generalise for our application. The dead time period causes the voltage deviation between the input ideal waveform and the output stage. It depends on the direction of the load current.

Fig. 2 shows Plus and Minus output power stage waveforms and the result in differential mode $V_r = V_{Plus} -$

V_{Minus}. V_i is the input and V_e is the deviation error. Effect of output capacitances is not considered in Fig. 1. The polarity of the output current is positive when the current flows into output. Each time, current in Plus and Minus stage are opposite ($i_m = -i_p$). Current in Plus stage are given as reference ($i = i_p$).

For example, a positive current introduces negative error on output voltage resulting in diodes D_{pl} and D_{mh}(Fig 5) conducting during the dead time. For a negative current, D_{ph} and D_{ml} conduct. In this case, the error is positive.

When the swithing is positive ($T = 1$), the positive edge is delayed in Plus stage because current i_p is positive. In opposite, output voltage in Minus stage keeps input shape. When switching is negative ($T = 0$), the output voltage in Plus stage follows the input but voltage in Minus stage is delayed by the dead time. Finally, this lag time causes output voltage deviation.

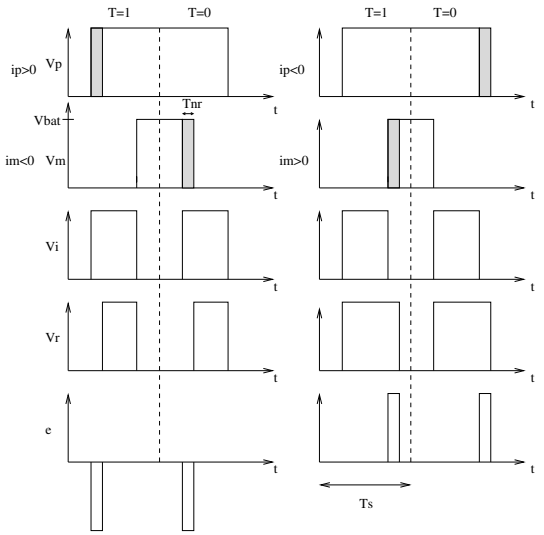

Fig. 1: Error due to dead time

The blanking time delay causes an error which is correlated with output current. Deviation voltage is negative when current i is positive and oppositly. The time delay can be evaluated by averaging voltage deviation over each positive and negative half cycle of the current with the switching cycle with period t_s:

$$V_e = \begin{cases} -V_{bat}\frac{t_{nr}}{t_s} & (i > 0) \\ V_{bat}\frac{t_{nr}}{t_s} & (i < 0) \end{cases} \quad (1)$$

where V_{bat} is supply voltage of power stage and t_{nr} dead time.

In conclusion, with a pure sinusoidal current, this effect introduces a square error on output voltage, resulting in odd harmonic distortion. Fig.2 is an other representation of deviation voltage due to dead time.

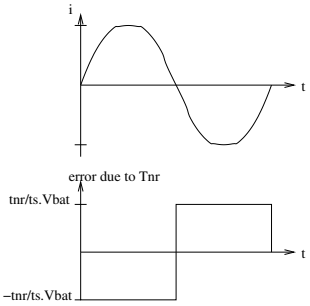

Fig. 2: Square error due to dead time

The error fourier transform shows the effect of dead time on output spectrum. Square error introduces odd-order harmonics on output spectrum. The magnitudes of harmonic can be expressed as :

$$A_d(m) = V_{bat}\frac{t_{nr}}{t_s}\frac{sin(m\frac{\pi}{2})}{m\frac{\pi}{2}} \quad (2)$$

In this equation, m is the order of odd harmonic, t_{nr} dead time, t_s sampling period and V_{bat} supply voltage.

The Total harmonic Distortion (THD) is defined as :

$$THD(M,\alpha) = \frac{\sqrt{\sum_{i=2}^{N_{max}}(V_{bat}\alpha\frac{sin(i\frac{\pi}{2})}{i\frac{\pi}{2}})^2}}{M - \frac{2V_{bat}\alpha}{\pi}} \quad (3)$$

where, $\alpha = \frac{t_{nr}}{t_s}$ and M the modulation index ($\frac{V_{in}}{V_{out}}$).

Dead time introduces odd harmonic, which is dependant on dead time to sampling period factor ratio and supply voltage.

Unfortunately, this equation can not be predicted THD accurancy when dead time is close to few nanoseconds. Moreover, this effect cannot be explained by the improvement of audio quality when capacitances are added in output power stage.

2.2. Effect of output capacitances

In this part, effect of output capacitances is explained. Although a similar approach is taken in [1], analytical

expression is added to underline the opposite effect to dead time. Morevover, PWM inverter with capacitors in parallel on each transistor is used to reduce switching loose and noise in [6]. But, these publications does not include the effects in audio band.

The output capacitances error has a affect on pulse amplitude. The ouput rise and fall times depend on the direction and the magnitude of output current. Indeed, switching elements have an equivalent capacitance. Output capacitance is composed of parasitic MOS capacitance and additional output capacitance (Fig.5).

For example, Fig. 3 shows the voltage deviation of output when current is positive. Three cases are shown in Fig.4 and are explained in the following.

case 1 : When current is high or/and output capacitances are low, the capacitances are discharged immediately. The capacitances have no effect on deviation of output voltage.

case 2 : In the case that the discharge time is lower than dead time, the output capacitances can be discharged completly before the end of dead time. After the discharge, the lower body diode conduct.

case 3 : The third case is produced when current is low or capacitances have a large value. The discharge time is higher than dead time. The output capacitances have no time to discharge competly before the turn on of the lower transistor.

In discharge region, the output voltage is as the following:

$$V_{out}(t) = V_{bat} - \frac{1}{C}\int_{t_0}^{t} i_{out}\,dt \qquad (4)$$

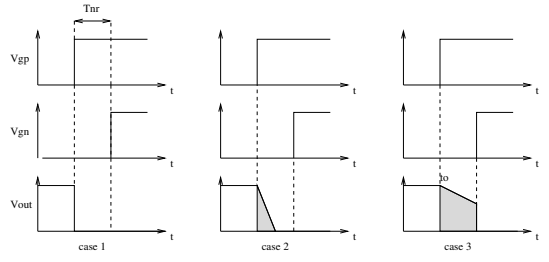

Fig. 3: Output Voltage deviation

In conclusion, effect of capacitances introduces a gain voltage error during the discharge of the output capacitances. This error can be expressed by :

$$V_e = \begin{cases} sign(i)V_{bat}\frac{t_c}{2t_s} & (t_c < t_{nr}) \\ sign(i)(V_{bat} - \frac{V_f}{2})\frac{t_{nr}}{t_s} & (t_c > t_{nr}) \end{cases} \qquad (5)$$

where $tc = C\frac{V_{bat}}{i_t}$, $V_f = t_{nr}\frac{i_t}{V_{bat}}$, $C = C_h + C_l + C_p$ and C_p value of output parasitic capacitances.

In this equation, t_c is the charge or discharge time of the output capacitances, i_t switching output current and $sign(i)$ the current direction.

Fig. 5 shows voltage deviation during a current period for different values of capacitances ($C_1 > C_2 > C_3$). Indeed, the error shape depends on current or capacitances values. In this example, C_1 converges towards infinity.

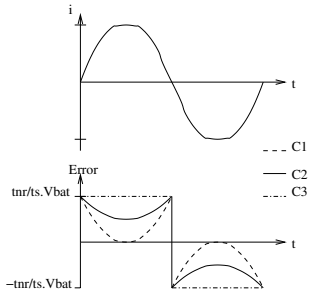

Fig. 4: Voltage deviation

3. IMPLEMENTATION OF THE TECHNIQUE

3.1. Proposed scheme

The circuit of D class amplifier is shown in fig.5. The PWM inverter is composed of two power MOS and two output capacitances C_H and C_L. The load is connected to the full bridge by a low pass filter. The double side sawtooth is used for PWM modulation. Overlap time control is designed to avoid the power stage cross conduction.

3.2. Compensation effect

In the previous section, two effects are described separatly. This part explains the intercompensation of these effects. PWM inverter has four switching states where these two effects appear (Tab. 1).

These effects are produced alternatively for each system states. Fig.6 shows the deviation voltage for each states

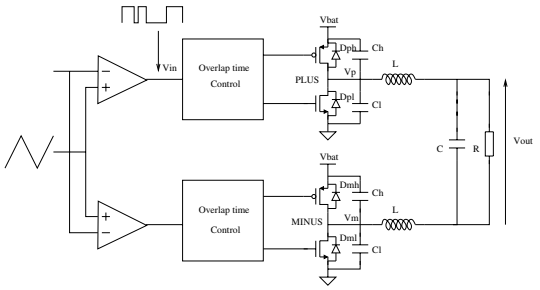

Fig. 5: Full bridge power stage

T	$i > 0$	$i < 0$
0	t_{nr}	capa
1	capa	t_{nr}

Table 1: Condition of dead time (t_{nr}) and output capacitances (capa) effects

in transient (case 3). V_i is the ideal voltage, V_r the power output voltage, V_e the voltage error. Error is expressed as $V_r = V_i + V_e$.

Fig.7 shows clearly the compensation between dead time and output capacitances effect. Fig. 7 shows the error of these effect where capacitances values vary ($C_1 < C_2 < C_3$).

The error function becomes more sinusoidal when output capacitance increases.

If $t_c > t_{nr}$ is true all time then the deviation error can be expressed as :

$$V_e = \begin{cases} -V_{bat}\frac{tnr}{ts} + (V_{bat} - \frac{i_t t_{nr}}{2V_{bat}})\frac{t_{nr}}{t_s} & (i > 0) \\ V_{bat}\frac{tnr}{ts} - (V_{bat} - \frac{i_t t_{nr}}{2V_{bat}})\frac{t_{nr}}{t_s} & (i < 0) \end{cases} \quad (6)$$

The first part shows the effect of dead time (1) and the second term represents the error due to output capacitance (5).

(6) can also be written as :

$$V_e = \begin{cases} -\frac{t_{nr}^2}{2V_{bat}t_s} i_t & (i > 0) \\ +\frac{t_{nr}^2}{2V_{bat}t_s} i_t & (i < 0) \end{cases} \quad (7)$$

It should be noted that V_e is only affected by i_t. The equation remaining is constant. The voltage error is pure

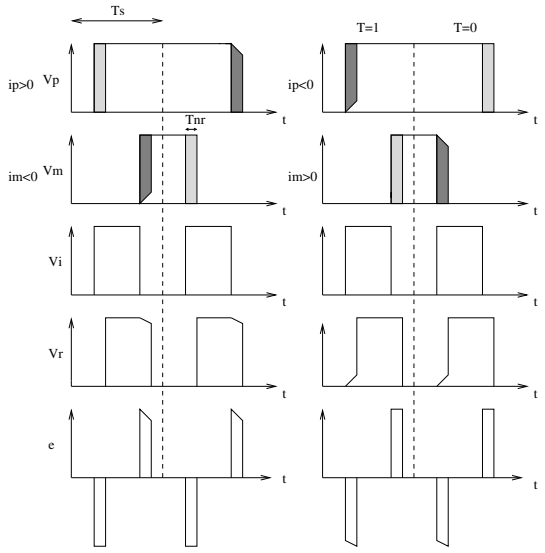

Fig. 6: Output Voltage deviation for two effects

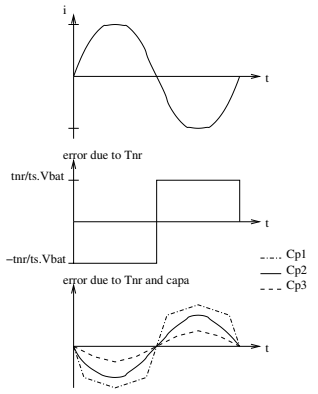

Fig. 7: Error voltage

sinusoidal. Therefore, it does not create distortion on output signal.

To be in this region, C must be large or output current must be low. In industrial applications, low power audio inverter can be in these conditions.

4. RESULTS AND DISCUSSION

In this part, the modelisation of two effects is investigated in an example and compared to transitor level simulation. Eldo is used to simulate the audio performance in the system. High level model is generated by MATLAB.

The power stage design is explained below. Fig.5 represents the general schematic. The PWM modulator is applied to a full-bridge transitor inverter that supplies an inductive load ($20uH$). Total output parasitic capacitances represents $50pF$.

The inverters operates on sinusoidal PWM, and the carrier frequency is $960kHz$. The output resistor is equal to 32Ω. Voltage supply is fixed at $2.5V$. Then, the current max is $62mA$ at $-2dBFS$.

The input of power stage is provided by digital circuit to generate PWM modulation. This circuit is not completly linear and create odd-order harmonic at $-2dbFS$ ($THD = 97dB$).

To generalize and to compare with analytical expressions, we do not use symetrical overlapp control. Non overlapp control delays the voltage gate control with two differents times. When the transition is high (T=1), the delay is equal to $6.6ns$. In other hand, when transition is low, $11ns$ is the delay between the command of PMOS and NMOS.

Fig.8 compares results of eldo simulations vs models of two effects. The solid line shows the eldo reference. Other ones are obtained by MATLAB simulations. The dashed line is the model results without current variation. Indeed, output current vary between Plus and Minus stage switching. Current switching variation depends on inductive load value. The dash-dot line is the model with oscillation current. Fig.7 shows clearly that output capacitances inhibit distortion.

It can be seen that there is a generally good agreement between calculations and predictions when output capacitances are low. It should be noted that output capacitances have a strong effect on distortion level.

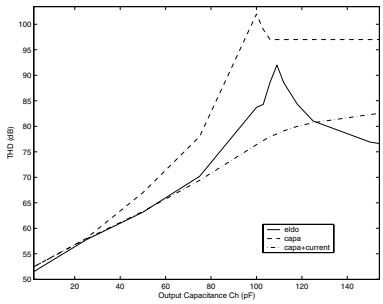

Fig. 8: Distortion vs output capacitances

When oscillation current is introduced, the increase of audio quality is very close to eldo simulation for small value of capacitances. Current oscillations decrease capacitances effect because capacitances effect appears when current is the lower. In opposite, the dead time effect appear when switching current is the higher. As the capacitances effect depends on current, its effect and nonlinear compensation decreases.

However, eldo model predicts a distortion decrease after a capacitances value. It can be explained by turn on transitor time is increasing with capacitances value. This effect introduces nonlinear distortion. The MATLAB model does not care of this turn on delay. Therefore, model predicts constant improvement of distortion until clamping on output digital distortion.

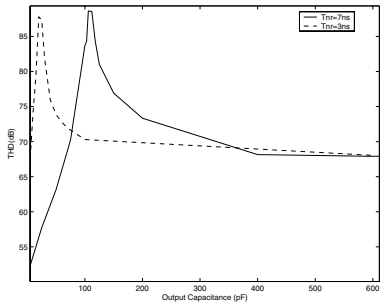

Fig. 9: Distortion vs output capacitance and dead time

Fig.9 shows the variation of audio performance due to dead time. These results are obtained by eldo. At $t_{nr} = 3ns$, the performance increases more rapidely. Moreover, the maximum is obtained when capacitances value is smaller than at $t_{nr} = 7ns$. In fact, it is easier to compensate the dead time effect when it decreases. In both

cases, large value of capacitances compensate distortion due to dead time effect and introduce the same non linearity. Audio performance does not depend on dead time for large capacitances value. This effect underlines the compensation effect between dead time and capacitance.

Finally, audio performances depend on input signal. Fig.10 shows variations between input signal at $2kHz$ and $7kHz$ when dead time is fixed at $7ns$. Eldo is used to obtain these results.

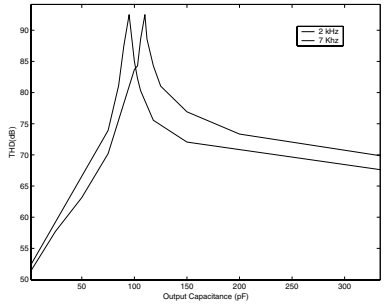

Fig. 10: Distortion vs output capacitance and input frequency

5. CONCLUSION

In this paper, the mechanism that causes the inverter nonlinearities is described in details. Moreover, an analytical method is proposed to modelise the output capacitances effect. The validity of the method is confirmed by simulations using low level simulation. Futhermore, high level distortion analysis take 2000 time less than low level simulation.

Output capacitances introduce significant nonlinear distortion into the voltage that compensates dead time effect. The addition of dead time and output capacitances effects improve audio quality. To decrease nonlinear distortion, output capacitances have been added. Unfortunately, efficiency decreases with the size of output capacitor. But in the previous example, efficiency decrease into 2% for a $30dB$ distortion gain.

The principle discussed in this paper will be useful for any types of low power applications which require good audio quality. Capacitances are simple and easy to implement. Moreover, impact on system area depends on process. If MIM capacitor is used, the size of capacitor has a little impact on system area. Finally, analytical models can improve design time because it can be used for a first approach.

Conventional PWM inveters generates a large amount of electromanegnic (EMI). [6] underline the improvement of switching noise. Also, since the switch-voltage waveforms are trapezoidal in improved class-D inverters. They contain a smaller amount of harmonics than the square waves encountered in the conventional class-D inverters. Consequently, the EMI and the noise level are inherently reduced.

6. REFERENCES

[1] K. Yamamoto, K. Shinohara, H. Ohga, Effect of Parasitic Capacitance of Power Device on Output Voltage Deviation during Switching Dead-Time in Voltage-Fed PWM Inverter, Power Conversion Conference - Nagaoka 1997., Proceedings of the , Volume: 2 , 3-6 Aug. 1997

[2] R.C. Dodson, P.D. Evans, H. Tabatabaei Yazdi, S.C. Harley, Compensating for dead time degradation of PWM inverter waveforms, IEE Proceedings B , Volume: 137 , Issue: 2 , March 1990

[3] K. Nielsen, PEDEC-a novel pulse referenced control method for high quality digital PWM switching power amplification, Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE , Volume: 1 , 17-22 May 1998

[4] Seung-Gi Jeong; Min-Ho Park, The analysis and compensation of dead-time effects in PWM inverters, Industrial Electronics, IEEE Transactions on , Volume: 38 , Issue: 2 , April 1991, Pages:108 - 114

[5] Wu, C.M.; Wing-Hong Lau; Shu-Hung Chung, H., Analytical technique for calculating the output harmonics of an H-bridge inverter with dead time, Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , Volume: 46 , Issue: 5 , May 1999, Pages:617 - 627

[6] Kazimierczuk M.K, Szaraniev W, Class-D zero-voltage-switching inverter with only one shunt capacitor, Electric Power Applications, IEE Proceedings B [see also IEE Proceedings-Electric Power Applications] , Volume: 139 , Issue: 5 , Sept. 1992, Pages:449 - 456