The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters and on Oversampling Delta Sigma ADCs

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Abstract

Sampling clock jitter is inevitable in a digital studio environment. This paper discusses the audio effects of clock jitter on an Analog-to-Digital Converter (ADC). The clock jitter sensitivity of a conventional Nyquist sampling ADC is compared and contrasted to that of a 3 MHz 64X oversampling delta sigma ADC.

0 INTRODUCTION

The increasing density of digital equipment in studios has prompted much discussion on synchronization of multiple items of digital audio equipment. The distribution of a master clock, for example via the AES/EBU interface, will inevitably add jitter to the clock. Each item of digital audio equipment that contains an analog-to-digital converter (ADC), or a digital-to-analog converter (DAC), will require a stable sampling clock, which is frequency locked to the distributed master clock. This paper investigates the amount and nature of jitter that an ADC can tolerate.

Included in the paper are a theoretical analysis of the effect of clock jitter on the sampling process, the results of a computer simulation, and measured results taken from actual ADC's with deliberately jittered clocks. Different types and amplitudes of jitter are investigated. In addition, the jitter sensitivity of a 76.8 kHz sampling ADC is compared and contrasted to that of a 3 MHz oversampling delta sigma ADC.

1 Clock Jitter Theory

The effects on ADC performance of jittering the sampling clock bear a strong resemblance to classical FM modulation. The input frequency is equivalent to the carrier frequency, and the clock jitter frequency (or spectrum) is equivalent to the modulation frequency. For simplicity of initial analysis, consider an ADC with a sine wave input signal, and a sampling clock time modulated (jittered) by a low frequency sine function. If a record of data is taken from the ADC and analyzed using Fourier analysis, then the effect of the clock jitter is to reduce the height of the input sine component, and to introduce sideband frequency components. The sideband frequencies are equally spaced either side of the input component, at a distance equal to multiples of the jitter frequency. The amplitude of the sidebands varies with the amount of clock jitter. However clock jitter is not precisely FM modulation; there are some important behavioural differences. The equation for sinusoidal sampling clock time jitter is:

$$v(t) = A \cos[\omega_i(t + J \sin \omega_j t)] \qquad (1)$$

where A is the ADC input signal amplitude, ω_i is the input signal frequency, J is the peak amplitude of the jitter, and ω_j is the jitter frequency. Notice that if ω_i is increased then the contribution of the jitter term also increases. This agrees with the intuitive reasoning that if the slew rate of the input signal increases, then the amplitude error caused by clock jitter will increase. Notice also that the units of J is time, in seconds.

Equation (1) may be re-written as:

$$v(t) = A \cos[\omega_i t + J\omega_i \sin \omega_j t)]$$

Substituting $\beta = J \omega_i$ gives:

$$v(t) = A \cos[\omega_i t + \beta \sin \omega_j t)] \qquad (2)$$

Equation (2) is the classical FM modulation equation, where β is the modulation index. Analysis of the height of sidebands in terms of β is well documented using Bessel functions [1], where $J_0(\beta)$ is the relative amplitude of the input frequency component, and $J_1(\beta)$ is the relative amplitude of the first pair of sidebands. Since we are only concerned with small amounts of clock jitter, and therefore small β, only the first pair of sidebands are significant.

As an example of using these formulae, let's set the input frequency to 10900 Hz, and the clock jitter peak amplitude to 1 ns. Therefore, since $\beta = J \omega_i$, $\beta = 6.848 \times 10^{-5}$ radians. Unfortunately, commonly available tables of Bessel functions have $J_0(\beta)$ and $J_1(\beta)$ values for $\beta = 0$, and then for $\beta = 0.1$, and are therefore useless for determining sideband heights for very small β. However, as a result of previous work at Crystal Semiconductor concerning testing T1 line interface parts for very low jitter specifications [2], a useful relationship between β and $J_1(\beta)/J_0(\beta)$ was noticed:

$$J_1(\beta)/J_0(\beta) = \beta/2 \qquad \text{(only for very small } \beta) \qquad (3)$$

This relationship is also confirmed by approximations for Bessel coefficients given in [3].

Using (3) gives us a $J_1(\beta)/J_0(\beta)$ ratio of 3.424×10^{-5}, which is -89.3 dB. Quantization noise for a 16-bit, Nyquist sampling ADC is -122 dB peak with respect to a 0dB full scale input. Assuming the ADC is normally run at -10 dB input level for full amplitude music, then the sidebands have to be -112 dB down to guarantee non-audibility. Therefore for our example, the sidebands may be audible (ignoring masking effects of the ear).

How much clock jitter will cause a sideband to rise above the quantization noise floor, and therefore be potentially audible ? Using the above equations, and for an input frequency of 10900 Hz, assuming a 16-bit ADC, the answer is 232 ps peak clock jitter. This result aligns well with previously published estimates [4].

2 Clock Jitter Simulations

In order to facilitate the understanding of the effects of clock jitter, a simulation program was written, shown in Figure 1. Line 160 through line 210 form the main program loop, which increments the time sample count, G, by one for each pass. Line 170 calculates the jitter amplitude for each sample. Line 180 simulates a pure cosine input signal, jittered by an amount of time, J. Notice the use of double precision arithmetic. Lines 185 and 200 quantize the output values to X bits. The output of the program is a set of numbers which are written to a file.

To confirm the accuracy of the simulation compared to theory, the program was run with the same input conditions as used in the theory example. The resulting file of numbers was then processed by a standard FFT analysis and display program in routine use at Crystal Semiconductor for testing all types of ADCs [5]. Figure 2 shows the resulting spectrum. The two sidebands are 89.66 dB down from the input frequency amplitude, which agrees closely with the theoretical result.

Modifying line 170 allows changing the nature of the clock jitter. Changing line 180 allows investigation of different ADC input signals.

3 Measured Results

A CS5101 sampling successive approximation ADC was used to verify the theoretical and simulation results. Figure 3 shows the test set-up. A 6.144 MHz clock was used to allow later substitution of an alternate delta-sigma ADC. Using a 6.144 MHz clock determines the sample rate of 76.8 kHz. Figure 4 shows the Phase Lock Loop (PLL) circuit used to inject clock jitter. The set-up was verified to introduce no additional distortion compared to a jitter free crystal based clock source. Clock jitter is added by injecting the desired jitter modulation signal into the Voltage Controlled Oscillator (VCO) of the PLL.

Using the same conditions as used for the theoretical and simulation example, the sidebands were shown to be 89.74 dB down from the input frequency component, shown in Figure 5. This validates the theory and simulation results. The clock jitter was checked by displaying a divided down version of the jittered clock on a delayed time base oscilloscope. Figure 6 shows a rising edge of the divided clock, corrupted by 1 ns peak jitter. This measurement was taken at the same time as the Figure 5 test result plot.

Correlation between clock jitter amplitude and side-band height has previously been verified at Crystal Semiconductor by compared the jitter readings of an HP 3785A jitter test unit with the same clock jittering an ADC sampling clock [2].

4 Oversampling ADC Clock Jitter Sensitivity

Oversampling delta-sigma ADC's have several advantages over more traditional Nyquist sampling successive approximation ADC's and are also becoming more available [6] .The CS5326 from Crystal Semiconductor has an oversampling ratio of 64, sampling the input at 3 MHz. The output of the delta sigma modulator is a 3 MHz serial bit stream which is then digitally filtered (dc to 22 kHz) and decimated to produce 16-bit numbers at a 48 kHz word rate. How sensitive is such an ADC to clock jitter ?

As a proportion of clock period, a given amount of jitter is more significant to a 3MHz sampling clock, compared to a 50 kHz sampling clock. However the amount of amplitude error resulting from the clock jitter is the same in both cases, since the slew rate of the input signal is the same. Also, for noise induced jitter, the extra noise induced by the jitter will be spread out between dc and 1.5 MHz, and then low pass filtered by the 22 kHz cut-off digital filter. Thus it is reasonable to speculate that an oversampling delta-sigma ADC will be no more sensitive to clock jitter than a Nyquist sampling ADC. To prove this hypothesis, a theoretical simulation was performed, along with measured results.

Figure 7 shows the results of the CS5326 oversampled ADC simulation program. The input conditions were the same as previously used, that is an input frequency of 10900 Hz, 1ns peak sinusoidal 980Hz jitter, and -10 dB input amplitude. The difference in amplitude between the fundamental and the jitter induced sidebands is 89 dB, which is the same result as obtained in the Nyquist sampling case. The lack of low frequency noise in Figure 7 is because the simulation did not include the final truncation to 16-bits after the filter.

Figure 8 shows the measured results from the CS5326 oversampled ADC. The test conditions were the same as above, and the test set-up was the same as shown in Figure 3, using a CDB5326 evaluation board. The plot shows that the difference in amplitude between the fundamental and the jitter induced sidebands is 89.5 dB, which agrees well with the oversampled ADC simulation results, and with the previously given non-oversampled ADC test results.

The above results confirm that an oversampled delta-sigma ADC has the same sensitivity to clock jitter as a Nyquist sample rate ADC.

5. Non Sinusoidal Jitter

In practical hardware, clock jitter will not be sinusoidal. It is likely to consist of noise components and some periodic components. To investigate the effects of white noise jitter, the simulation program given in Figure 1 was modified, replacing the sine jitter equation with a random number generator equation (Figure 9).

A number of simulations were run which show that white noise clock jitter results in an overall elevation of the noise floor of the ADC system. This will degrade the available dynamic range. For example, 2 ns peak white noise clock jitter will degrade a perfect 16-bit ADC from a dynamic range of 98 dB to 91 dB (Figures 10 &11). To reduce clock jitter effects to less than 0.5 dB impact on dynamic range, the peak jitter amplitude has to be less than 400 ps (Figure 12).

6. Conclusions

A combination of theoretical analysis, computer simulations and practical measurements has allowed the confident prediction of the audible effects of sampling clock jitter. As the resolution, and therefore dynamic range, of ADC's and DAC's increase beyond 16-bits, sampling clock jitter will become more significant. The analysis techniques presented allow maximum allowable levels of clock jitter to be determined.

It has been demonstrated that delta-sigma oversampling ADC's are no more or less susceptible to the effects of clock jitter than Nyquist sampling architectures.

7. Acknowledgements

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8. References

[1] H. Taub & D.L. Schilling, "Principles of Communication Systems," McGraw-Hill, pp 113-131.

[2] Lamay J.L. & Caldwell D.C., "A Telecommunications Line Interface Test System Architecture", Proceedings of the IEEE International Test Conference, 1989, pp 216-221.

[3] Pipes, L.A., "Applied Mathematics for Engineers and Physicists", McGraw-Hill Book Company, New York, 1958.

[4] Lidbetter, P.S., "Basic Concepts and Problems of Synchronization of Digital Audio Systems", Presented at AES 84th Convention, Paris, March 1988

[5] Harris S., " Dynamic Techniques Test High-Resolution ADCs on PCs", Electronic Design, September 3, 1987.

[6] Welland D.R. et al, "A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio", J. Audio Eng. Soc., Vol. 37, No. 6, June 1989.

```
10 REM  ADC SIMULATION PROGRAM "JITSINE"    Steven Harris  8/3/89

95 INPUT "Number of samples in output file ?",SIZE
96 REM Set X = to # of bits in ADC
97 LET X = 16
100 PRINT "JITSINE generates ";SIZE;" numbers quantised to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "Sine wave jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Signal Frequency ?", FIN#
146 INPUT "Input Signal Amplitude relative to full scale (=1) ", INAMP#
147 INPUT "Jitter Frequency ?",FJ#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
168 REM Form jitter amplitude for this time sample
170 LET J# = JPA#*SIN(Offsetj + ((G-1)*2*PI#*FJ#/FS#))
172 REM Form unquantized clock jittered cosine value for this sample
180 LET A# =INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "######";S
210 NEXT G
220 CLOSE #1
230 GOTO 95
```

Figure 1. BASIC program which simulates a perfect N-bit ADC with sinusoidal clock jitter

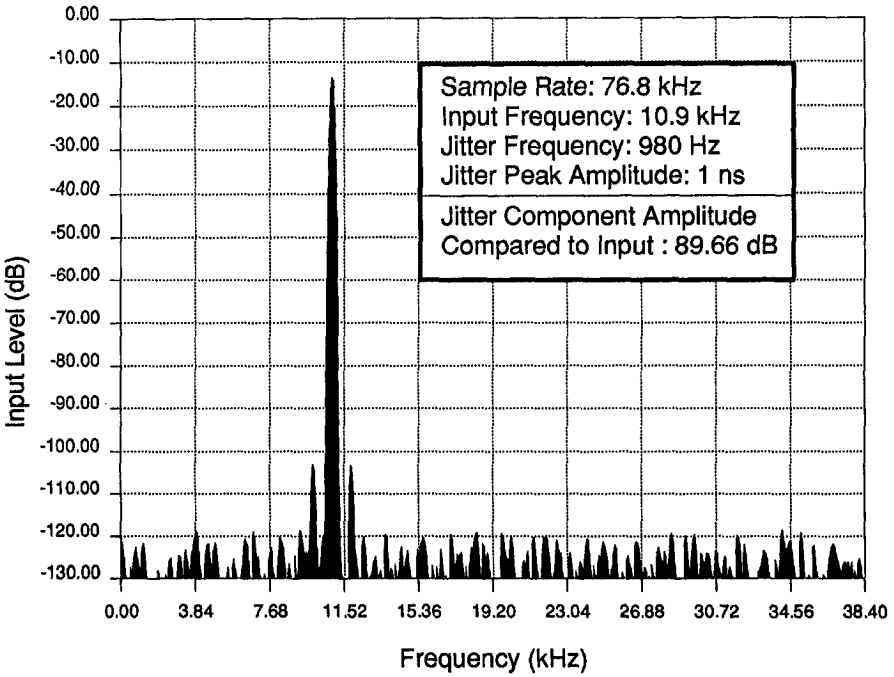

Figure 2. Nyquist Sampling ADC Simulation with 1ns Peak SIne Clock Jitter

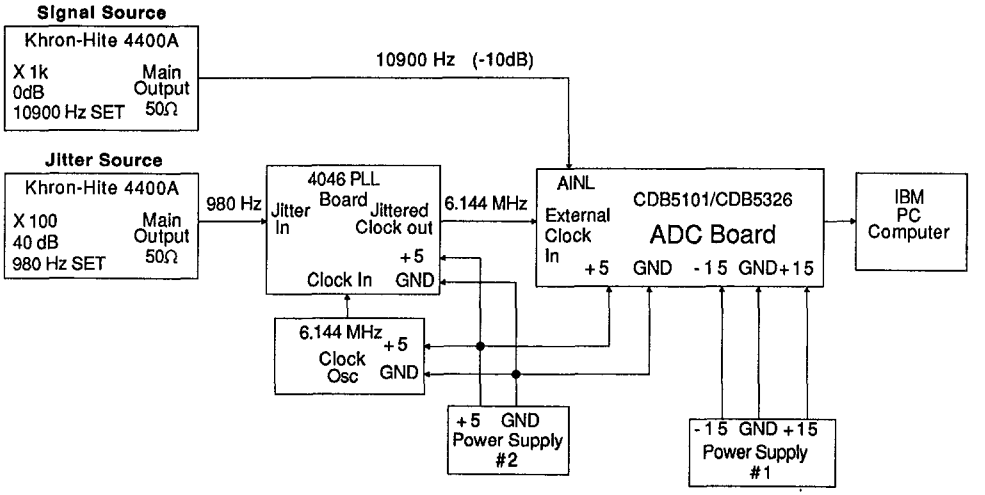

Figure 3. Jitter Experiments Test Set-up

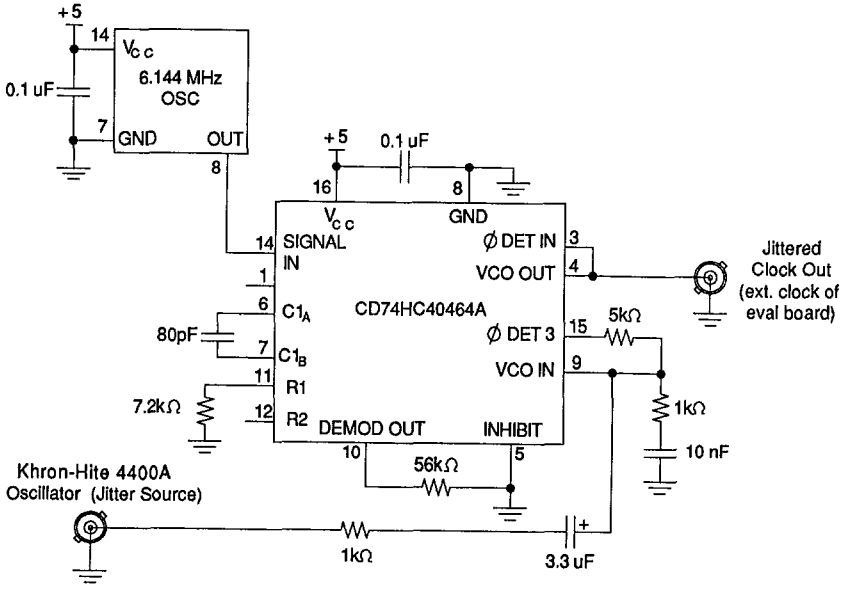

Figure 4. Phase Locked Loop Jitter Generator Schematic

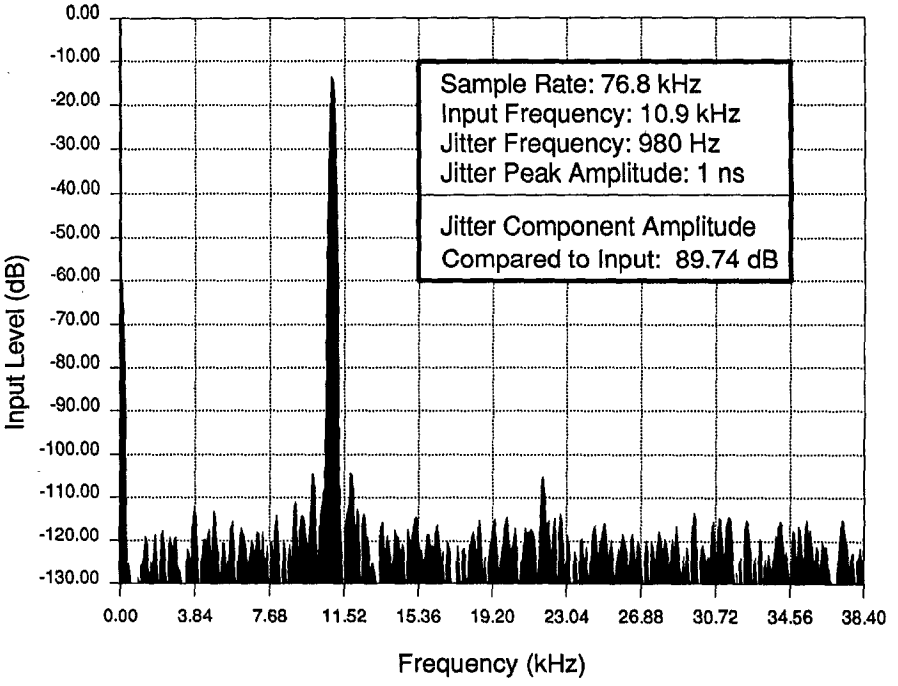

Figure 5. Measured Nyquist Sampling ADC (CS5101) with 1 ns Peak Sine Clock Jitter

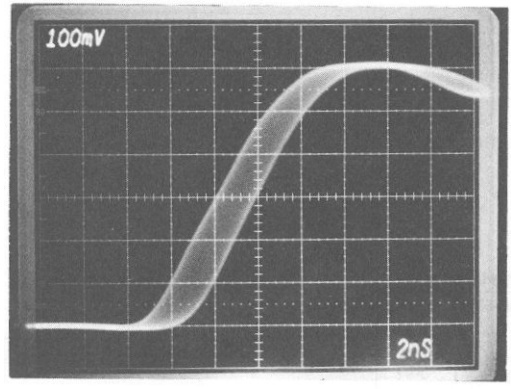

Figure 6. ADC Sampling Clock Jitter Measured at the Output of the Clock Jitter Generator Shown in Figure 4

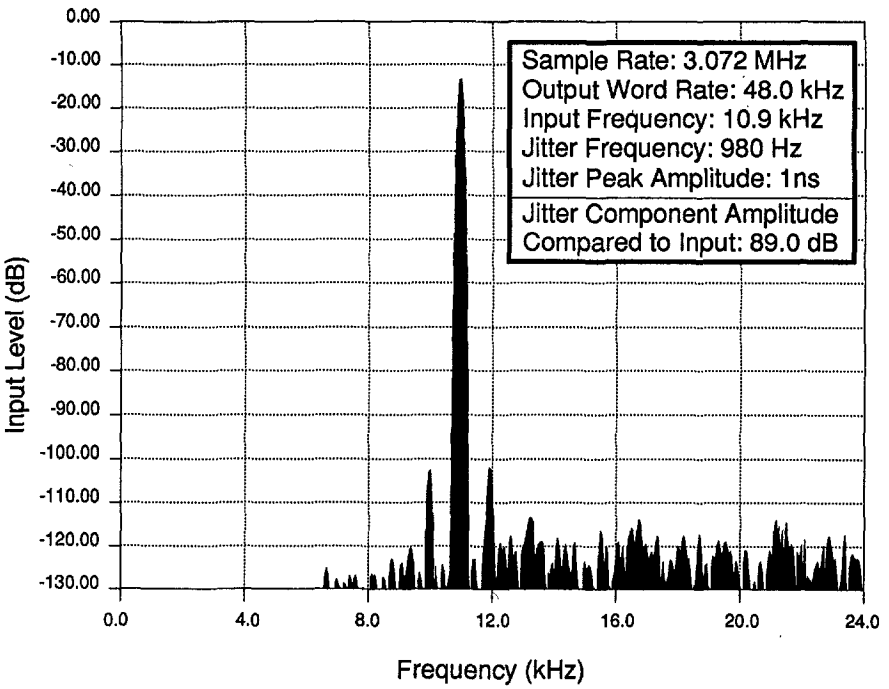

Figure 7. Simulated 64 x Oversampling Delta Sigma ADC with 1 ns Peak Sine Clock Jitter

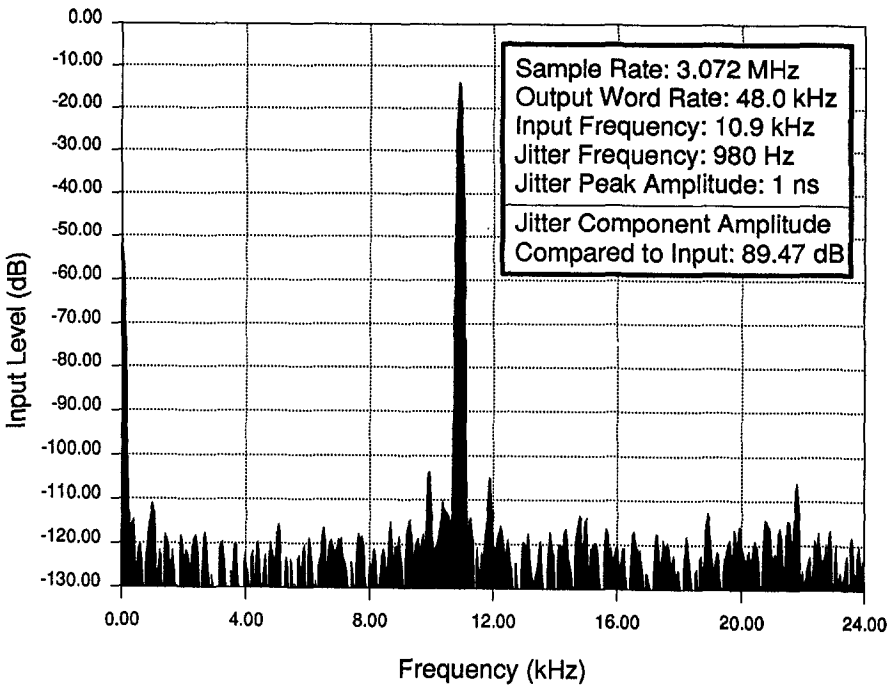

Figure 8. Measured 64 x Oversampling Delta Sigma ADC (CS5326) with 1 ns Peak Sine Clock Jitter

```
10  REM  ADC SIMULATION PROGRAM  "JITNOISE"  Steven Harris 8/3/89

95  INPUT "Number of samples in output file ?",SIZE
96  REM Set X = to # of bits in ADC
97  LET X = 16
100 PRINT "JITNOISE generates ";SIZE;" numbers quantised to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "White noise jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Frequency ?", FIN#
146 INPUT "Input signal amplitude relative to full scale (=1) ?", INAMP#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
169 LET NOISE=RND
170 LET J# = JPA#*(NOISE*2-1)
172 REM Form perfect clock jittered sine
180 LET A# = INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "######";S
210 NEXT G
220 CLOSE #1
230 GOTO 95
```

Figure 9. BASIC program which simulates a perfect N-bit ADC with noise jittered clock

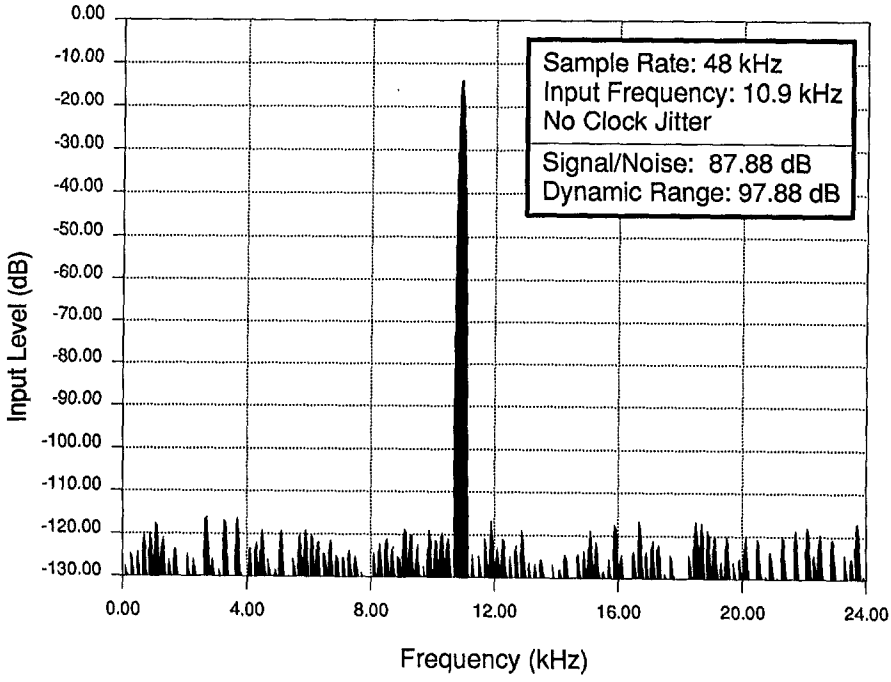

Figure 10. Nyquist Sampling ADC Simulation with No Clock Jitter

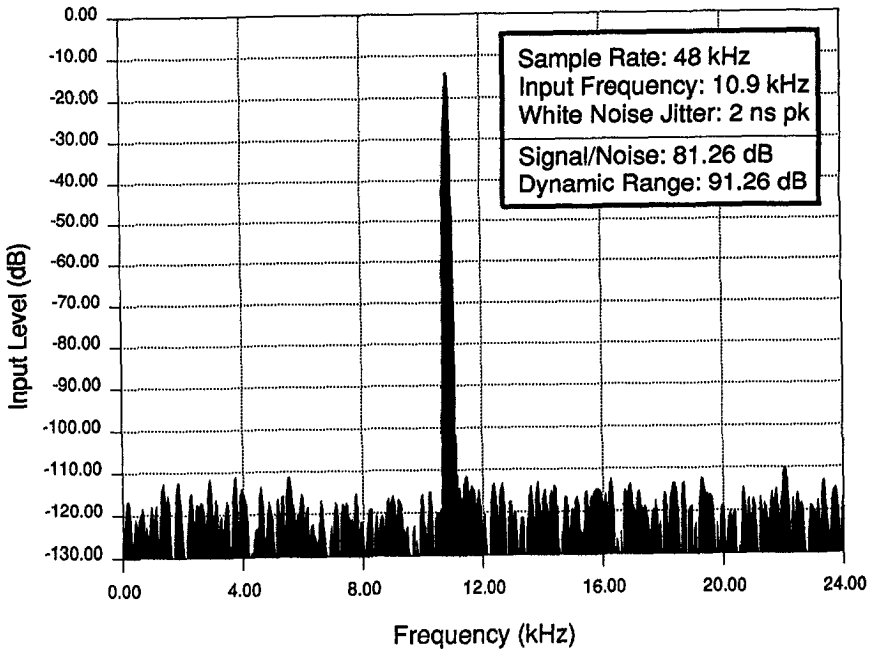

Figure 11. Nyquist Sampling ADC Simulation with 2 ns Peak White Noise Clock Jitter

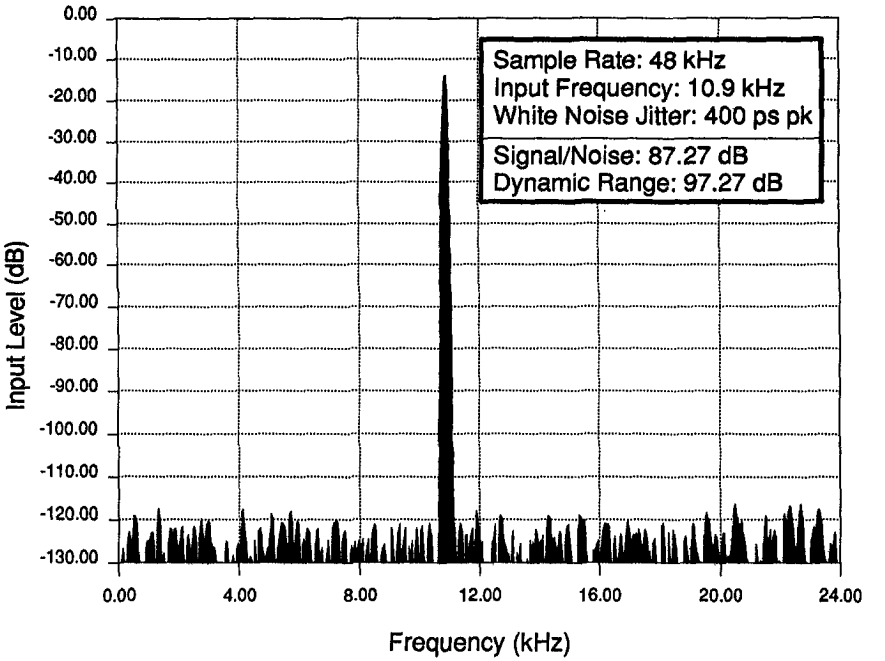

Figure 12. Nyquist Sampling ADC Simulation
with 400 ps Peak White Noise Clock Jitter