DRIVING CAPACITIVE LOADS

The internal compensation of the AD817, together with its high output current drive, permit excellent large signal performance while driving extremely high capacitive loads.

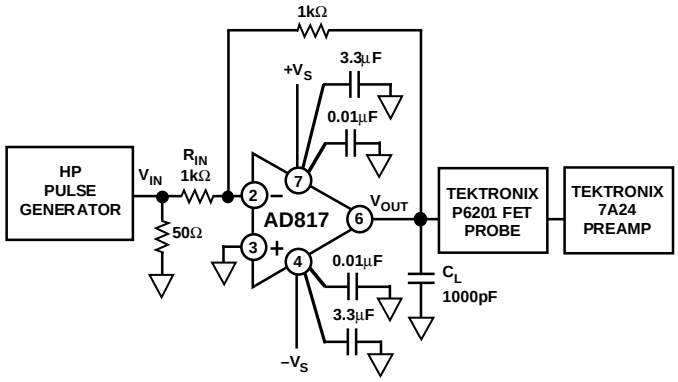

Figure 30a. Inverting Amplifier Driving a 1000 pF Capacitive Load

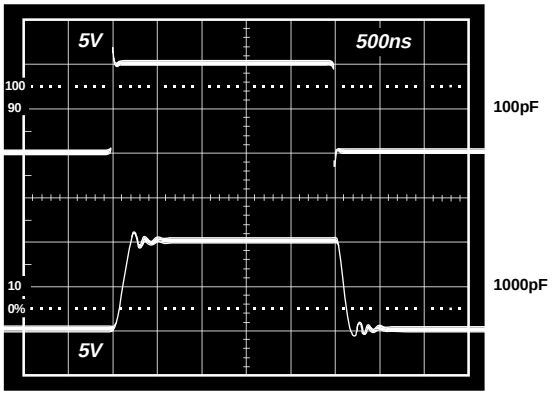

Figure 30b. Inverting Amplifier Pulse Response While Driving Capacitive Loads

THEORY OF OPERATION

The AD817 is a low cost, wide band, high performance operational amplifier which effectively drives heavy capacitive or resistive loads. It also provides a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD817 (Figure 31) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

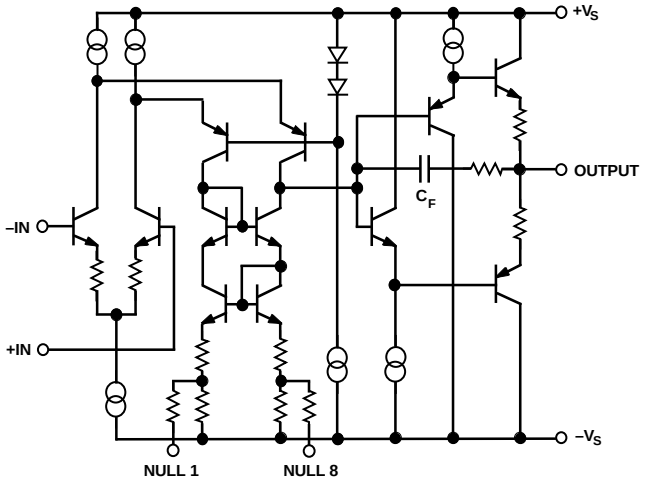

Figure 31. Simplified Schematic

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 22) is required in circuits where the input to the AD817 will be subjected to transient or continuous overload voltages exceeding the +6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

GROUNDING & BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (<1 kΩ) to assure that the time constant formed with the inherent stray capacitance at the amplifier's summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of R_F/R_{IN}, form a pole in the loop transmission which may result in peaking. A small capacitance (1 pF–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μF are recommended.

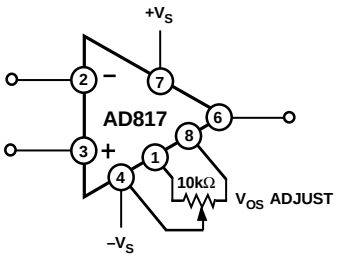

Figure 32. Offset Null Configuration