A Study on Differential Mode to Common Mode Conversion due to Asymmetric Structure in Differential Transmission Line

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***Abstract*—Recently, differential transmission lines which have low electromagnetic radiation performance are widely used for high speed digital interconnections. Though high electrical balance is required to obtain that performance, degradation of the balance may often occur from asymmetry of the structure, such as additional patterns and electrical components connected to one or both of single lines of differential transmission line. In that case, some part of differential-mode signal is converted to common-mode signal, which may often increase electromagnetic radiation from the differential transmission line. It is therefore important to reduce the differential mode to common mode conversion ratio (S_{cd21}) by keeping the electrical balance in the design stage in order to provide low EMI equipments. In this paper, we present an equivalent circuit model to evaluate the mode conversion due to the asymmetry of structure. The additionally connected patterns and components are modeled with a shunt capacitor connected between the single line and the ground. Then, S_{cd21} can be expressed as a simple function of the frequency and the capacitance difference between each single line of the differential transmission line, and is independent on the position of the capacitors. The proposed model is verified by the comparison of calculated S_{cd21} with the experimental results, and is applicable in low EMI design of differential transmission lines.**

Keywords—EMC; EMI; common-mode signal; differential transmission line; component

I. INTRODUCTION

Recently, differential transmission lines which have low electromagnetic radiation performance are widely used for high speed digital interconnections. Though high electrical balance of the transmission line is required to obtain that performance, degradation of the balance may often occur from asymmetry of the structure. Fig.1 shows block diagram of High Speed Digital Interconnections Interface. Signal is transmitted from a physical layer chip (PHY) to connector through the differential transmission line on the printed circuit board. A pulse transformer and a common mode choke coil are often used for reducing the common mode signal generated by the PHY. But, sometimes additional circuits are inserted between such devices and the connector. For example, lightning protection circuits are connected as shown in Fig.2. The lightning protection circuit is realized by connecting each single transmission line and the ground pattern through a branching pattern and an arrester. By the constraints of printed circuit board layout design, the branching patterns and the arresters may often be arranged asymmetrically to the two single transmission line patterns, as shown in Fig. 3. In that case, the structure causes a degradation of electrical balance, and some part of differential-mode signal is converted to common-mode signal, which may often increase electromagnetic radiation from the differential transmission line. It is therefore important to reduce the differential mode to common mode conversion ratio (S_{cd21}) by keeping the electrical balance in the design stage in order to provide low EMI equipments.

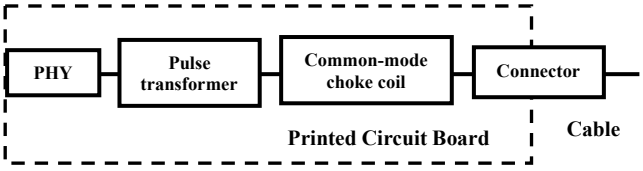

Fig. 1. Block diagram of the High Speed Digital Interconnections Interface

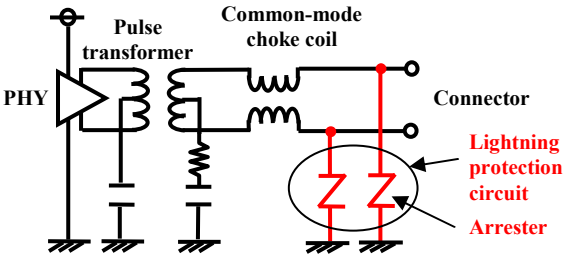

Fig. 2. Equivalence circuit of the High Speed Digital Interconnections Interface with additionally connected patterns and components

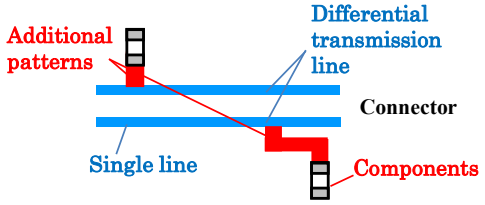

Fig. 3. The asymmetry the structure caused by the additional patterns and components.

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In this paper, we present an equivalent circuit model to evaluate the mode conversion due to the asymmetry of structure. We assumed that the additionally connected patterns and components such as lightning protection circuits can be modeled with a shunt capacitor connected between the single line and the ground. By analyzing the circuit model, it is found that, S_{cd21} is expressed as a simple function of the frequency and the capacitance difference between the capacitors connected to each single line of the differential transmission line, and S_{cd21} is independent on the position of the capacitors.

II. The Capacitor Model

A. *Modeling of the additionally connected patterns and components*

In order to evaluate the differential mode to common mode conversion ratio (S_{cd21}) caused by the asymmetric structure, we obtain a simple equivalent circuit model. First, we assume that the additional patterns and components connected to the single lines can be modeled with a shunt capacitor connected between the single line and the ground. Then, we apply the capacitor model to the equivalent circuit of the transmission line.

If the size of the additional pattern is much smaller than the wave length of the signal, the pattern can be modeled by a parallel prate capacitor shown in Fig.4, and the capacitance of the pattern can be calculated approximately by the following equation.

$$C = \varepsilon \frac{S}{d} \quad , \tag{1}$$

where ε is permittivity of dielectric, S is area of the metal pattern, d is distance between the metal pattern and ground plane. Some components such as arresters can be modeled by a capacitor, because these components have two facing electrodes which are insulated in the ordinary state. Most of other components such as inductors can be disregarded because they will have high impedance characteristics at high frequency to avoid an electrical influence to the high speed transmission signal.

To verify the above assumption, we measured the differential mode to common mode conversion characteristic by an asymmetrically connected arrester. Fig. 5 shows the measured test board (PWB) with differential transmission line and an arrester connected to one of the transmission line pattern(Line 1). The frequency response of $|S_{cd21}|$ is shown in Fig. 6. The solid line show the measured characteristic of the test board and the dashed line show the calculation result of the case where the shunt capacitor is connected to one of the line and ground. It is confirmed that the characteristic of the arrester can be expressed by a shunt capacitor.

By applying the capacitor model, the differential transmission line including the additional patterns and components as shown in Fig.3 can be expressed by an equivalent circuit shown in Fig.7.

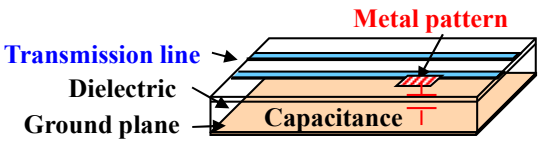

Fig. 4. Top perspective view of PWB of which additional additional patterns and components are modeled with metal pattern.

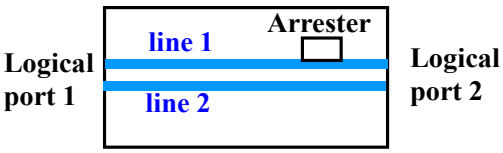

Fig. 5. Top view of PWB with component

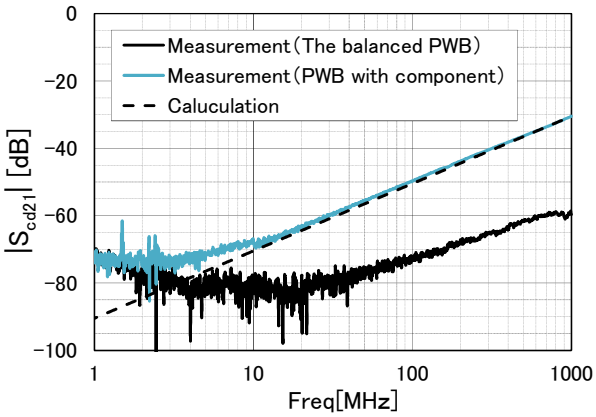

Fig. 6. Caluculation and experimental result of PWB with component

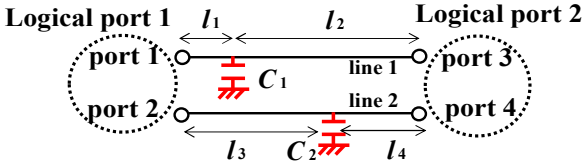

Fig. 7. The equivalent circuit model of PWB with additional patterns and components

B. *Circuit analysis*

We derive the relationship between the asymmetric structure and S_{cd21} by analyzing the equivalent circuit of Fig.7. We consider S_{cd21} of logical port 1 and 2. S_{cd21} is given as[1]

$$S_{cd21} = \frac{1}{2}\left(S_{31} - S_{32} + S_{41} - S_{42}\right), \tag{2}$$

In the S_{mn}, m is the output port, n is the input port. Under the assumption of low interaction between line 1 and line 2, or S_{32}, $S_{41} << S_{31}$, S_{42}, S_{cd21} is approximated as follows,

$$S_{cd21} = \frac{1}{2}\left(S_{31} - S_{42}\right) . \tag{3}$$

Here, we consider two-port S-parameter of single ended port 1 and port 3. Line 1, from port 1 to port 3 line, can divide each element, l_1 length line, capacitance C_1, and l_2 length line. T-parameter of the finite length l transmission line is expressed as

$$\begin{bmatrix} e^{-jl} & 0 \\ 0 & e^{jl} \end{bmatrix}. \tag{4}$$

When the capacitance C is connected to transmission line, T-parameter is expressed as

$$\begin{bmatrix} 1-\frac{j\omega C}{2Y_0} & -\frac{j\omega C}{2Y_0} \\ \frac{j\omega C}{2Y_0} & 1+\frac{j\omega C}{2Y_0} \end{bmatrix}, \tag{5}$$

where ω is angular frequency, Y_0 is characteristic admittance of transmission line. The T-parameter of line 1 is calculated by multiplication (4) and (5).

$$\begin{aligned} \begin{bmatrix} T_{11} & T_{13} \\ T_{31} & T_{33} \end{bmatrix} &= \begin{bmatrix} e^{-jl_1} & 0 \\ 0 & e^{jl_1} \end{bmatrix} \begin{bmatrix} 1-\frac{j\omega C}{2Y_0} & -\frac{j\omega C}{2Y_0} \\ \frac{j\omega C}{2Y_0} & 1+\frac{j\omega C}{2Y_0} \end{bmatrix} \begin{bmatrix} e^{-jl_2} & 0 \\ 0 & e^{jl_2} \end{bmatrix} \\ &= \begin{bmatrix} \left(1-\frac{j\omega C}{2Y_0}\right)e^{-j(l_1+l_2)} & -\frac{j\omega C}{2Y_0}e^{j(l_2-l_1)} \\ \frac{j\omega C}{2Y_0}e^{j(l_1-l_2)} & \left(1+\frac{j\omega C}{2Y_0}\right)e^{j(l_1+l_2)} \end{bmatrix} \end{aligned} \tag{6}$$

In the T_{mn}, m is the output port, n is the input port. Two-port S-parameter of single ended port 1 and port 3 is calculated from T-parameter, as follows,

$$\begin{aligned} \begin{bmatrix} S_{11} & S_{13} \\ S_{31} & S_{33} \end{bmatrix} &= \frac{1}{T_{33}} \begin{bmatrix} T_{13} & T_{11}T_{33}-T_{13}T_{31} \\ 1 & -T_{31} \end{bmatrix} \\ &= \frac{1}{\left(1+\frac{j\omega C}{2Y_0}\right)e^{j(l_1+l_2)}} \begin{bmatrix} -\frac{j\omega C}{2Y_0}e^{j(l_2-l_1)} & \left(1-\frac{j\omega C}{2Y_0}\right)\left(1+\frac{j\omega C}{2Y_0}\right)+\left(\frac{j\omega C}{2Y_0}\right)^2 \\ 1 & -\frac{j\omega C}{2Y_0}e^{j(l_1-l_2)} \end{bmatrix} \\ &= \frac{2Y_0}{2Y_0+j\omega C}e^{-j(l_1+l_2)} \begin{bmatrix} -\frac{j\omega C}{2Y_0}e^{j(l_2-l_1)} & 1 \\ 1 & -\frac{j\omega C}{2Y_0}e^{j(l_1-l_2)} \end{bmatrix} \end{aligned} \tag{7}$$

The two-port S-parameter of line 2, from port 2 to port 4 line, is obtained in the same manner.

Substituting for (3) from (7), we obtain

$$S_{cd21} = \frac{1}{2}\left(\frac{2Y_0}{2Y_0+j\omega C_1}e^{-j(l_1+l_2)} - \frac{2Y_0}{2Y_0+j\omega C_2}e^{-j(l_3+l_4)}\right) \tag{8}$$

Since the whole length of line 1 and line 2 are equal, (8) can be rewritten as follows, using $l_1+l_2=l_3+l_4=l$,

$$S_{cd21} = \frac{1}{2}\left(\frac{2Y_0}{2Y_0+j\omega C_1} - \frac{2Y_0}{2Y_0+j\omega C_2}\right)e^{-jl} \tag{9}$$

Under the assumption of $2Y_0 \gg \omega C_1,\ \omega C_2$, the approximate expression of S_{cd21} is obtained by dropping a squared or higher term of $\omega C_1,\ \omega C_2$.

$$S_{cd21} = \frac{1}{2}\left(\frac{2Y_0}{2Y_0+j\omega\Delta C} - 1\right)e^{-jl} \tag{10}$$

Then, S_{cd21} can be expressed as a simple function of the frequency and the capacitance difference between each single line of the differential transmission line (ΔC). (10) also shows that S_{cd21} is depend on only ΔC and is independent on the position of capacitances. Fig. 8 shows the relationship between $|S_{cd21}|$ and ΔC at 125 MHz (fundamental frequency of the100M Ethernet PHY chip).

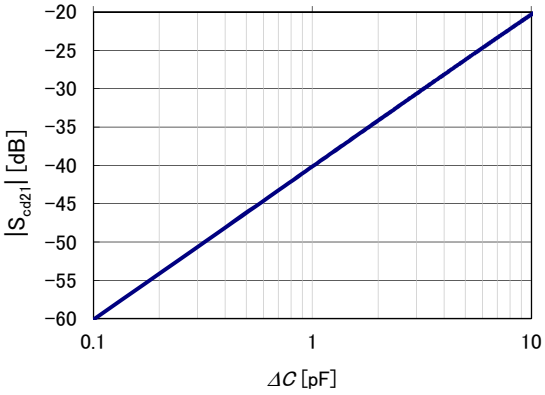

Fig. 8. Caluculation result of $|S_{cd21}|$ (@125MHz)

III. Comparison with Experimental Result

A. Configuration of the test printed circuit board

To confirm the simplified expression of S_{cd21} (Eq.10) , we fabricated some test printed wiring boards (PWBs) and compared the measured characteristic of S_{cd21} and calculated S_{cd21} using Eq.10. "The balanced PWB" and "PWB with metal pattern 1 and 2" are made, as shown in Fig. 9.

The PWB is made of FR-4 (relative permittivity: 4.3 @1 GHz, dielectric thickness: 0.8 mm, dielectric dissipation factor: 0.02). The size of PWB is 80 by 40 mm. The size of microstrip line structure is length l = 80 mm, width w = 1.5, thickness h = 0.035 mm, the spacing s = 2.0 mm. The differential transmission lines (line 1, line 2) are located top layer of PWB with characteristic impedance of transmission line Z_0 = 50 Ω. The line extended both ends of boards to connect SMA end launch connector. A ground plane is located in bottom layer. In this PWBs, we add a metal pattern to the microstrip pattern as a symmetric structure. Table 1 shows the equivalent capacitances of the metal patterns on each test PWB. "The balanced PWB" has no additional metal pattern. "PWB with metal pattern 1 and 2" are asymmetrical topology with different metal pattern size and layout, but with same capacitance difference ΔC.

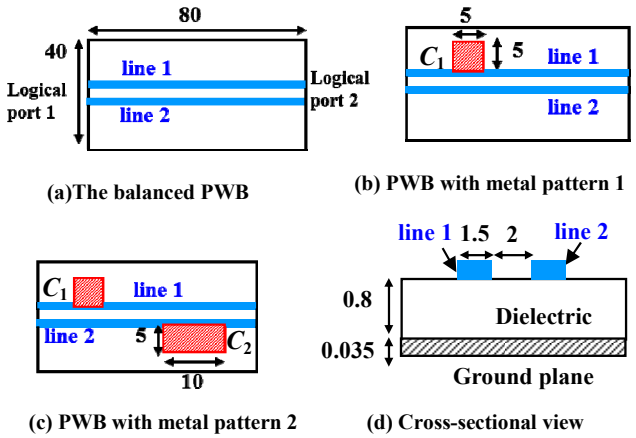

Fig. 9. Geometries of the PWBs (in mm)

TABLE I. CAPASITANCE OF EACH PWB

	C_1 [pF]	C_2 [pF]	ΔC [pF]
The balanced PWB	0	0	0
PWB with metal pattern 1	1.2	0	1.2
PWB with metal pattern 2	1.2	2.4	1.2

B. Measurement and calculation of S_{cd21}

The mixed-mode S-parameters of PWBs are measured. A four-port vector network analyzer (Agilent 85052D) was used to take the mixed-mode S-parameter measurement. The frequency response of $|S_{cd21}|$ is shown in Fig. 10. The solid and dashed lines show the experimental results from the network analyzer with 4 ports, and the calculation result from (10), respectively. Measured $|S_{cd21}|$ of "The balanced PWB" is about -70 dB at 125 MHz. On the other hand, measured $|S_{cd21}|$ of "PWB with metal pattern 1 and 2" are about -40 dB at 125 MHz. Thus the degradation of the balance causes an increase of S_{cd21}. And calculation result from (10) with ΔC = 1.2 pF (from Table 1) is good agreement with experimental result. So the proposed model is verified.

If S_{cd21} threshold is defined from the regulation value of EMI, optimal value of ΔC is derived from (10). Furthermore, "PWB with metal pattern 1 and 2" have same ΔC, but number and position of capacitances is different. But, from the calculation, it is found that S_{cd21} did not change by the number or position of the capacitors, and the result shows a good agreement with a measurement. We confirm S_{cd21} is determined by the capacitance difference between two lines of differential transmission line, and is independent on the position of the capacitors.

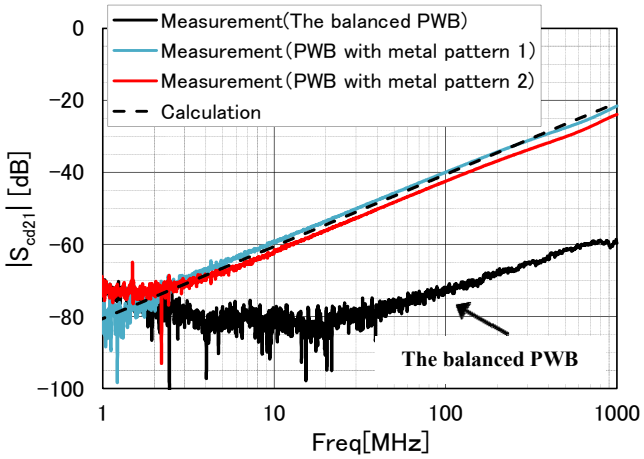

Fig. 10. Caluculation and experimental result

IV. SUMMARY

The proposed model is verified by the comparison of calculated S_{cd21} with the experimental results, and is applicable in low EMI design of differential transmission lines. From the study using the proposed model, it is found that S_{cd21} is determined by the capacitance difference between two lines of differential transmission line, and is independent on the position of the capacitors.

REFFERENCES

[1] William R. Eisenstad, Bob Stengel, Bruce M. Thompson, "Microwave Differential Circuit Design Using Mixed-Mode S-Parameters", 2006, Artech House