A new audio amplifier topology with push-pull transimpedance stage – Part 2: Biasing, stability and AC performance

Samuel Groner - September 26, 2012

*This article originally appeared in **Linear Audio** Volume 2, September 2011. Linear Audio, a book-size printed tech audio resource, is published half-yearly by **Jan Didden**.*

*[**Part 1** introduces an audio amplifier topology which uses a novel push-pull transimpedance stage that offers a substantial improvement in power supply rejection over standard amplifier configurations.]*

4. Biasing Considerations

The first thing to get right in a circuit design is the biasing conditions. So I will, first of all, discuss the necessary considerations in this respect. Please consider figure 6 for this, which shows several additional circuit elements that are essential, or at least very helpful, for a practical realisation.

There are three fundamental bias currents to be chosen for this novel transimpedance stage: the collector current of the emitter followers Q8 and Q9, that of the common-emitter transistors Q10 and Q11, and finally the current in the folded cascodes formed by Q14 and Q15. Needless to say, the collector current of complementary pairs (e.g., Q8 and Q9) should be set to approximately equal values. There are various trade-offs associated with the selection of these bias conditions. Detailed discussion of these is beyond the scope of this article, so I'm just quoting suggested values which will be found to work well in most typical power amplifier designs:

- 0.5–1 mA for Q8 and Q9
- 5–2 mA for Q10 and Q11
- Use the same, or a slightly higher, collector current for Q14 and Q15 as for Q10 and Q11.

The collector current for Q8 and Q9 is easily set by selecting appropriate values for R7 and R8. Biasing Q10 and Q11 requires a bit more thought, however. As mentioned in the previous section, an explicit bias current control circuit will not be required for the new push-pull transimpedance stage. However, to mitigate the sensitivity to transistor tolerances and thermal effects, the addition of emitter resistors is necessary. In figure 6, R11 and R12 realise this. In most cases choosing their values such that they each carry about a 100 mV voltage drop at the nominal collector current of Q1 and Q11 will be sufficient for good bias current stability.

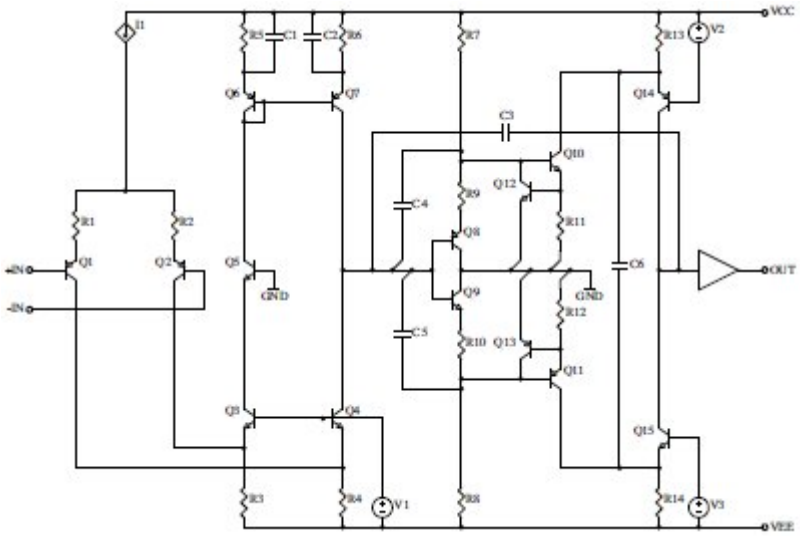

Figure 6: More detailed amplifier schematic using the new second stage topology.

Minimising the value of the emitter resistors is advantageous as this lowers the sensitivity to loading of the second stage output node (details on this can be found in [5]), so going above the suggested 100 mV voltage drop is not advised. Once the emitter resistor value is determined, an appropriate bias voltage is set up by selecting R9 and R10. Simulation can be helpful to derive an initial estimate for the value of these parts, however experimental verification will usually be needed.

The collector current of the folded cascodes (Q14 and Q15) is set both by the emitter resistors (R13 and R14) and the base reference voltage sources V2 and V3. To maximise available output voltage swing the DC voltage drop across the emitter resistors should be minimised; a lower limit of about 200 mV is set by the need that the emitter impedance of the folded cascode transistor (given by the reciprocal of its transconductance) is small compared to the emitter resistor, such that most of the AC collector current of Q10 and Q11 actually flows into the emitter of the corresponding folded cascode (and thus to the output node), rather than into the emitter resistor (and thereafter into the power supply, where it does not produce any usable output).

After discussion of the biasing considerations of the transimpedance stage, we will turn our attention to the folded cascodes of the input stage (Q3 and Q4 in figure 6). As these folded cascodes are part of the input stage, they must be carefully designed to not impair the voltage noise of the amplifier (such considerations are essentially negligible in the second stage, where there is a substantial amount of loop gain available to reduce the impact of the corresponding folded cascodes).

That's particularly important if, as routinely done in audio power amplifiers, the input stage transconductance is reduced by the addition of emitter resistors in the differential pair (note R1 and R2). While the emitter degeneration is very useful for improving input stage distortion and slew rate [1, 2], it also pronounces noise contributions from following stages.

As detailed in the appendix, there are several design strategies available to minimise the impact of the folded cascodes:

- Maximise the value of the emitter resistors by minimising the quiescent current of the folded cascode transistor and the use of a voltage reference with large DC voltage.
- Use a voltage reference with low noise and low impedance.
- Choose transistors with high hFE and low excess noise.

If these strategies are combined they will ensure that amplifier performance is not significantly degraded by the presence of the folded cascodes. There's one caveat regarding the quiescent current of the folded cascode transistors: if it is chosen lower than the collector current of the input differential pair, additional distortion at high frequencies might result (because at peak output currents of the differential pair one or the other folded cascode transistor will switch fully off). Usually the most suitable bias condition for the folded cascode transistors is hence a collector current equivalent to, or slightly above, that of the transistors of the input differential pair.

The current mirror (Q6 and Q7 in figure 6) has a very similar impact on the voltage noise of the amplifier as the folded cascodes Q3 and Q4. As indicated in the appendix, the procedures to minimise its contribution are very similar to those of the folded cascode.Most important, the emitter resistors R5 and R6 should have a large value [5, 9]. Unlike the prior art topologies from figure 1–3, there is plenty of voltage headroom at the current mirror output available, which allows the use of rather large emitter resistors without pushing the current mirror close to saturation.

Figure 6 reveals a last enhancement for the input stage. The common-base transistor Q5 is introduced to keep the folded cascode transistors Q3 and Q4 at approximately the same collector-emitter voltage. This minimises offset due to Early effect and different thermal operating points. Moreover, the base current of this additional transistor partially cancels the base current errors of the current mirror. This further reduces amplifier offset voltage.

5. Stability and AC Performance

Having clarified the basic biasing conditions, let us focus on stability and AC performance. The stability of the global feedback loop does not need any special attention (in this article, not as general design practice!), as AC open-loop gain is defined the same way as for prior art two-stage topologies - namely by the input stage transconductance and the Miller compensation capacitor C3 [1, 2, 3]. However the stability of the local Miller compensation loop should be considered, as additional transistors (the folded cascodes in the second stage, Q14 and Q15 in figure 6) are now included within this loop. These necessarily contribute some delay and phase shift, which could impact stability margins.

I have stated above that folded cascodes reduce stability margins by a small amount only; this applies solely to the global feedback loop (and hence to the folded cascodes of the input stage), which, for audio power amplifiers, typically has a unity loop gain frequency in the order of 1 MHz or less. However the bandwidth of the local Miller loop of the second stage can extend into the 100 MHz region, and here the effects of an additional common-base stage are not negligible.

The additional delay and phase shift typically manifests itself as gain peaking in the 10–100 MHz region. Generally associated with this is a peak in second stage output impedance, which interacts as an LC resonant network with the input capacitance of the output power buffer. As the latter can be substantially dependent on output voltage and output current, a potential instability mechanism may only be triggered under certain load and signal conditions.

To largely eliminate these effects I've found the use of feed-forward capacitors in the emitter followers of the second stage to be the most dependable and powerful technique [10, 11]. C4 and C5 implement these capacitors. They bypass Q8 and Q9 such that, at high frequencies, the local Miller loop consists of a cascaded common-emitter (Q10 or Q11) and common-base transistor (Q14 or Q15) only. Such a transistor arrangement has excellent stability margins within the local Miller compensation loop, and no significant gain peaking is observed. At low frequencies, where the

impedance of the feed-forward capacitors is large, the emitter followers are fully in the signal path, and improve amplifier performance (in particular low frequency open-loop gain and distortion).

As suitable measurement equipment to quantify gain peaking above the 10 MHz region (i.e., a network analyzer) is not routinely found in audio engineering laboratories, the value of these feed-forward capacitors will in most cases be determined by simulation. The smallest value which still minimises gain peaking is usually the most suitable - typically around 100 pF. It should however be appreciated that,with the standard SPICE transistor models, characterisation of transistor behaviour near the cut-off frequency f_T may be rather inaccurate. If experimental verification reveals a remaining instability mechanism in the Miller compensation loop, the choice of a larger feed-forward capacitor should be considered.

I have promised that the novel amplifier topology will bring absence of slew rate limitations in the transimpedance stage; this was, admittedly, a bit cheating at first. To support very high slew rates the output current of the second stage must be able to dynamically exceed the quiescent current by a substantial amount (at least as long as we apply a reasonable upper limit for quiescent current, for practical reasons). This however is not the case for the new push-pull transimpedance stage, because the output current of the folded cascodes is limited by their bias voltage sources and emitter resistors.

Fortunately there is an easy fix for this; with the use of capacitor C6 (in figure 6) greatly increased transient output currents are made possible. This capacitor acts as a high-frequency level shifter, such that the common-emitter transistor of one half of the transimpedance stage (e.g. Q11) can dynamically increase the collector current of the folded cascode in the other half (Q14). Thereby the operation mode of the transimpedance stage is changed to class AB. There is no primary limit for the value of this capacitor; however its presence means that high-frequency power supply ripple modulates the quiescent current of the folded cascodes. Hence its value should not be chosen larger than necessary. Usually 1 nF is perfectly adequate, and 10 nF should suffice to support even very high slew rates.

It must be appreciated that this slew rate enhancement capacitor cannot increase the second stage output current at low frequencies. It is still necessary to choose a sufficiently high quiescent current to drive the output power buffer. However, as typically the required drive currents increase towards high frequencies (due to the capacitive portion of the input impedance of the output power buffer), the slew rate enhancement capacitor will nonetheless reduce the need for high quiescent currents.

Above I suggested that the emitter resistors of the current mirror (R5 and R6 in figure 6) should have a large value to minimise the noise contribution of the current mirror. However at some point large emitter resistor values will introduce a detectable pole to the open-loop gain of the amplifier, and under some conditions also present a large-signal limitation.[4] The capacitors connected in parallel with the emitter resistors (C1 and C2) avoid this, while preserving the improvement from the emitter resistors at audio frequencies. Typical values for these capacitors range from 1 pF to 1 nF.

[4] The large-signal limitation follows from increased transient output currents in the current mirror,which occur during signals with fast rate of change.With such transient currents the current mirror output may be pushed into saturation, as the voltage across the emitter resistors of the

current mirror momentarily increases.

6. Current Limiting

Another view on figure 6 reveals two last components whose function I've not yet disclosed - Q12 and Q13. These transistors limit the collector current of Q10 and Q11 to a value of about six times the quiescent current. This is necessary because otherwise overload conditions can increase the collector current and power dissipation beyond the maximum rating of typical low power parts. Usually this current limiting scheme will not interfere with the slew rate capability of the amplifier; if necessary, the emitter resistors R11 and R12 may be bypassed with a capacitor to restrict the current limiting to lower frequencies.

The emitter followers (Q8 and Q9) in the transimpedance stage need no explicit protection, as R7 and R8 inherently limit their collector current. Similarly, the average collector current of the folded cascode transistors is limited by their emitter resistors and bias voltage sources, as noted above. The slew rate enhancement capacitor C6 enables increased transient output currents; however, as these are of short duration only, they will not usually trigger a failure condition for the folded cascode transistors.

7. Further Improvement of Power Supply Rejection

As analysed in some detail in the previous sections, the basic power supply rejection limitation of prior art amplifier architectures is absent in the novel topology presented in this article. However, we also need to consider second-order effects at some point.

If the power supply rejection of a typical implementation, based on figure 6, is simulated it is found that the power supply rejection is indeed independent of frequency (that is, at least up to about 10 kHz), but limited to roughly 60 dB (figure related to the output). At high frequencies this is a definite improvement over the performance of standard amplifier topologies, but the restless urge for perfection asks for more.

It is possible to remove many of the second-order effects by circuit modifications (e.g., by replacing R7 and R8 in figure 6 with current sources, or by substituting the simple Widlar current mirror formed by Q6 and Q7 with a more elaborate implementation) and thereby improve power supply rejection, but a far more powerful and yet simpler approach exists.

Due to the voltage gain of typical power amplifier implementations the output voltage swing is far greater than the voltage swing at the amplifier input. Thanks to the structure of the novel topology, only the folded cascodes in the transimpedance stage will see the full output voltage swing. This means that only these circuit elements, which represent a very minor ripple injection route, need to be connected to the main high voltage power supply.

All preceding stages are easily powered from a supply with lower voltage, which must just accommodate the input voltage swing. Such a low voltage power supply is straightforward to derive from the main power supply by the use of simple voltage regulators; note that this comes without the cost of additional mains transformer secondary windings, rectifiers, large smoothing capacitors and so forth. It is hence a very economical solution, adopted without hesitation even for cost sensitive applications.

In figure 7 a possible basic implementation of such an amplifier with regulated supplies for the amplifier front-end is shown. Even if the used shunt regulators (D1, D2, R7 and R8) are just implemented with resistors and discrete zener diodes as shown, the ripple rejection will approach 40

dB, pushing the overall amplifier power supply rejection to 100 dB.

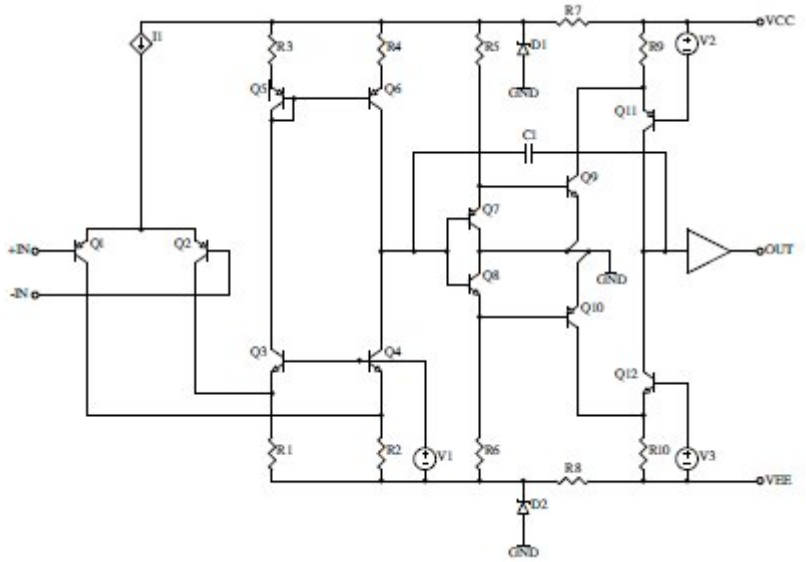

Figure 7: Conceptual amplifier with shunt regulators for the front-end added.

At low frequencies, it is possible to advance things another order of magnitude by the use of more elaborate regulators (e.g., by replacing R7 and R8 with current sources). At high frequencies, the output buffer also contributes some power supply rejection limitations which are not easily removed, and layout effects will be more difficult to control. Currently these figures are based merely on simulation results; however, I have no indication that these should be misleadingly optimistic.

Besides the power supply rejection improvement, there is another benefit from the use of such low voltage, regulated power supplies for the amplifier front-end: the need for transistors with large breakdown voltage ratings is eliminated, and we can choose from a far greater range of transistors with improved performance, e.g., with lower noise and higher h_{FE}. Also as power dissipation is reduced, smaller (and standard surface mounted) packages might be used which is beneficial to reduce cost.

I shall not fail to point out that the use of very low power supply voltages for the input stage may pronounce common-mode distortion at some point. If supply rails substantially below ±15 V are used, this should be carefully evaluated. Usually the use of a bootstrapped cascode [1, 2] for the input differential pair will be a complete cure.

8. Adaptation to Other Input Stage Topologies

So far we have considered the application of the new transimpedance stage to standard voltage feedback input stages with one differential pair only. However, it is perfectly feasible to adapt the new second stage to other input stage structures. Below I will give some examples of this.

In figure 8, an amplifier with complementary differential input pairs is sketched. The output current of each differential pair is made single-ended by an according current mirror (Q5 and Q6, or Q7 and Q8) and subsequently level-shifted to the common input node of the transimpedance stage by folded cascodes Q9 and Q10.

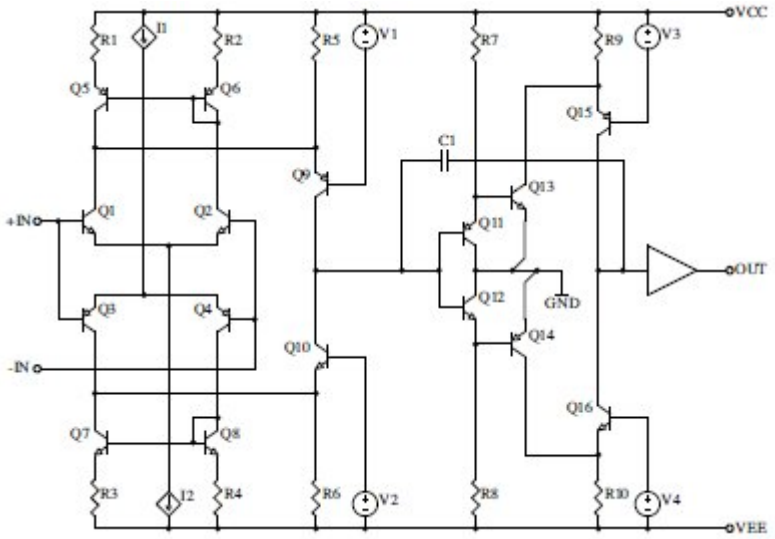

Figure 8: Novel transimpedance stage adapted to an input stage with complementary differential pairs.

With suitable, minor input stage modifications [8] such an amplifier can be designed to support very high slew rates. Note that, compared to the topology from figure 2, there is only one compensation capacitor and no need for a second stage bias control circuit. As for any of the following examples, the use of low-voltage regulated power supplies for the amplifier front-end (as detailed in section 7) is fully supported.

The simplest form of current feedback is implemented as shown in figure 9. This topology is particularly applicable to low level preamplifiers, as only one transistor, Q1, acts as primary noise source. I1 is optional to reduce the rather large bias current flowing from the inverting input terminal. Two amplifiers of this structure may be used to form the front-end of an instrumentation amplifier, such as is in frequent use in transformerless microphone preamplifiers [12].

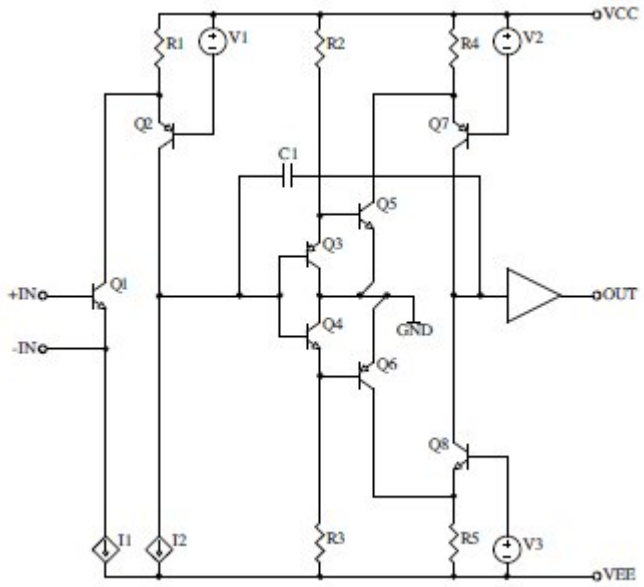

Figure 9: Single-ended current feedback amplifier.

Further improvements regarding large-signal performance may be made with a complementary current feedback input stage (see figure 10).

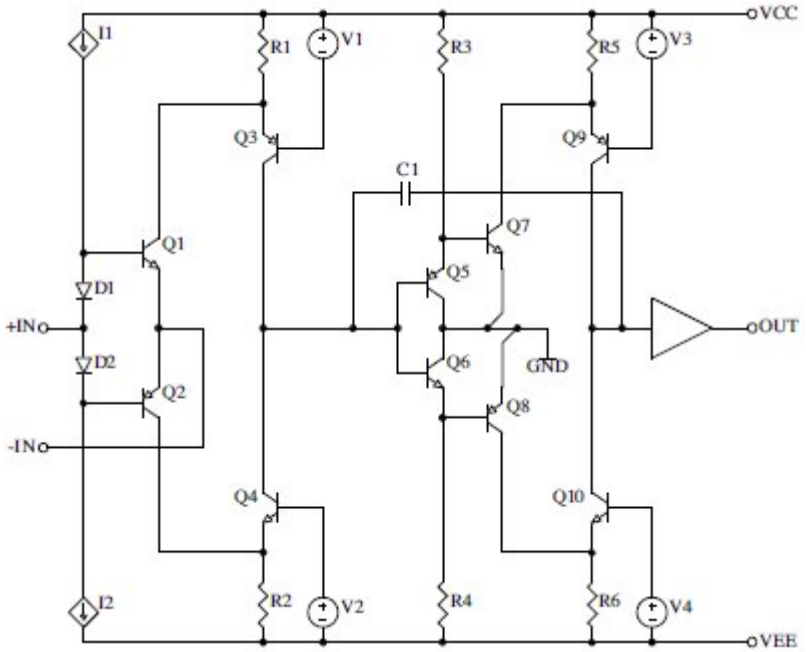

Figure 10: Complementary current feedback input stage combined with new push-pull second stage.

Most complementary current feedback amplifiers are based on one-stage topologies; figure 10 however represents a full two-stage architecture, with the resulting advantages regarding open-loop gain (in the context of current feedback amplifiers usually referred to as *transimpedance*), insensitivity to loading from the power output stage and distortion. Although not discussed further, the use of two transimpedance stages and a suitable amplifier subcircuit for common-mode feedback will permit the design of fully differential amplifiers [13].

Coming up in Part 3: **Experimental verification**.

References

[1] Douglas Self: *Audio Power Amplifier Design Handbook*, 5th edition, Focal Press, 2009
[2] Bob Cordell: *Designing Audio Power Amplifiers*, 1st edition, McGraw-Hill, 2010
[3] J. E. Solomon: *TheMonolithicOp Amp: A Tutorial Study*, IEEE J. Solid-State Circuits, vol. 9, no. 6, pp. 314–332, December 1974
[4] Bhupendra K. Ahuja: *An Improved Frequency Compensation Technique for CMOS Operational Amplifiers*, IEEE J. Solid-State Circuits, vol. SC-18, no. 6, pp. 629–633, December 1983
[5] Samuel Groner: *Comments on Audio Power Amplifier Design Handbook by Douglas Self*, February 2011, available for download from **www.sg-acoustics.ch/analogue_audio/power_amplifiers/pdf/audio_power_amp_design_comments.pdf**
[6] Bruno Putzeys: *The F-word - or,why there is no such thing as too much feedback*, Linear Audio, vol. 1, pp. 112–132, April 2011
[7] Royal A. Gosser, Jeffrey A. Townsend: *Integrated-Circuit (IC) AmplifierWith Plural Complementary Stages*, US Patent 5,537,079, filed December 1994, issued July 1996
[8] Giovanni Stochino: *Ultra-fast amplifier*, Electronics &WirelessWorld, pp. 835–841, October 1995
[9] Alberto Bilotti: *Noise Characteristics of Current Mirror Sinks/Sources*, IEEE J. Solid-State Circuits, vol. SC-10, no. 6, pp. 516–524, December 1975
[10] William H. Gross: *New High Speed Amplifier Designs, Design Techniques and Layout Problems*, Analog Circuit Design: Operational Amplifiers, Analog to Digital Convertors, Analog Computer Aided Design, Springer, 1993
[11] William F. Davis, Robert L. Vyne: *Design Techniques for Improving the HF Response of a*

Monolithic JFET Operational Amplifier, IEEE J. Solid-State Circuits, vol. SC-19, no. 6, pp. 978–985, December 1984
[12] Graeme John Cohen: *Double Balanced Microphone Amplifier*, AES preprint, no. 2106, August 1984
[13] Bruno Putzeys: *High-Performance Discrete Building Blocks for Balanced Audio Signal Processing*, AES preprint, no. 6294, October 2004

About the author

Samuel Groner was born and currently lives in Zurich, Switzerland. He has been passionate about both art and science as long as he can remember. At present he works for Weiss Engineering Ltd. in the field of analogue hardware design and freelances as classical recording engineer/producer. Besides this, he teaches several courses at a local sound engineering school (ear training, classical music production and audio measurement) and enjoys a manifold activity as pianist, singer and choirmaster. If time permits, he is found on one of the numerous Swiss hiking trails, preferably in company with one of his cameras and a few sheets of black-and-white film. He holds a MSc degree in computer science and a MA degree as Tonmeister (recording engineer/producer).

*This article originally appeared in **Linear Audio** Volume 2, September 2011. Linear Audio, a book-size printed tech audio resource, is published half-yearly by **Jan Didden**.*