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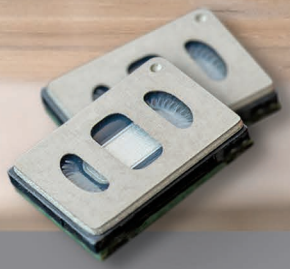

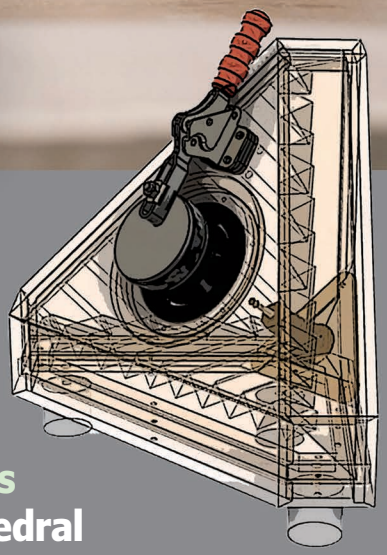

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OCTOBER 2021

Cascodes, Folded Cascodes, and Current Mirrors (Part 1)

Cascodes and Folded Cascodes

By
Morty Tarr

Cascodes, folded cascodes, and current mirrors are circuit topologies that are used to provide specific functions for an amplifier design. These topologies improve the performance of the devices, but also add complications. In this first article, the author discusses cascodes and folded cascodes.

As designers, we have many devices from which to choose. Some devices are ideally suited to certain tasks. Other tasks require performance that is difficult to achieve. While many excellent devices exist today, ideal devices do not exist, except maybe in Spice simulations.

Cascodes, folded cascodes, and current mirrors are circuit topologies that are used to provide specific functions for an amplifier design. These topologies improve the performance of the devices, but also add complications to the design.

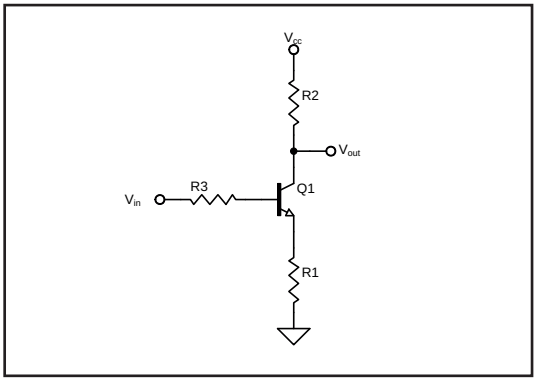

Figure 1: This schematic shows a basic NPN voltage gain stage.

Why Would We Need a Cascode?

Figure 1 shows a basic NPN voltage gain stage. Transistor Q1 is operating in common emitter mode, where the base terminal is the input, the emitter is connected to ground, and the output is taken from the collector. The gain is equal to R2/R1 (inverting) where R1 includes the emitter resistance of Q1. Since the emitter resistance of Q1 varies with current, it is important that R1 be larger than the ~26Ω/mA resistance of the emitter.

There are several factors that limit the bandwidth and linearity of the amplifier in Figure 1. In a common emitter gain stage, the capacitance between the base and the collector terminals of the transistor feeds the output signal (the collector voltage) back to the base (the input terminal). As the frequency increases, the impedance of the base-collector capacitance decreases. This contributes to the frequency response roll-off at high frequencies, especially since we like high input impedance for our gain stages. The collector-base junction capacitance varies with collector-base voltage. Higher voltages correspond to lower capacitance. This is the Miller Effect or Miller Capacitance.

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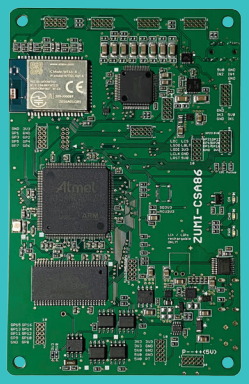

The ZUMI CS-A86 is a single board audio spectrum measurement instrument.
The CS-A86 operates autonomously to execute advanced measurement sequences, apply pass-fail criteria and log all data.
The device is aimed at implementation in automated test equipment for production and development.
The primary function is to obtain frequency response function measurements for devices under test (DUT) that require testing of signal paths especially involving filter structures or other signal conditioning elements. The built in capability to configure DUT's via serial interfaces allows a comprehensive set of quality control tests to be completed without user input.

Features

- Standalone audio spectrum measurement instrument
- 6 input channels
- 2 x 2ch analogue output
- Bluetooth A2DP source, HFP-AG, SPP
- Digital interfacing via USART, UART, SPI, I2C, SPP, GPIO

Applications

- Custom test fixtures for drivers and mics
- Automated production measurement for audio related PCBA's
- ANC filter testing
- Quality control systems with remote data reporting

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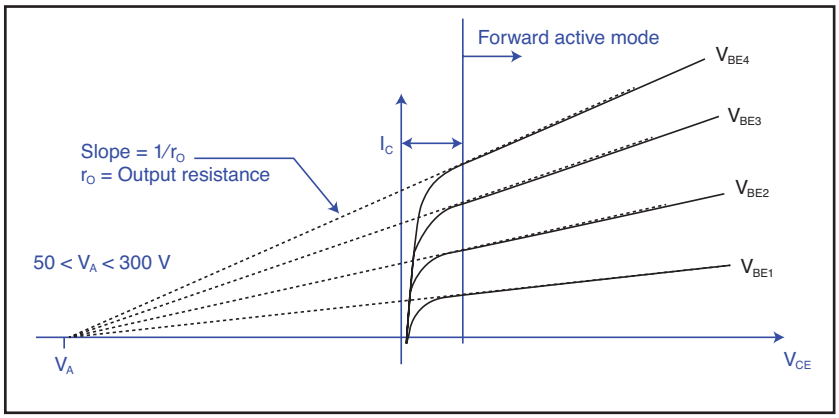


Figure 2: As the collector voltage of a transistor increases, the base width becomes smaller and the gain increases. (Original graph by Analog Devices)

Transistors also exhibit a phenomenon named after James Early, who discovered it. In a bipolar transistor, the width of the base region is modulated by the base-collector voltage. The width of the base affects the gain (β, or H_{FE}) of the device. Smaller base widths correspond to higher gain. As the collector voltage of a transistor increases, the base width becomes smaller and the gain increases. This is illustrated in **Figure 2**.

The Early Voltage (VAF in Spice) is an extrapolation of the constant V_{BE} curves to a point on the horizontal axis. Larger (more negative) values indicate a smaller Early Effect.

If the effective gain of the transistor can change with signal level, the stage will create distortion. A typical goal of 0.01% distortion is 1 part in 10,000. This can be easily exceeded by the Miller Effect and Early Effect. These effects can be mitigated via feedback, cascodes, or a combination of the two.

Cascodes are not new. Cascodes were and are used in tube circuits, particularly in high-frequency designs. In this article, we'll focus on solid-state devices.

BJT Cascodes

Let's start with a basic bipolar junction transistor (BJT) cascode. **Figure 3** shows a basic cascode circuit. Q1 is the input transistor and Q2 is the cascode transistor. The voltage gain is given by R2/R1 and is inverting just like a single transistor gain stage.

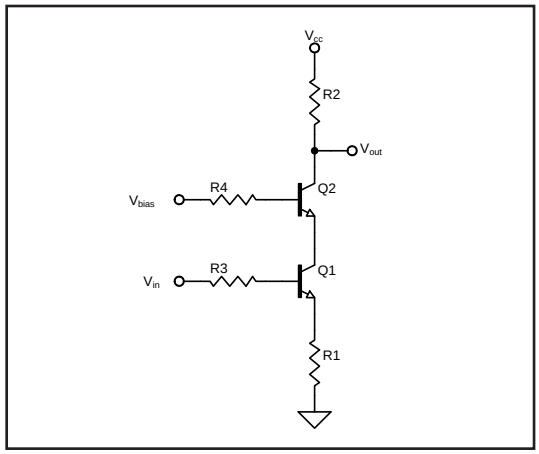


Figure 3: Here is a schematic for a basic cascode circuit.

Gain transistor Q1 is operating in common emitter mode, with the base as its input. This is where our signal is applied. Cascode transistor Q2 is operating in common base mode (the base is connected to a DC bias voltage), its input is the emitter terminal.

Here's how it works. As voltage V_{in} increases, the current in Q1 increases. Since the only place this current can go is through Q2, the current in Q2 increases. V_{BE} of both Q1 and Q2 also increases due to the higher current, so the bias at the collector of Q1 changes, but only slightly. The current in Q2 is then impressed on R2, rising current driving voltage V_{out} toward ground. As V_{in} decreases, the voltage at V_{out} increases in a similar but opposite manner. This is pretty much the same as if we didn't include Q2 and R4.

Adding Q2 provides several advantages. With Q2 in place, the collector of Q1 is held at an almost constant voltage. This minimizes the effect of the base-collector capacitance (the Miller Effect) thereby increasing the bandwidth of the gain stage. Holding Q1C at a constant voltage also minimizes Q1's Early Effect.

As an example, if we bias the base of Q1 in Figure 3 at a constant DC voltage, and increase the voltage at the base of Q2, we are increasing the collector voltage of Q1. As we do this, the gain of Q1 will increase with a corresponding effect on the collector current of Q1, even though we did not change the DC bias voltage V_{in}.

This is not an effect we want. If the gain of the stage changes with signal voltage, distortions will result. We'd like the gain of the stage to be independent of the signal, at least until we get close to clipping.

The cascode transistor Q2 prevents the collector of Q1 from moving more than a few tens of millivolts, thereby minimizing the Early Effect as well and the feedback capacitance. Note that there is no requirement for Q1 and Q2 to be the same type of device. Q1 can be a low voltage high β device, and Q2 can be a high voltage, lower β device. The β of Q2 determines only how much base current it draws through R4. With a cascode, R4 is almost always required to reduce sensitivity to oscillation. Usually 100Ω to 1kΩ is sufficient.

Devices designed for higher voltage have thicker bases, therefore, they have lower β. They also have a higher voltage at which the Early Effect becomes significant. Unfortunately, the Early Effect is not

mentioned in device datasheets. Nor is the Early voltage, which is extrapolated from the slope of the constant V_{BE} curves of the device. For an amplifier stage, a higher Early Voltage is desirable, as this will minimize the gain changes with signal level.

We set up the cascode so the gain transistor, Q1, has a nearly ideal collector-emitter voltage. This is generally in the 5V to 10V range. To do this, we set the DC voltage V_{bias} at about 10V higher than the DC component of V_{in}. The base-emitter junction of Q2 will drop about 650mV, so we will have 10V – 0.65V = 9.35V across Q1. A higher voltage across Q1 makes it more linear, but then we can run into power dissipation issues if the current is significant. Q2 can be a high voltage transistor (e.g., the KSC2690 or the KSC3503). The larger packages also allow significantly more voltage across the device without running into power dissipation limits.

Please don't try to use a cascode without base resistors. The high gain and high-frequency response are very likely to cause oscillation. Also, you should not put a decoupling capacitor at the base of Q2; that is about the same as omitting R4. In practice, I test to make R4 as small as I can without oscillation and then use double that value. Generally, R4 = 220Ω is a good starting point.

Note that in the cascode configuration, Q2 provides a current gain of just under 1.00. In other words, the current at R2 is the same as the current at R1 (less the base currents of Q1 and Q2).

Although we have illustrated these effects with NPN bipolar transistors, they apply to PNP transistors as well. MOSFETs also have many similarities. In a MOSFET, the drain-gate capacitance is the feedback capacitance, C_{rss}. The equivalent of the Early Effect is the channel length modulation. So we can't really get away from these issues with today's technology. A cascode stage with N-Channel MOSFETs is shown in **Figure 4**.

MOSFET Cascodes

A MOSFET cascode has much lower bias current as the gates of the field-effect transistors (FETs) draw orders of magnitude less current than the bases of bipolar transistors. Also, the gate-source voltage of most MOSFETs is in the 4V to 5V range, where the base-emitter voltage of a BJT is in the 600mV to 800mV range. This means that the difference between V_{bias} and V_{in} has to be 4V to 5V higher than in the BJT case.

Although it may not be obvious in the case of MOSFETs, "interesting" things happen if we let the drain voltage approach the gate voltage. These effects include significant changes in node capacitances and stored charge as V_{DG} approaches zero volts. These effects can be mitigated in switching circuits, but not so much in linear designs. So keep the drain voltage higher than the gate voltage. I find a 5V difference to be a good minimum, with 10V ideal, but often hard to achieve.

Folded Cascodes

A cascode increases the bandwidth of a gain stage and its inherent linearity. It would be good to be able to have these advantages, and also reverse

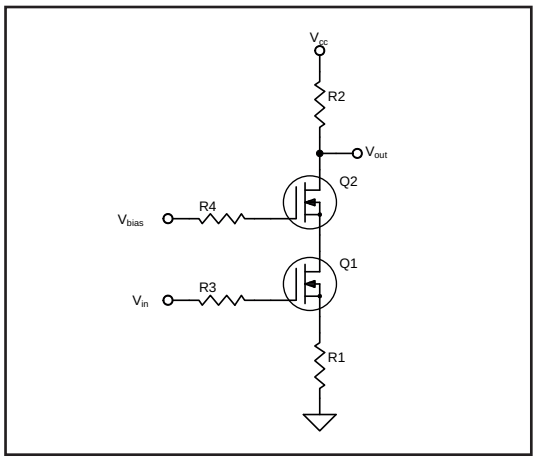


Figure 4: A cascode stage with N-Channel MOSFETs is shown.

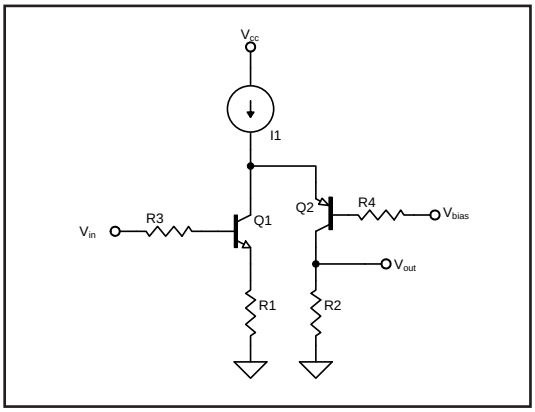


Figure 5: A BJT folded cascode is shown here.

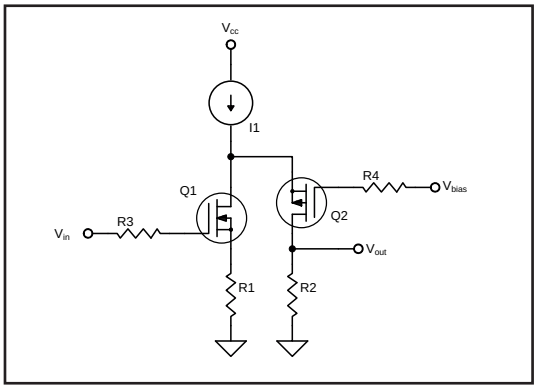


Figure 6: This is a schematic for a folded cascode that is very similar to the BJT example.

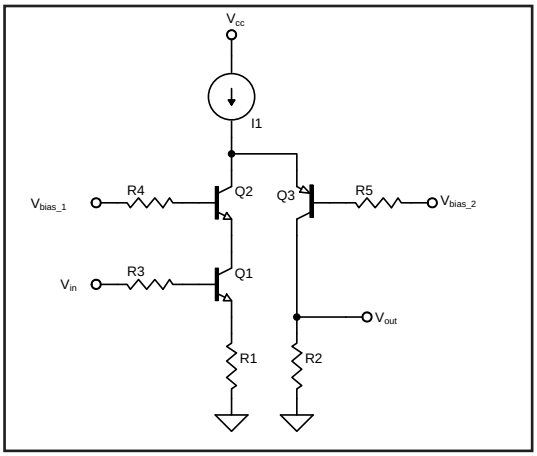


Figure 7: Here we have combined a basic cascode and a folded cascode.

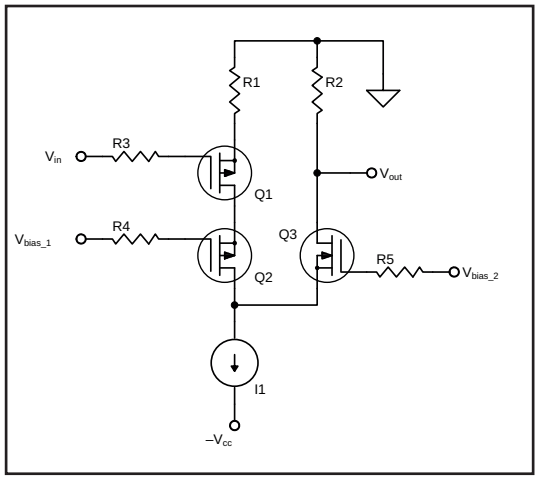


Figure 8: Input transistor Q1 is a PMOS device.

the polarity to bring the signal level back down to ground, or near ground. A folded cascode can do this. **Figure 5** shows a BJT folded cascode.

In a folded cascode, the cascode transistor is the opposite polarity of the gain transistor. In this example, Q1 is the input (an NPN transistor) and Q2 is the folded cascode (a PNP transistor). Current source I1 provides the operating current for Q1 and Q2. The current in Q2 is the current supplied by I1 less the current consumed by Q1. As V_{in} rises, the current in Q1 increases, so the current in Q2 decreases and V_{out} also decreases. The stage is inverting, just as the basic cascode.

Note that the voltage at the emitter of Q2 will change with the current in Q2. As the current in Q2 increases, the emitter voltage of Q2 will also increase as V_{BE} of Q2 increases, so if we're using a resistor for the current source, there will be small changes in the total current. For precision, I recommend a current source rather than a resistor for I1. The change in current in Q2 is equal to the change in current in Q1, so the gain of the circuit is still R2/R1 (inverting).

The emitter of Q2 is again kept at a reasonably constant voltage, so the feedback capacitance of Q1 has minimal impact on the frequency response. Here Q2 must be a different device, although it could be what we call a complementary device. In reality, NPN and PNP transistors (and N-MOS and P-MOS FETs) are not truly complementary, but that is a topic for another article.

In a basic cascode, the DC current in Q1 and Q2 is the same; in a folded cascode the DC current in Q1 and Q2 can be different. However, the AC current in Q1 and Q2 will be the same, as the current changes in Q1 are the same magnitude but opposite polarity of the current changes in Q2. Cascodes do not provide current gain. We can make a folded cascode with MOSFETs as well.

Figure 6 shows a folded cascode that is very similar to the BJT example. V_{GS} of the MOSFETs is higher than V_{BE} of the transistors, so we have to accommodate that in the biasing of the devices. Q1 is an N-Channel MOSFET and Q2 is a P-Channel MOSFET. We do not want either Q1 or Q2 to saturate as that would be really bad for linearity.

We can combine a basic cascode and a folded cascode as shown in **Figure 7**. We would do something like this if we were making an amplifier where we needed a large output swing, but we wanted to use a lower voltage device for input transistor Q1. Q2 allows Q1 to function at a lower (and almost constant) collector voltage while the output at Q3 can be a much larger voltage. Q3 would ideally be a device with a high Early Voltage

to minimize the effects of β changes. An example of these requirements is the input stage of an audio power amplifier.

The input transistor is Q1, cascoded by Q2 whose emitter sets the collector voltage for Q1. The emitter voltage of Q3 sets the collector voltage of Q2, and again the voltage at Q3's emitter will change with the current conducted by Q3.

P-Channel Cascodes

Cascodes are not limited to N-type devices; a P-Channel cascode is also possible. For the schematic in **Figure 8**, input transistor Q1 is a PMOS device. It is cascoded by Q2, also a PMOS device. The cascode is then folded by Q3, an NMOS device.

Note that in each of these examples, we could have a BJT or MOSFET cascode with a JFET input, or a BJT cascode with a MOSFET input, or any combination that makes sense for the design requirements. We are not constrained to use the same or even similar devices (as some silicon designers are constrained by integrated circuit process parameters). For example, in Figure 8, Q2 could be a PNP transistor and Q3 could be an NPN transistor.

Next Month

In Part 2 of this article series, we will discuss current mirrors and line stages built with cascodes, folded cascodes, and current mirrors.

Author's Note: I would like to thank John Curl for generously sharing his time, knowledge and insight.

About the Author

Morty Tarr has more than 30 years' experience in Electrical Engineering. Morty graduated from Cornell University in 1972 with a Bachelor of Arts in Physics, and a minor in Electrical Engineering. He continued his studies at Tufts University in Electrical Engineering.

Morty began his career at recording studios in NYC and Boston. Then he started to be interested in the design of electronic equipment and made the transition from audio to electronic design.

He has extensive experience in the fields of video, audio, test and measurement, networking, and wireless (primarily Wi-Fi and Bluetooth). More recently, from 2006 to 2015, Morty led a team at Bose responsible for advanced development for a $2 billion business. He set the direction for the group and for technology strategy spanning wireless, digital, analog, and system architecture across multiple product lines. Prior to Bose, he worked for LTX developing GHz test systems, at Octave Communications developing conference call bridges, and at Avid Technology. Prior to Avid, at Data Translation, he created the first 24-bit resolution A/D for a PC for Chromatography applications, and then led the team that developed the first Media 100 video editing system.

Morty currently has 20 patents and has spent most of his professional career developing first-in-class products. Innovative ideas and new concepts come naturally to him.

Cascodes, Folded Cascodes, and Current Mirrors (Part 2)

Current Mirrors and Line Stages

By
Morty Tarr

In Part 1 of this three-part article, Morty Tarr discussed cascodes and folded cascodes. Cascodes are useful to improve high frequency response and device linearity. Folded cascodes add the ability to move the signal level back toward ground. In Part 2, he focuses on current mirrors and line stages.

In addition to cascodes and folded cascodes, another method to improve the performance of a basic amplifier is to use a current mirror. A basic current mirror is shown in **Figure 9**. The inputs and outputs of a current mirror are currents, not voltages. In Figure 9, an input current is applied to PNP transistor Q1.

Q1 functions as a diode, so the current I_{in} is applied across the base-emitter junction of Q1. It is assumed that Q2 is matched to Q1, so Q2 has the same base emitter voltage and therefore the same collector current (however, this is not exactly true, we'll get to that later). For current mirrors, the input is a current sink, and the output is a current source.

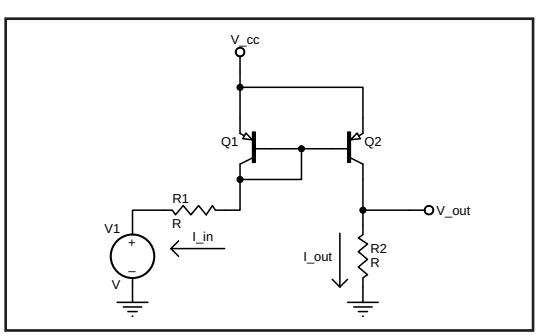


Figure 9: In this basic current mirror, the inputs and outputs are currents, not voltages. Here an input current is applied to PNP transistor Q1.

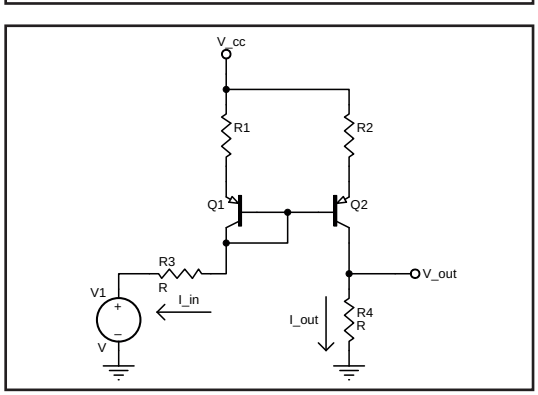


Figure 10: This schematic shows a current mirror with emitter resistors R1 and R2 added.

Current Mirrors

Current mirrors are used extensively in op-amp design, as matched transistors are easy to create and the supply voltages are limited. This is not the case with discrete designs.

So far, current mirrors seem very simple, where can it go wrong? In discrete designs, the matching of the transistors may not be ideal, and the temperature tracking will not be ideal. To minimize the impact of imperfectly matched transistors, we add emitter resistors. These resistors also serve to reduce the noise generated by the current mirror. Remember, the devices do not know they are a current mirror; they have a high impedance collector load (a current) and a small emitter resistance (approximately 26Ω at 1mA with no additional resistor). This is the formula for a very high gain.

Figure 10 shows a current mirror with emitter resistors R1 and R2 added. We also add base resistors to suppress the tendency to oscillate as shown in **Figure 11**. Figure 11 shows a current mirror adapted to discrete design. The input to the current mirror is a current, which can be applied using a voltage source and a resistor, or an active device such as a BJT (Q3), JFET (J1), or MOSFET (not shown).

Note that an active device of the proper polarity can be the input to any current mirror. In the schematics that follow, only a voltage source and resistor will be shown, but in all cases, an active device could be used instead.

The value of the emitter resistors should be as high as you can stand it. If it is a current mirror operating at 1mA, a 1KΩ resistor will drop about 1V and dissipate 1mW. If the current mirror is operating at 10mA, a 1KΩ resistor will drop about 10V, and that's going to be too much. So something between 100Ω and 500Ω

might be appropriate. Just remember, as the resistor gets smaller, the ability to minimize any mismatch decreases and the noise gain increases. As in most designs, there are many trade-offs!

The circuit in Figure 11 will not make a very good current mirror for audio. A good current mirror should have a very high output impedance since the output is a current. The output impedance of the circuit in Figure 11 is in the tens of kilohms. We can increase this with, guess what, a cascode.

Also, we want Q1 and Q2 to match, but their operating conditions do not match. Q1 has a collector-base voltage 0V and Q2 has a much greater collector-base voltage. We can add a cascode to just the output and make a Wilson Current Mirror (there are both three and four transistor versions of the Wilson Current Mirror), or we can add a cascode on both sides as shown in **Figure 12** and make a cascode current mirror.

The cascode raises the output impedance by about two orders of magnitude, greatly improving performance. It also enables Q1 and Q2 to have very similar operating conditions, which also improves performance.

Note that the current gain is less than 1.00 by a factor of four base currents (4% if Beta = 100). This would not be problem if Beta was constant (but Beta changes with collector current). Also, Q1 and Q3 are operating at a collector-base voltage of 0V, which is not a good operating point for a transistor in a linear circuit. We can add LEDs to the design to increase the collector-base voltage of Q1 and Q3.

Since the transistors draw only microamperes of base current, LEDs are a good (low noise) choice for increasing the collector-base voltage. Green LEDs drop about 1.7V each in this configuration (1.9V to 2.1V with a 5mA current).

Bipolar junction transistor (BJT) current mirrors can be made with NPN or PNP transistors. **Figure 13** shows a PNP current mirror that will reflect against the positive rail. An NPN current mirror will reflect against the negative rail. BJT current mirrors suffer from Beta changing with collector current. While the change is small, it creates second harmonic (2H) distortion. A metal-oxide semiconductor (MOS) current mirror can mitigate this problem.

There are other forms of current mirrors, but due to limited space we cannot discuss them here.

Figure 14 shows the current mirror of Figure 13 with the BJTs replaced by metal-oxide semiconductor field-effect transistors (MOSFETs). The MOSFETs contribute much lower levels of 2H distortion compared to BJTs.

When I use current mirrors in audio circuits, the best matched devices become Q1 and Q2. The match

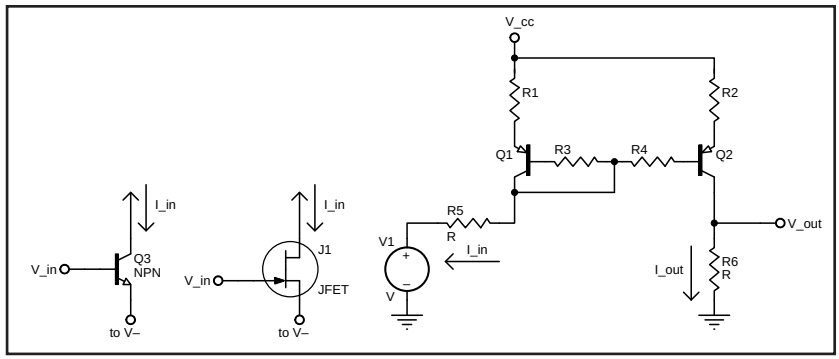


Figure 11: Base resistors have been added to suppress the tendency to oscillate and shows a current mirror adapted to discrete design.

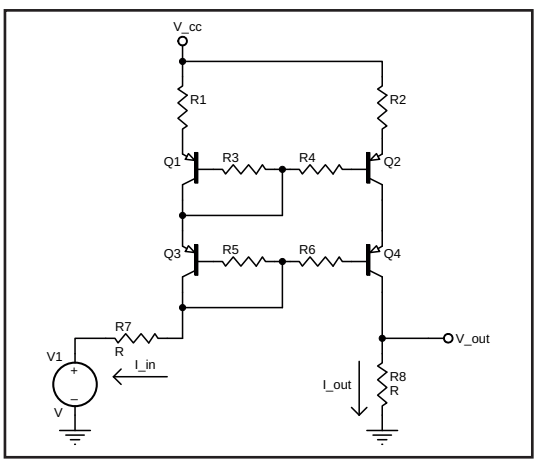


Figure 12: A cascode on both sides makes a cascode current mirror.

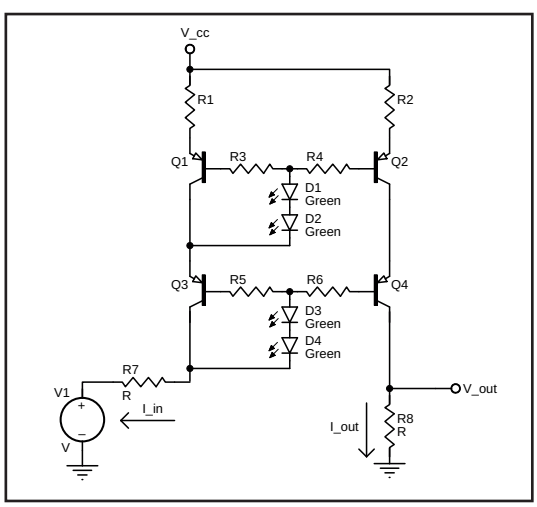


Figure 13: A PNP current mirror like the one shown here will reflect against the positive rail.

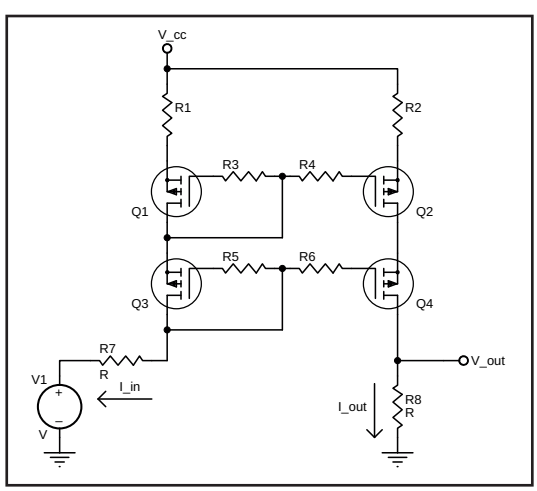


Figure 14: Here is a current mirror of Figure 13 with the BJTs replaced by MOSFETs.

requirements for Q3 and Q4 do not have to be as good. It is better to use high voltage devices, especially for Q3 and Q4 due to channel modulation effects.

There are significant differences between current mirrors and a folded cascode. Current mirrors are non-inverting and current mirrors can have gain.

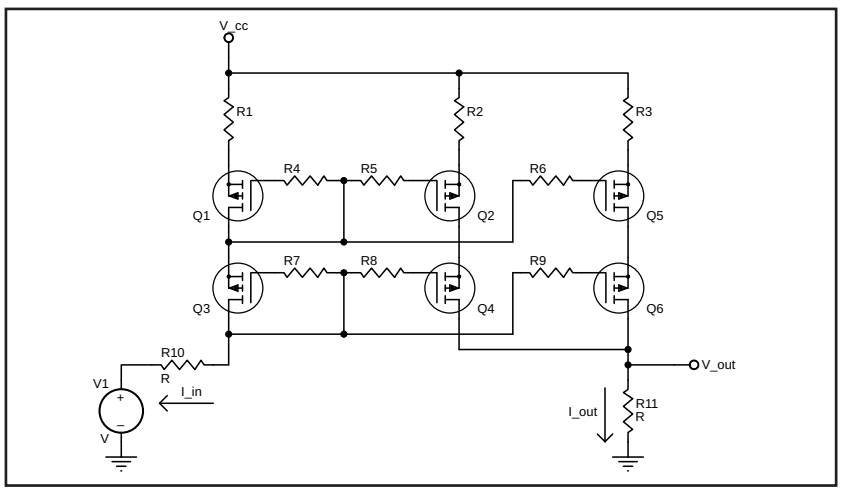


Figure 15: This is the same current mirror as shown in Figure 14, but with Q5, Q6, and R3 added.

A current mirror with gain is shown in **Figure 15**. Figure 15 shows the same current mirror as Figure 14, but with Q5, Q6, and R3 added. Q5 is matched to Q1 and Q2, Q6 is matched to Q3 and Q4. This configuration has double the output current of the circuit shown in Figure 14. The concept can be extended to include additional output mirrors so long as reasonable matching can be maintained.

Folded Cascode Line Stage

An amplifier can be built using cascodes, folded cascodes, and/or current mirrors. An example of a folded cascode line stage is shown in **Figure 16**.

Note that the current sources are biased from a string of forward-biased LEDs. I chose green LEDs, which are about 2V each. LEDs provide a low noise, low impedance bias point for the current sources. Zener diodes above 5.6V are actually avalanche diodes and contribute significant noise, which is hard to filter out.

Figure 16 shows the "block diagram" of a line stage using cascodes and folded cascodes. The block diagram is easier to follow than the actual schematic (**Figure 17**).

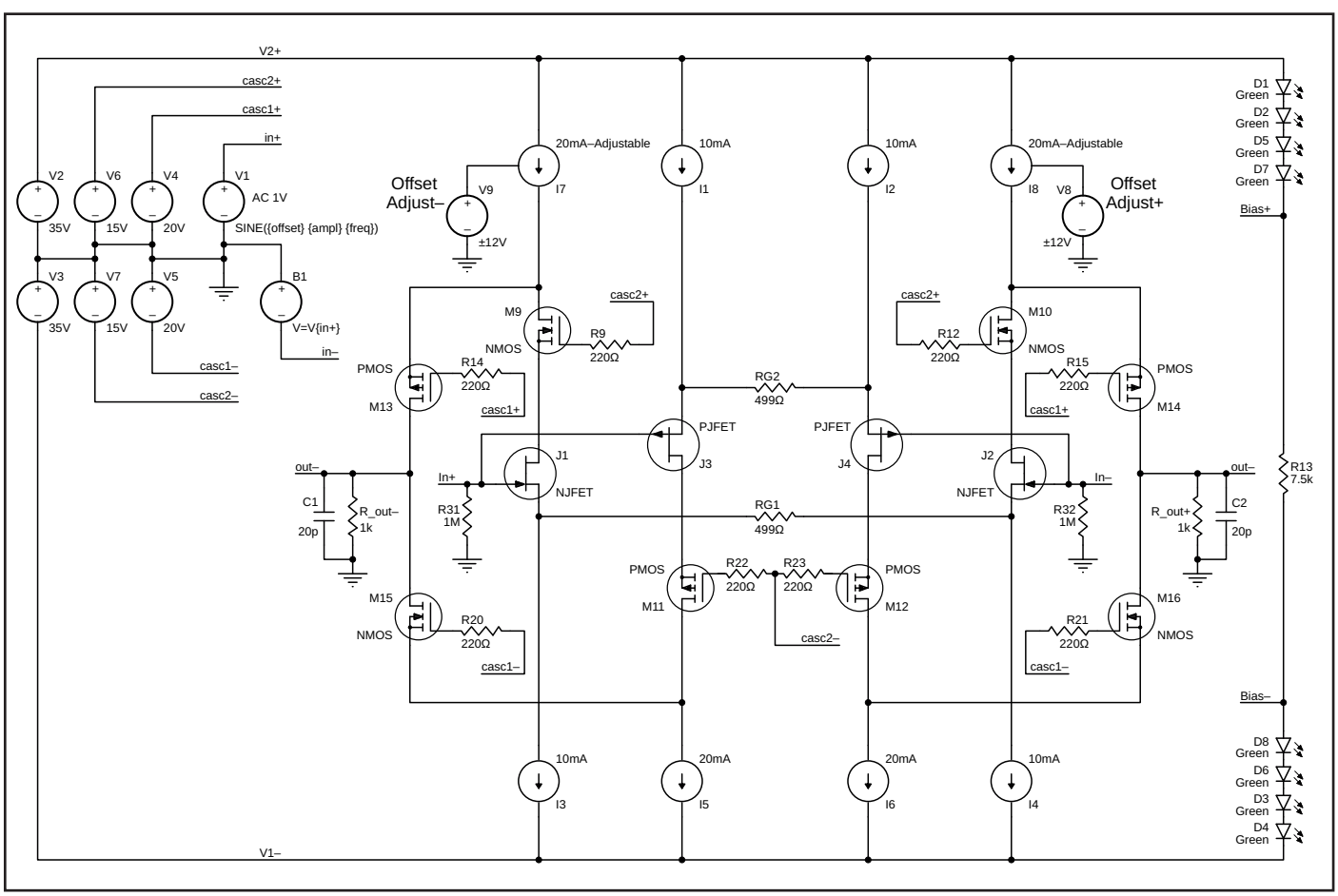


Figure 16: This block diagram shows a line stage using cascodes and folded cascodes.

A note about terminology: The gate of a device will be designated with a G suffix, the source an S suffix, and the drain a D suffix. The gate of J1 will be J1G, the source, J1S, and the drain J1D.

The input stage includes J1, J2, J3, J4, the input JFETs. J1 and J2 are biased by current sources I1 and I2. J3 and J4 are biased by I3 and I4. The current sources are set to 10mA, which is good operating current for the JFETs. The drains of the JFETs are cascoded by M9, M10, M11, and M12. The cascodes keep the JFET drain voltage constant and also limit the dissipation in the JFETs.

Since any errors in this circuit show up as distortion, we want to treat the JFETs as "nicely" as possible. J1 and J2 are Linear Systems LSK389Ds, dual, high transconductance N-Channel JFETs. J3 and J4 are LSJ74Ds. Since the JFETs are operated at 10mA, we want I(DSS) of the JFETs to be at least 12mA to account for signal currents. Since Linear Systems does not offer a dual, high-transconductance P-Channel JFET, the LSJ74s should be matched for I(DSS).

JFETs J1–J4 form a four-quadrant voltage to current converter. J1 and J2 are matched N-Channel JFETs, biased by 10mA current sources connected to J1S and J2S. If the voltage at in+ (the gate of J1) goes positive, the voltage at J1 source (J1S) rises and current flows in RG1 from J1S to J2S. Since each JEFT is biased by current sources, the current in the JFETs has to change as the current in I1 and I2 has to be constant. The current in J1 will increase with a corresponding decrease in the current in J2. This change in current is reflected in the JFET drains, J1D conducting more current and J2D conducting less current. The difference between these currents is flowing in RG1.

For example, if in+ is at +250mV and in- at -250mV, there is a 500mV difference between the

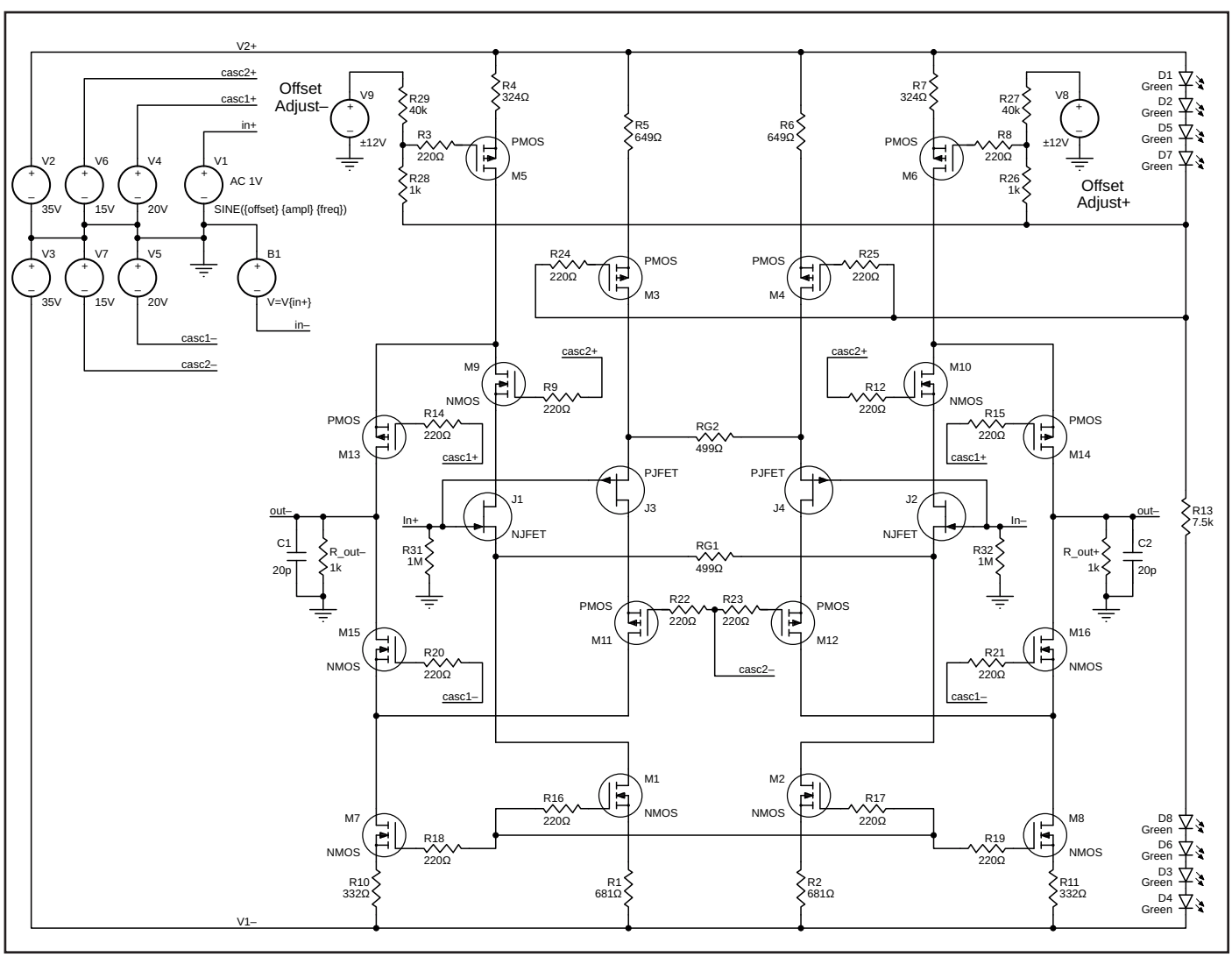


Figure 17: An actual schematic of a line stage using cascodes and folded cascodes.

Corrected Figure 17 on page 16

gates of J1 and J2. Since J1 and J2 are matched, there is a 500mV difference between J1S and J2S, causing 1mA to flow through RG1 from J1S to J2S. Therefore, the current at J1D must be 11mA and the current at J2D must be 9mA, as I1 and I2 conduct 10mA each.

The current in output cascode M13 is 20mA – 11mA = 9mA, and in M15 it is 20mA – 9mA = 11mA. The same situation happens with J3 and J4, except the polarities are reversed. This results in the current in M14 equal to 11mA and the current in M16 equal to 9mA. The 2mA difference between M13 and M14, and between M15 and M16 is impressed across the 1KΩ output resistors resulting in out+ = 2V and out- = -2V, or a 4V balanced output.

When the voltage at in- increases, the current at J2D increases and the current at J1D decreases. In a similar way, J3 and J4 (P-Channel JFETs) convert the voltage difference between in+ and in- to a current difference in J3D and J4D.

The output (folded) cascodes invert the current and apply the current difference to the output resistors (R_{out+} and R_{out-}), creating an output voltage.

The drains of all four JFETs are biased to 20mA (10mA for the JFET and 10mA for the output (folded) cascode. I5 and I6 are fixed at 20mA, while I7 and I8 are adjustable to set the output offsets to 0.00V.

Note that the change in drain-source current in the JFETs is equal and opposite to the change in drain-source current in the MOSFET (folded) cascodes. There is no current gain in a folded cascode.

This is a current mode amplifier, as the only nodes where the voltage changes significantly with input signal are the input nodes and the output nodes. It is also a transconductance amplifier as the output of the amplifier is a current. We impress this current across a resistor to create an output voltage. These are resistors R_{out+} and R_{out-}.

Capacitance at the output of this amplifier will limit the frequency response but it will not cause oscillation. Note capacitors C1 and C2, which provide frequency response compensation to eliminate peaking. These are the only capacitors in the design.

With R_{out} = 1kΩ and a load capacitance of 500pf (which is generally more than 10′ of shielded cable), the -1dB point is greater than 150kHz and the -3dB point is over 300kHz. Reasonable load capacitance should not be a problem.

For applications that need a lower output impedance, a diamond buffer, or other type of emitter or source follower can be added.

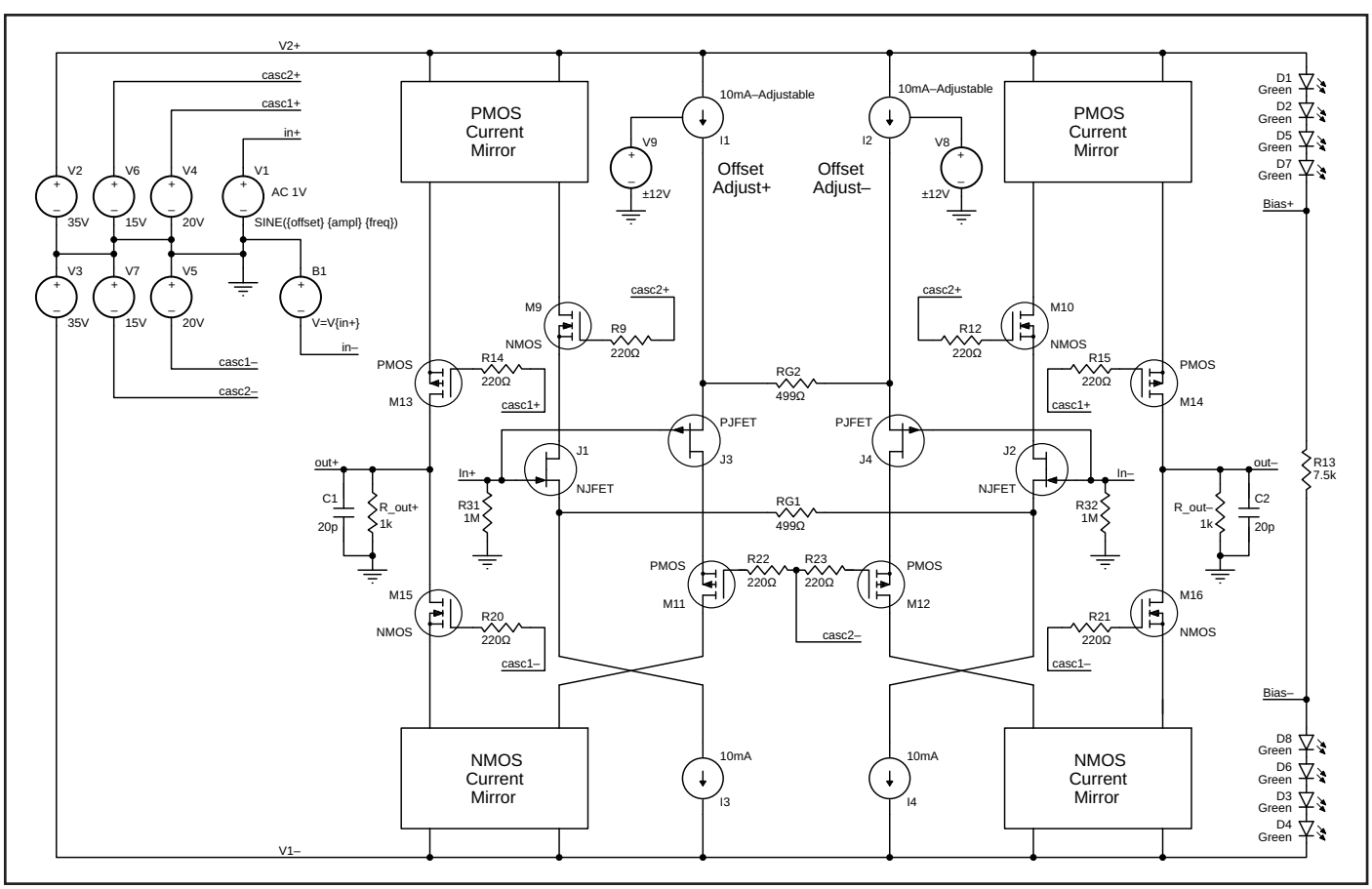


Figure 18: This is a Current Mirror Line Stage block diagram.

Here are some details based on the folded cascode line stage schematic shown in Figure 17:

- When an input voltage is present, the current in J1 and J2 becomes unbalanced as does the current in J3 and J4. Since J1 and J2 are matched, and J3 and J4 are matched, the difference between J1S and J2S is the same voltage as the difference between J3S and J4S. We now have current flowing in RG1 and RG2, The sum of the currents in RG1 and RG2 is impressed across the output resistors, R_{out+} and R_{out-}. The gain of the amplifier is approximately $2\times R_{out}/RG1$, assuming RG1 = RG2 and $R_{out+} = R_{out-}$ (0.1% matching recommended). In this case, the gain is 2×1000/250 = 8 V/V or 18dB. We could increase the gain by making the output resistors (R_{out+} and R_{out-}) larger, say, 2KΩ, or making the gain resistors (RG1 and RG2) smaller.
- With 499Ω gain resistors, an input of $1V_{PP}$ will cause 2mA to flow in each of the gain resistors, causing a ±2mA imbalance at the outputs. With 1KΩ output resistors this is ± 2V or $4V_{PP}$ at each of out+ and out- or a differential output voltage of $8V_{PP}$, which is equivalent to $5.65V_{RMS}$. This is more than enough to drive most power amplifiers to clipping. The actual gain is about 85% of the theoretical gain due to the limited transconductance of the JFETs and MOSFETs. So, instead of 8V/V, we get about 6.65V/V or 16.5dB gain. I have found that deviations from the standing DC current of ±10% maintain very low distortion levels even without global feedback.

Selecting Devices

If you were to build this circuit, use JFETs where I(DSS) is at least 12mA for our 10mA design. It is best if the pairs of JFETs are matched. Linear Systems LSK389C and LSK389D are candidates for J1 and J2. Linear Systems LSJ74C and LSJ74D are candidates for J3 and J4. In this case, the JFETS J3 and J4 should be matched for I(DSS) on the bench.

I have used Supertex (now Microchip) VP2450/VN2450 or Zetex (now Diodes, Inc.) ZVP4424/ZVN4424 for the MOSFETs. Both seem to work equally well. I am certain there are other choices that will also work well. Note that these are high voltage devices. It is best to buy about twice the required number so that they can be matched and used in matched pairs.

Current Mirror Line Stage

We could also design a Current Mirror Line Stage using a similar technique. The block diagram is shown in **Figure 18**. In the Current Mirror Line Stage, the input JFETs function the same as they do in the Cascode Line Stage. The difference is that the folded cascodes are replaced by current mirrors. We use cascode current mirrors for accuracy and low distortion. The current mirrors are non-inverting where the folded cascodes are inverting, so the out+ and out- nodes switched sides.

As in the Cascode Line Stage, the input JFETs are cascoded to limit their power dissipation and to keep their drains at a constant voltage for best performance. The output side of the current mirrors are also cascoded for the same reasons.

Here we have to trim the JFET current sources to balance the outputs at 0.00V. This is done by having one set of current sources adjustable while the other set is fixed. The adjustment can be continuous using an op-amp integrator, or manual using a potentiometer. An op-amp integrator will limit the low-frequency response, but we can set the roll-off to well below 1Hz so it has minimal effect on the audio signal path.

This amplifier, like the Cascode Line Stage is fully differential (balanced) in and out. There are four current mirrors in the Current Mirror Line Stage schematic (**Figure 19**), a P-Channel Current Mirror for each of out+ and out-, and an N-Channel Current Mirror for each of out+ and out-.

Here again, the input JFETs act as voltage to current converters. The JFET drain currents are loaded by the current mirrors, which reflect the current toward the opposite rail. A P-Channel and N-Channel Current Mirror are combined through cascode transistors to create an output current. The cascode transistors stabilize the voltage at the output of the current mirrors, improving the linearity. The current differences are impressed across the output resistor to create an output voltage.

To control the offset, we have to adjust the current sources. The N-Channel current sources are fixed

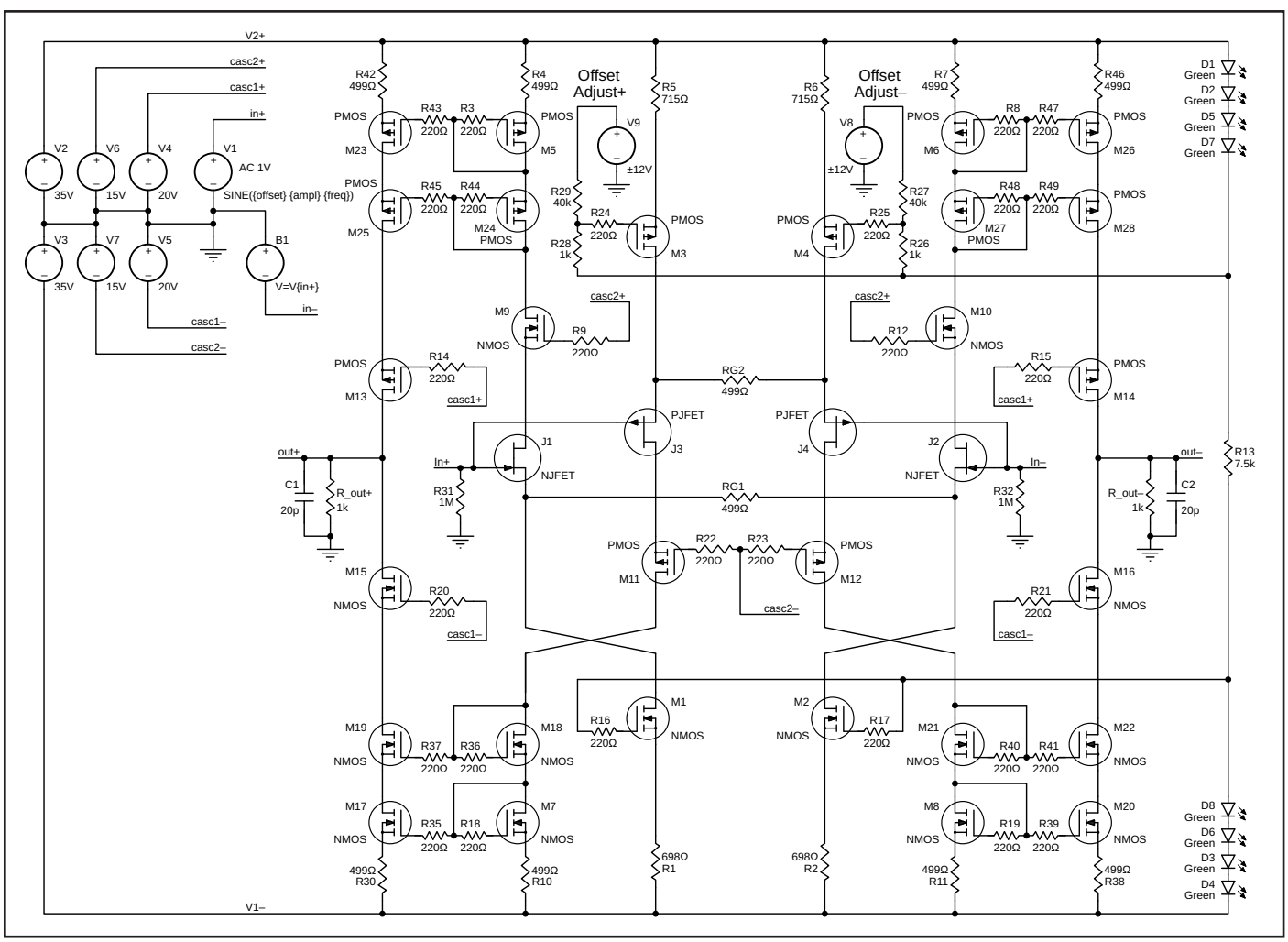


Figure 19: There are four current mirrors shown in the Current Mirror Line Stage schematic.

(M1 and M2), and the P-Channel current sources are adjustable. The adjustment can be made via a potentiometer or an op-amp configured as a non-inverting integrator.

Each has its own advantages, the op-amp continuously trims the offset to 0.000 V, but gives the amplifier a low-frequency roll-off (below 1Hz). The potentiometer setting cannot be adjusted continuously, so there will be a small residual offset at the output, but no low-frequency roll-off.

The resistor values for the current sources in Figure 17 and Figure 19 are dependent on the V(GS) of the MOSFET devices used. These values may have to be modified if different devices are used.

Observations Thus Far

For both of these line stages, I have measured distortion levels of better than -90dB (0.0032%) with $2V_{PP}$ output, single-ended in and out. At $2V_{PP}$, there are no distortion components higher than the third harmonic (3H). At $8V_{PP}$ out, the distortion is still better than -80dB (0.01%).

My measurement system consists of an HP339A Distortion Analyzer and an HP3580A Spectrum Analyzer. Since most of my consulting work is not related to audio, I cannot justify the expense of an Audio Precision measurement system. I believe the distortion specs previously quoted would be significantly better if measured on an Audio Precision system.

Next Month

In Part 3, we will discuss some of the details involved in building these line stages including matching transistors, DC servos, and capacitance multiplier power supplies.

About the Author

Morty Tarr has more than 30 years' experience in Electrical Engineering. Morty graduated from Cornell University in 1972 with a Bachelor of Arts in Physics, and a minor in Electrical Engineering. He continued his studies at Tufts University in Electrical Engineering.

Morty began his career at recording studios in NYC and Boston. Then he became interested in the design of electronic equipment and made the transition from audio to electronic design. He has extensive experience in the fields of video, audio, test and measurement, networking, and wireless (primarily Wi-Fi and Bluetooth). More recently, from 2006 to 2015, Morty led a team at Bose responsible for advanced development for a $2 billion business. He set the direction for the group and for technology strategy spanning wireless, digital, analog, and system architecture across multiple product lines. Prior to Bose, he worked for LTX developing GHz test systems, at Octave Communications developing conference call bridges, and at Avid Technology. Prior to Avid, at Data Translation, he created the first 24-bit resolution A/D for a PC for Chromatography applications, and then led the team that developed the first Media 100 video editing system.

Morty currently has 20 patents and has spent most of his professional career developing first-in-class products. Innovative ideas and new concepts come naturally to him.

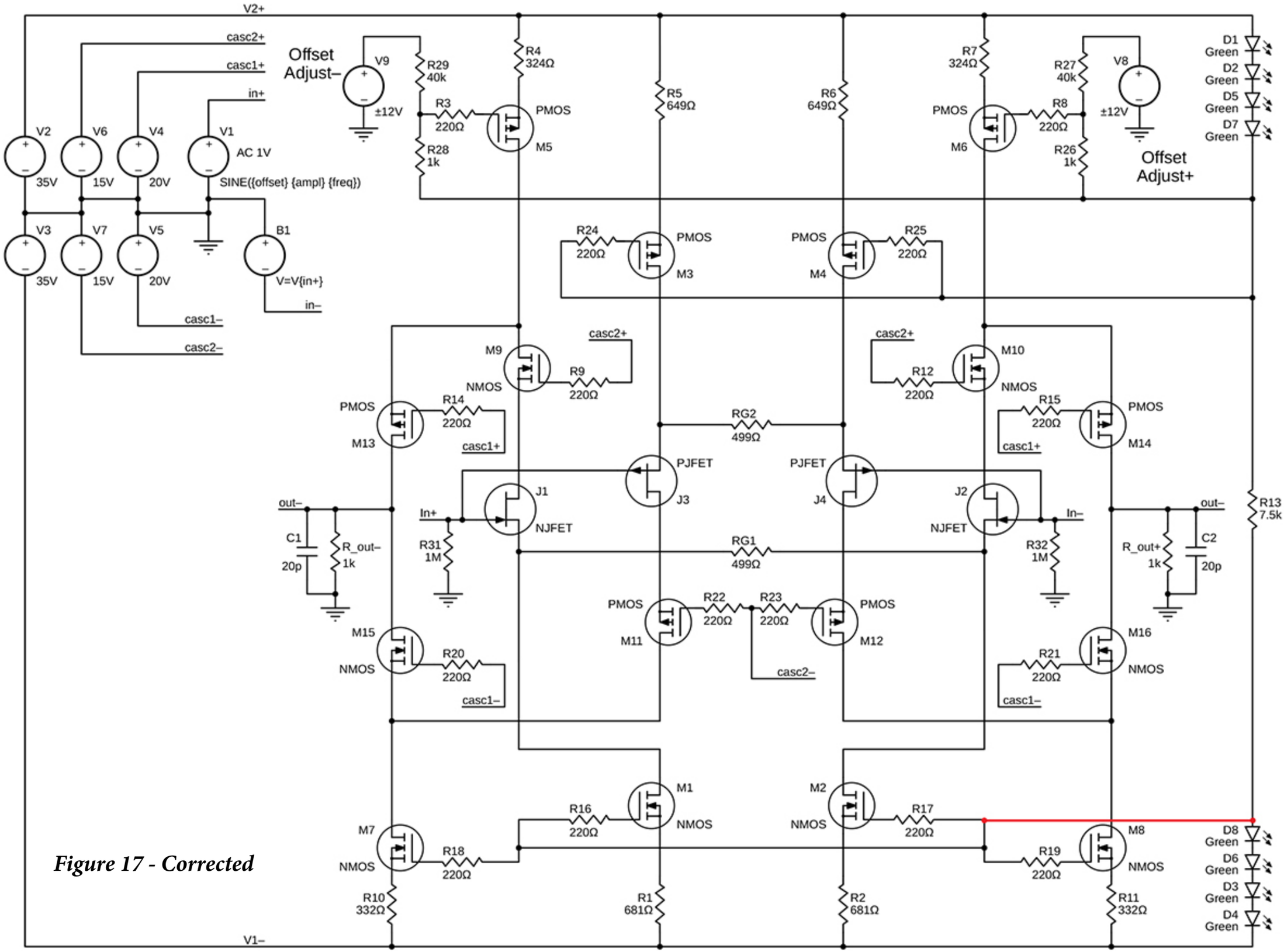


Figure 17 - Corrected

Cascodes, Folded Cascodes, and Current Mirrors (Part 3)

Using a Test Circuit

By
Morty Tarr

In the first two parts of this article series, Morty Tarr discussed the technical merits of cascodes and related circuits. As mentioned, many of these circuits benefit from matched (FET) devices. Matching is not hard, but you need to set up a simple test circuit.

Matching Components

Many circuits have improved performance when certain semiconductor components are matched. Matching involves controlling certain parameters while measuring another parameter and selecting device pairs, triples, or quads based on these measurements. For example, we can set up a MOSFET to have a V_{DS} of 10V and an I_D of 10mA; measuring V_{GS} under these conditions. This is how we could match the current mirror MOSFETs for the amplifiers.

The JFET pairs should be matched for I_{DSS} and V_{GS}. This will minimize both distortion and offset voltage. Fortunately, matching for V_{GS} at the operating point (I_D) is sufficient as V_{GS} and I_{DSS} are related for JFETs:

$$I_D = I_{DSS} \times \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

When we match for V_{GS} at I_D, we are also matching for I_{DSS}. For a current mirror, it is advantageous to match the MOSFETs in the mirror. I use a simple matching fixture that only works for MOSFETs and BJTs. It is not for JFETs, as it has limited gate voltage range.

Matching Fixtures for MOSFETs and BJTs

In **Figure 20**, Q1 and Q2 are the devices to test. It is okay to just use one test socket at a time. Q3 is for the AD711, which had an output phase shift when starting up. C1–C4 prevent oscillations (this circuit has lots of feedback), reduce noise, and stabilize the measurement.

I use this fixture with a single 20V supply, which means there will be 10V across each MOSFET. With R1 and R10 = 1kΩ, there is 10mA I_D current. I measure V_{GS} for each MOSFET and tape the devices to a sheet of paper where I can write down the measured parameter.

Note that as the device is powered up, the die temperature is changing and the measurement will be changing as well. I wait 10 seconds after power up and take the measurement. The value is still changing at that point, but it has worked for me so far.

If we standardize on a 20V power supply, current through the device under test (DUT) can be changed by changing resistors R1 and R10. The voltage across the DUT is set by the divider R3 and R4. The ratio can be changed to change the voltage across the DUT. If you do this, you will need a separate divider for the N-Channel and P-Channel portions of the test jig. For more information, read Nelson Pass' article on device matching (see Resources).

There is a simple way to match JFETs for I_{DSS}. Referring to **Figure 21**, we measure across R1 (A to B), and multiply the voltage by 10. This number is I_{DSS} in milliamps. We can adjust V1 to get 10V across the JFET (or whatever voltage we need). I have found that running JFETs at about 10V V_{DS} puts them at a good operating point for the cascode and the current mirror amplifiers.

In general, a 3-1/2 or 4-1/2 digit digital voltmeter (DVM) will work to make these measurements. Either way, you will see the measurement drift as the die heats up.

We are looking to match devices, so any DVM can be used (calibration is not important), so long as its input capacitance does not make the circuit oscillate. Our goal is to use two (or three or four) devices that measure the same, or close to the same.

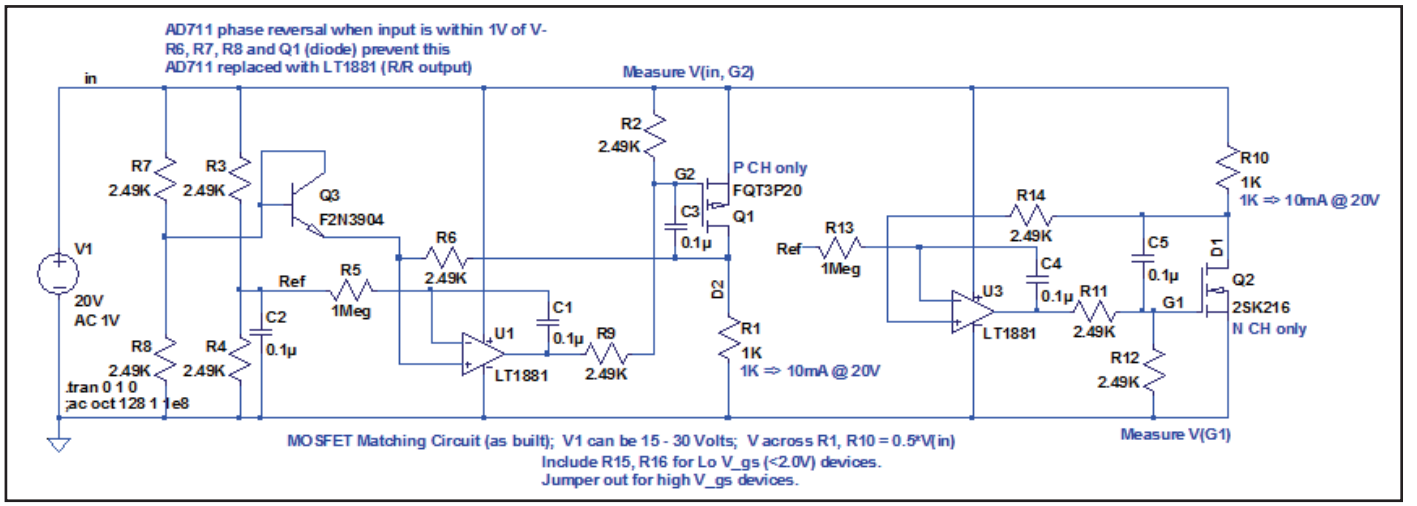


Figure 20: Q1 and Q2 are the devices to test.

I set the supply voltage so the voltage across the JFET is 10V. With a 10mA I_{DSS}, the voltage at point A will be 11V.

A Case History: the Blowtorch Line Stage

To provide a little background information, my research for the line stage designs discussed in Part 2 of this article started about 10 years ago. I discovered Dimitri Danyuk's compilation of John Curl's publications and blog posts, "Condemnation without Examination is Prejudice" online (see Resources).

After some reading, I became determined to hear a Blowtorch line stage. Since John Curl was no longer building them (and he wanted in excess of $10,000 to purchase one), my option was to make one myself. There was plenty of information in the document, and much more in the Blowtorch threads on the diyAudio website.

At some point, I had enough information to re-create the design. I also decided I wanted to meet John Curl. We actually met at CES about a year later. I was able to visit him in California and he gifted me several pairs of Toshiba 2SK389/2SJ109, which were matched to each other. I use those devices to compare the results obtained with the Linear Systems and other devices to insure that performance is not degraded.

Six years ago, I had PCBs fabricated and built my version of the Blowtorch line stage. I used IRF510 and IRF9510 MOSFETs as John did, and I was disappointed to get distortion in the -50dB range even at output levels of 2V to 4V_{PP}, indicating a problem. A quick call to John resulted in the additional information that IRF P-Channel devices were not linear enough. John had used Fairchild MOSFETs, and I needed to purchase a curve tracer.

Fairchild (now OnSemi) no longer made IRF510s and IRF9510s. But the company had the FQP3N30 and the FQP3P20, which have similar specifications. That made a significant difference, as these devices were much more linear. Now I had distortion better than -80dB.

I thought I could improve the design further (my goal was distortion products better than -90dB, which is 0.0032%). This involved converting the resistor current sources to active current sources and experimenting with different MOSFETs. Using active current sources, I was able to reduce the current in the output stage to 10mA (John's design has about 40mA in the output stage). I suspect the reason for the higher current is to minimize the change in V_{GS} with signal level,

By trying different combinations of FQP3N30 and FQP3P20 devices, I could get distortion products as good as -88dB, but I was unable to determine which characteristics resulted in this performance. Exicon lateral MOSFETs allowed me to get to about -93dB distortion products (0.0022%), but it seemed excessive to use 200W lateral MOSFETs as devices dissipating only 250mW. This is the best distortion performance I have been able to achieve so far. I have also achieved -93dB with Microchip (formerly Supertex) VP2450 and VN2450 MOSFETs, and Diodes, Inc. (formerly Zetex) ZVP4424A and ZVN4424A MOSFETs.

My measurement system is not state of the art, consisting of a HP339A analog THD+N analyzer, which has the meter output connected to an HP 3580A spectrum analyzer. The spectrum analyzer shows the distortion products present, and I look for distortion to be limited to second and third harmonics until the signal gets close to clipping. Using an Audio Precision would likely yield better

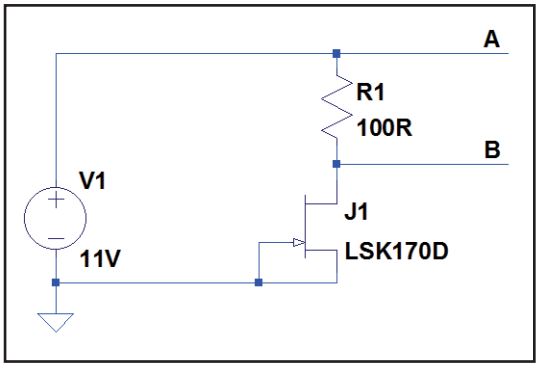


Figure 21: This is a simple way to match JFETs for I_{DSS}.

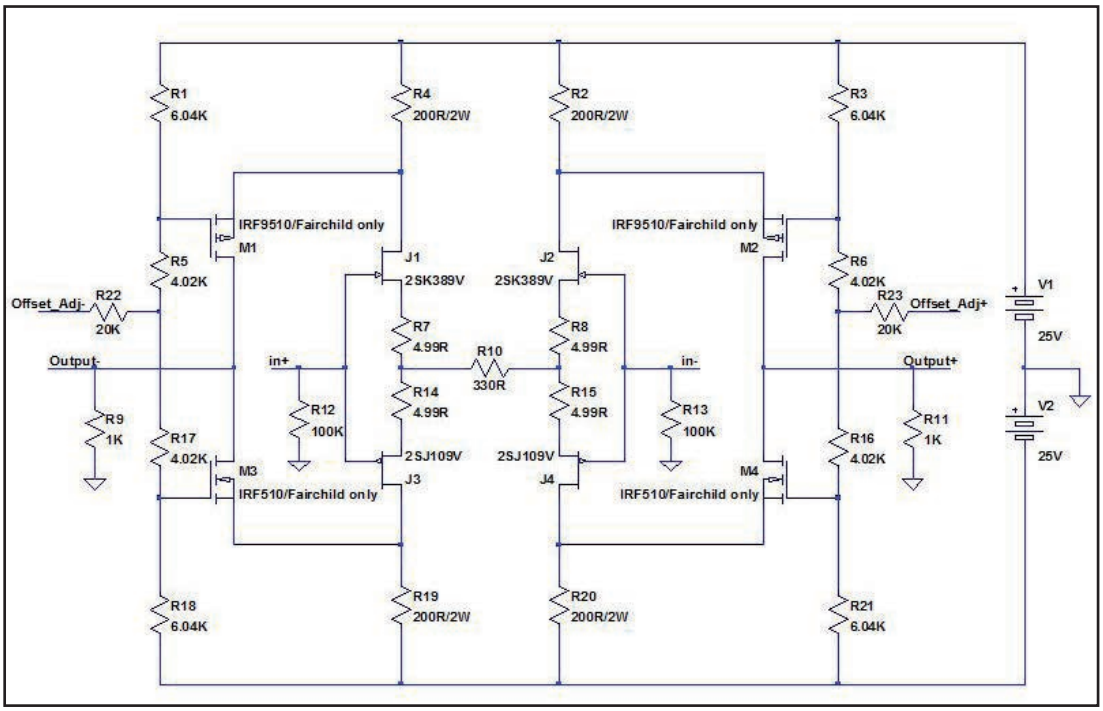


Figure 22: This is a schematic showing John Curl's circuit for the Blowtorch line stage.

results, as the fundamental could be fully removed and the noise could (optionally) be discounted. Also, it would make the measurement sequences much faster to acquire and record.

Starting with the Blowtorch

Figure 22 shows John Curl's circuit for the Blowtorch line stage. (It originally appeared in the diyAudio Blowtorch thread and on page 88 of the "Condemnation without Examination is Prejudice" article.)

John Curl invented this topology, and it is brilliant! JFETs J1 and J3 create a constant current source that is also the input buffer. Similarly, JFETs J2 and J4 create a constant current input buffer. The difference between in+ and in- is impressed across R10, the gain resistor.

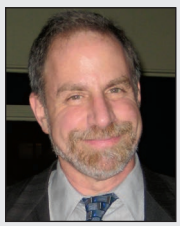
The biasing resistors, with ±25V supplies, puts the sources of the MOSFETs at about ±15V, which sets the current in the 200Ω resistors to about 50mA. This equates to 10mA for the JFETs and 40mA for the MOSFETs. Note that the input resistors, R12 and R13, can be 100kΩ or higher. An unused input should be shorted to ground (for lowest noise and offset).

My circuit design for the Blowtorch line stage substitutes current sources for the 200Ω resistors. I found I could get better distortion with lower current, so my current sources are 20mA (10mA each for the JFETs and MOSFETs).

This design is the origin of the circuits presented in Part 2 of this article series (*audioXpress*, November 2021). As it is very expensive to get sufficient quantities of JFETs to match the I_{DSS} of the N-Channel and P-Channel JFETs to each other today, I modified the design so that matching P-Channel to N-Channel devices is less critical. My design has the additional benefit of creating twice the current in the gain resistors, as the current is created between the N-Channel JFETs and also between the P-Channel JFETs vs. once in John Curl's design.

Note that if you can tolerate some additional noise, MOSFETs can be used in place of the JFET input devices that are shown in Figure 17 and Figure 19 from Part 2 of the article series. The MOSFET N-Channel and P-Channel pairs should be matched for

About the Author



Morty Tarr has more than 30 years' experience in Electrical Engineering. Morty graduated from Cornell University in 1972 with a Bachelor of Arts in Physics, and a minor in Electrical Engineering. He continued his studies at Tufts University in Electrical Engineering.

Morty began his career at recording studios in New York, NY, and Boston, MA. Then he became interested in the design of electronic equipment and made the transition from audio to electronic design. He has extensive experience in the fields of video, audio, test and measurement, networking, and wireless (primarily Wi-Fi and Bluetooth). More recently, from 2006 to 2015, Morty led a team at Bose responsible for advanced development for a $2 billion business. He set the direction for the group and for technology strategy spanning wireless, digital, analog, and system architecture across multiple product lines. Prior to Bose, he worked for LTX developing GHz test systems; at Octave Communications developing conference call bridges; and at Avid Technology. Prior to Avid, at Data Translation, he created the first 24-bit resolution A/D for a PC for Chromatography applications, and then led the team that developed the first Media 100 video editing system.

Morty currently has 20 patents and has spent most of his professional career developing first-in-class products. Innovative ideas and new concepts come naturally to him.

V_{GS} at 10mA, but the N-Channel and P-Channel devices do not have to match each other. Distortion performance is about equal to the JFET input stage (**Photo 1**).

Inverting vs. Non-Inverting Amplifier Stages

Referring to the two line stage designs in Part 2 of the article series, the Cascode Line Stage is inverting as the signal connected to in+ produces out- directly. This means that if we use the amplifier as a single-ended stage (in and out), our output will come from the side of the amplifier whose input is grounded. While this may seem like a bad idea, it is actually good in the same way a cascode is good. There is no change in the gate-drain capacitance of the JFETs whose gates are grounded, which results in marginally better performance. The difference is on the order of 1dB to 2dB better distortion, which is not necessarily audible, but is measurable. The Current Mirror Line stage is non-inverting. The advantage here is that we can choose to have gain, and/or use simpler inverting integrators for DC servos.

There are several things I'd like to point out about building these circuits, should you decide to do so.

LED Strings: I have built a number of these circuits. While assembly techniques usually call for assembling the lowest profile devices first, and moving to higher profile devices in order of their height above the PCB, I have found that this may not be the best way to assemble this design.

I install the LED bias strings first. With just the LEDs and their biasing resistors installed, I apply power to the PCB. All the LEDs should illuminate! If some do not, there may be an LED inserted backward or a defective device. I have found defective devices to be very rare.

In order to find a backward LED, use a clip lead to connect a resistor to ground (the value is not critical, I use 4.99K). Starting at the LED closest to the power supply, touch the other lead of the resistor to each LED in turn until you find one that does not illuminate. That will be the backward device. Note that the LED strings should be bypassed with capacitors. This is not shown in the schematics detailed in Part 2 of the article. I used 1µF film caps for this.

If at any time during debug and bring-up there is an LED that does not illuminate, this indicates a problem. Once the amplifier is fully assembled, it is harder to find a backward LED.

Power Dissipation: When we design circuits without global feedback, it is important to be careful with regard to device power dissipation. It is best to limit the dissipation to one-third, or at most, one-half of the device rating. This helps each device maintain a constant temperature and minimizes drift from changing device temperature. We do not want device temperature to change once it is warmed up, and especially to not change with input signal.

The reason power dissipation is more important without global feedback is that many devices change value (even slightly) with changing temperature. In a feedback amplifier, the feedback will correct for minor changes with minimal impact on performance. Without feedback, the value is not "corrected." If we think of a simple single stage amplifier, imagine the collector resistor changing value with signal level due to power dissipation changes.

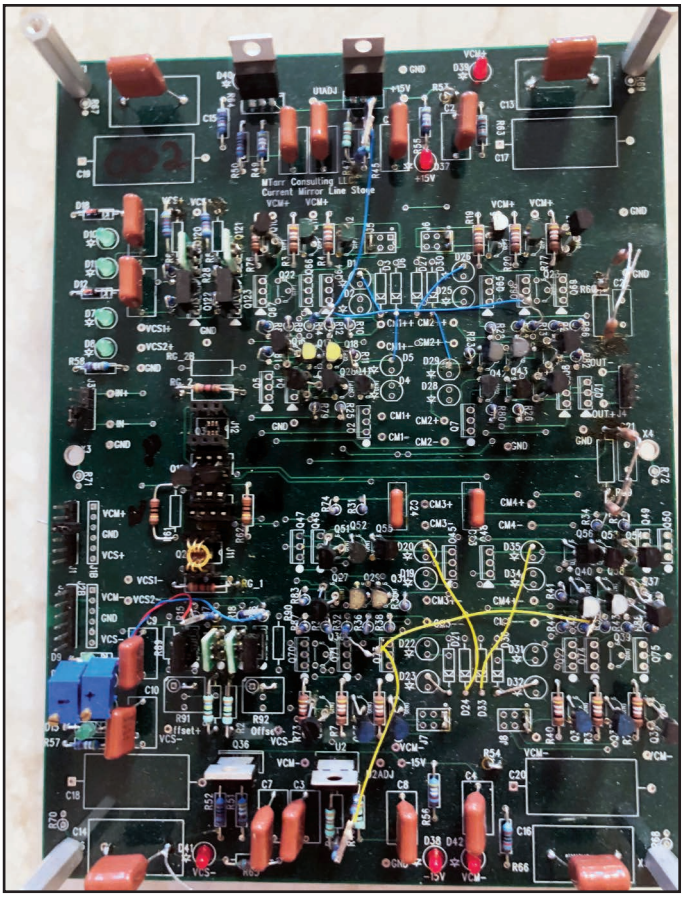


Photo 1: The current mirror line stage PCB. Three copies of this board were built, all worked very similarly. The first one has sockets for all the semiconductors; 12 sets of devices were run through this board to verify performance. The PCB shown only has sockets for the JFETs (J11 and J12, at left). Note that the MOSFETs are color coded based on matching data. These PCBs have wires and other modifications, as most prototype PCBs do. The boards were designed to accommodate three different versions of current mirror to determine the type that produces the lowest distortion without feedback.

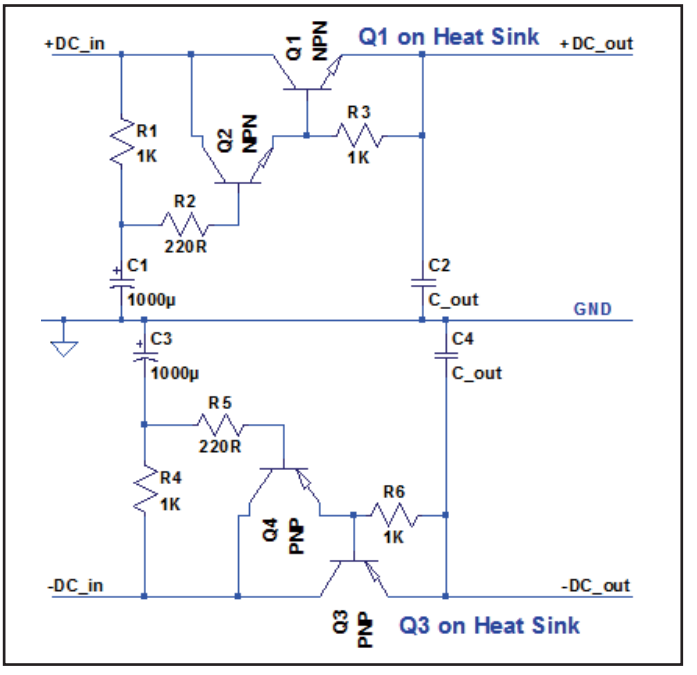


Figure 23: This schematic shows an example of a BJT capacitance multiplier.

This change can even follow the signal. As the resistor value changes, the gain changes, causing distortion. Without feedback, it is prudent to insure that device temperatures stabilize and do not change with input signal.

Power Supplies: In the article, we have not talked about power supplies. Amplifier performance can be affected by the power supplies to which it is connected.

The amplifiers presented in the article do not have a great Power Supply Rejection Ratio (PSRR) as many op-amps do. So the quality of the power supply is a significant concern with regard to amplifier performance.

Our goal for a power supply is to convert the AC line voltage to a DC voltage emulating an ideal battery; that is a DC voltage with virtually no ripple and no noise. Also, we want the power supply to be such that each amplifier is isolated from all the other amplifiers in the system.

There is not room here for a treatise on power supplies for audio, but a few recommendations are in order.

- Be mindful of the noise in the power supply output voltage (Zener diodes are noisy).
- If the output impedance of the power supply is significant, add a capacitance multiplier stage for each individual amplifier to isolate the amplifiers from each other.
- Use heatsinks for power transistors, if required.
- Use good quality capacitors to decouple the power supply at the PCB, and at points where the current draw can change with the input signal.

A capacitance multiplier can be effective for reducing power supply noise and preventing channel to channel crosstalk through the power supply. A capacitance multiplier can be made with BJTs or MOSFETs. Capacitance multipliers provide isolation when each circuit section has its own capacitance multiplier. **Figure 23** shows an example of a BJT capacitance multiplier.

A BJT-based capacitance multiplier has a voltage drop of about 1.5V. Q1 and Q3 are devices that handle the full supply current of the amplifier, and may need to be attached to heatsinks (depending on the current draw). Q2 and Q4 are small signal transistors, included to insure there is sufficient current gain.

R1 and C1 filter the input DC signal. The filtered signal is applied to the base of Q2 and then to the base of Q1 via Q2. R2 is present to ensure that the emitter followers do not oscillate. R2 should be located close to Q2. **Figure 24** shows an example of an MOS capacitance multiplier.

In the MOSFET version, we do not need Q2 and Q4 as the impedance at the MOSFET gate is very high. R2 and R5 should be located close to the gates of Q1 and Q3 to prevent oscillations. Since MOSFETs have a 3V to 5V differential from gate to source, we include voltage dividers R1/R3 and R4/R6 so the devices do not saturate. The voltage divider technique could be used with the BJT capacitance multipliers as well.

There are experts who advise that the output capacitors should not be electrolytic capacitors, but should be only high-quality film

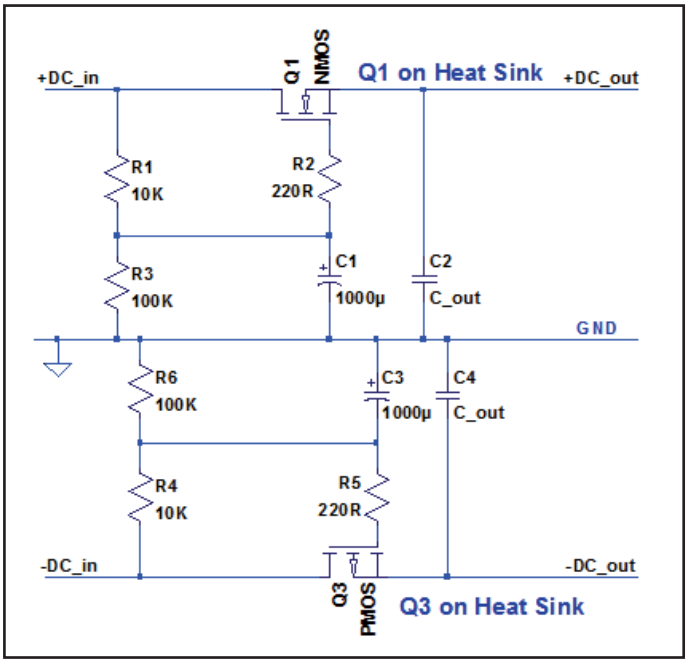


Figure 24: This schematic shows an example of an MOS capacitance multiplier.

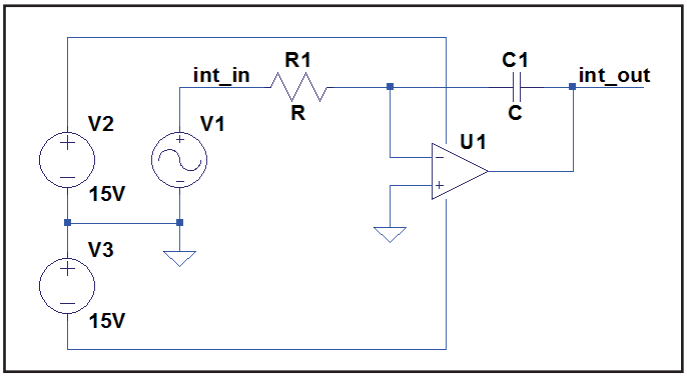


Figure 25: This circuit compares the input voltage to GND, and the op-amp output moves to keep node int_{in} at GND.

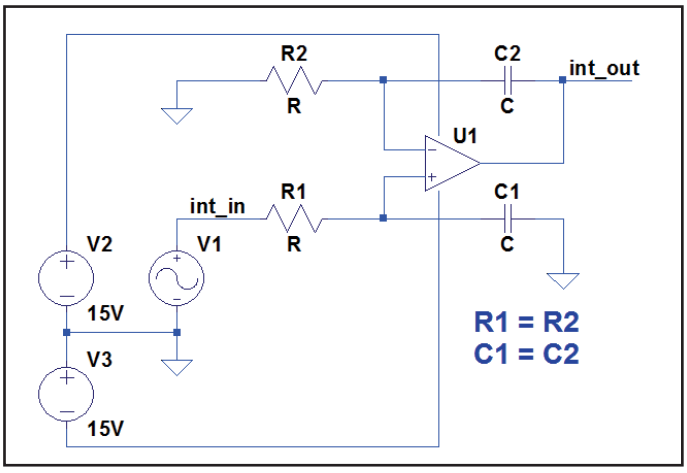


Figure 26: If our circuit is inverting, then we might need a non-inverting integrator (shown here).

capacitors. If you do this, the decoupling capacitors in the amplifier following the capacitance multiplier should be equally high-quality film capacitors.

Inverting and Non-Inverting Integrators

Integrators are important tools for finding average values. We use integrators as low-pass filters for DC servos in amplifiers. The basic idea is that the input of a servo is connected to the amplifier output. The output of the servo then represents the average or DC part of an amplifier output. By feeding this back to a suitable point in the amplifier, the servo can null the amplifier DC output. Amplifiers can be inverting or non-inverting so sometimes you need an inverting servo, at other times a non-inverting servo. Both types are discussed next. An inverting integrator is the simplest to make.

For the circuit shown in **Figure 25**, the time constant is R1 × C1 and a −3dB point of F = 1/(2 × π × R1 × C1). For R1 = 1 MΩ and C1 = 1µF, we have a time constant of 1 second and a -3dB point of 0.167Hz.

Note that the circuit shown in Figure 25 compares the input voltage to GND, and the op-amp output moves to keep the node int_{in} at GND. In this inverting integrator, int_{out} moves in the opposite direction of int_{in}.

If our circuit is inverting, then we might need a non-inverting integrator. For a non-inverting integrator (**Figure 26**), the time constants R1 × C1 and R2 × C2 must match. The time constant is equal to R1 × C1 as in the inverting case. The -3dB point is F = 1/(2 × π × R1 × C1), also the same as the inverting case. For the non-inverting integrator, int_{out} moves in the same direction as int_{in}.

In Conclusion

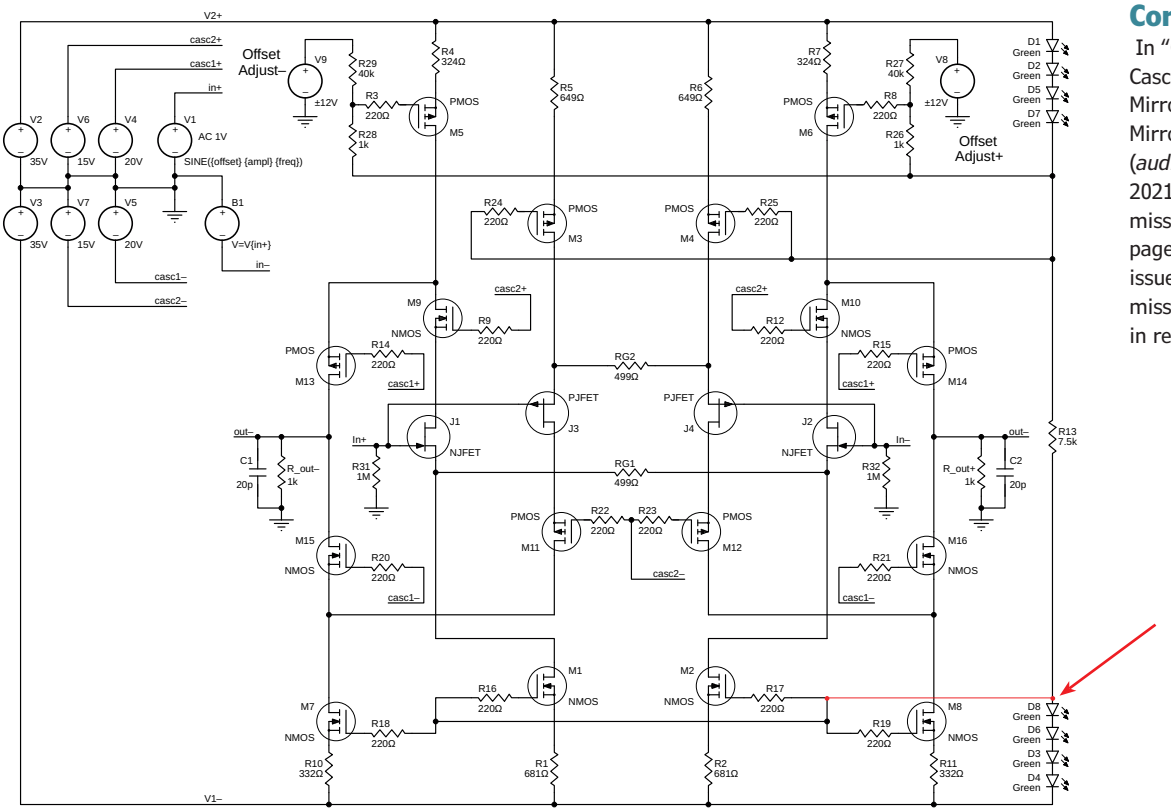
This three-part series is a brief description of some of the important aspects of amplifier design. It is by no means a comprehensive review of everything we need to know about amplifier design.

Resources

Blowtorch threads, diyAudio website:
Part 1: www.diyaudio.com/forums/solid-state/71189-john-curls-blowtorch-preamplifier.html
Part 2: www.diyaudio.com/forums/the-lounge/146693-john-curls-blowtorch-preamplifier-ii.html
Part 3: www.diyaudio.com/forums/the-lounge/318975-john-curls-blowtorch-preamplifier-iii.html

J. Curl, "Condemnation without Examination is Prejudice," May 2006, http://jockohomo.net/data/johncurl-v.0.1.pdf

N. Pass, "Matching Devices," Pass Laboratories, Inc., www.passdiy.com/project/articles/matching-devices



Correction:

In "Cascodes, Folded Cascodes, and Current Mirrors (Part 2): Current Mirrors and Line Stages (*audioXpress*, November 2021), there's a connection missing in Figure 17 on page 53 of the November issue of *audioXpress*. The missing connection is shown in red.