

FEATURES

- Balanced, transformer-like floating output
- OutSmarts® technology improves clipping into single-ended loads
- Stable driving long cables and capacitive loads
- High output: 18Vrms into 600 Ω
- Low noise: -101 dBu
- Low distortion: 0.0007% @ 1kHz
- Industry-standard pinout

APPLICATIONS

- Differential Line Drivers
- Audio Mixing Consoles
- Distribution Amplifiers
- Hi-Fi Equipment
- Audio Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- Telecommunications Systems
- Instrumentation

Description

The THAT 1606 and 1646 are a new generation of monolithic audio differential line drivers offering improved performance over conventional cross-coupled designs. Based on a high-performance, fully differential opamp and laser-trimmed thin-film resistors, both families exhibit low noise and distortion, high slew rate, and wide output swing. The parts are stable when driving difficult loads, and have short-circuit protected outputs.

Designed from the ground up in THAT's complementary dielectric isolation process, both models incorporate THAT's patented OutSmarts¹ technology. This is a dual feedback-loop design that prevents the excessive ground currents typical of cross-coupled output stages (CCOS) when clipping into single-ended loads. OutSmarts uses two individual negative-feedback loops to separately control the differential output voltage and common

mode output currents, making the designs inherently more stable and less sensitive to component tolerances than common CCOSes. As a result, THAT's topology prevents the loss of common-mode feedback that plagues common CCOS designs when clipping into single-ended loads. This avoids excessive ground currents that would otherwise upset power supplies and create additional distortion, even in adjacent channels.

The 1646 is pin-compatible with the TI DRV134 and DRV135, as well as the Analog Devices SSM2142. The 1606 offers an advanced common-mode offset voltage reduction scheme, which requires a small single capacitor instead of the two electrolytics required by the 1646 and its pin-compatible cousins. Additionally, the 1606 features differential inputs in a space-saving 16-pin QSOIP package. Both parts offer +6 dB gain.

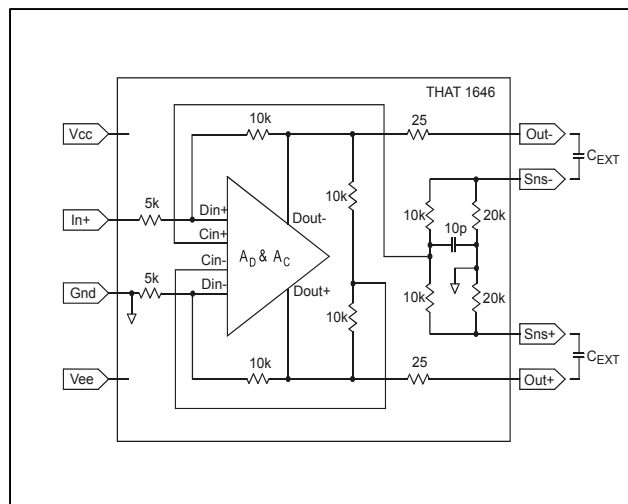


Figure 1. THAT 1646 Equivalent Circuit Diagram

Pin	1646			1606
	DIP8	SO8	SO16W	QSOIP16
1	Out-	Out-	NC	Gnd*
2	Sns-	Sns-	NC	NC
3	Gnd	Gnd	Out-	Out-
4	In	In	Sns-	Cap1
5	Vee	Vee	Gnd	Gnd
6	Vcc	Vcc	In	In-
7	Sns+	Sns+	NC	In+
8	Out+	Out+	NC	Gnd*
9	—	—	NC	Gnd*
10	—	—	NC	NC
11	—	—	Vee	Vee
12	—	—	Vcc	Vcc
13	—	—	Sns+	Cap2
14	—	—	Out+	Out+
15	—	—	NC	NC
16	—	—	NC	Gnd*

* See "Thermal Considerations" section on page 10

Table 1. THAT 1606/1646 pin assignments

1. For complete details of OutSmarts, see Hebert, Gary K., "An Improved Balanced, Floating Output Driver IC", presented at the 108th AES Convention, February 2000. Protected under US Patents numbers 4,979,218 and 6,316,970. Additional patents pending. THAT and OutSmarts are registered trademarks of THAT Corporation.

SPECIFICATIONS²

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Positive Supply Voltage (V_{CC})	+20 V	Storage Temperature (T_{ST})	-55 to +125°C
Negative Supply Voltage (V_{EE})	-20 V	Junction Temperature (T_J)	125°C
Output Short Circuit Duration	Continuous	Lead Temperature (T_{LEAD})(Soldering 60 sec)	300°C
Operating Temperature Range (T_{OP})	-40 to +85°C		

1646 Electrical Characteristics³

Parameter	Symbol	Conditions	Min.	Typ.	Max	Units
Input Impedance	Z_{IN}		4.00	5.00		k Ω
Gain	G1	$R_L=100\text{ k}\Omega$ per output Balanced	5.80	6.00	6.20	dB
		Single Ended	5.76	5.96	6.16	dB
Gain	G2	$R_L=600\ \Omega$ Balanced	5.00	5.30	5.60	dB
		Single Ended	4.96	5.26	5.56	dB
Gain Error	G1	$R_L=100\text{ k}\Omega$ per output, Balanced		0.02	0.20	dB
DC Power Supply Rejection Ratio	PSRR	$\pm 4\text{V}$ to $\pm 18\text{V}$	85	107		dB
Output Common-Mode Rejection Ratio	$CMRR_{OUT}$	$f=1\text{kHz}$, BBC Method	46	65		dB
Output Signal Balance Ratio	SBR	$f=1\text{kHz}$, BBC Method	35	54		dB
THD+N (Balanced)	$THD+N_1$	$V_O=10\text{ V}_{RMS}$, $R_L=600\ \Omega$ 20Hz-5kHz 20kHz		0.0007		%
				0.002	0.005	%
THD+N (Single Ended)	$THD+N_2$	$V_O=10\text{ V}_{RMS}$, $R_L=600\ \Omega$ 20Hz-5kHz 20kHz		0.0010		%
				0.0030	0.0090	%
Output Noise	$Onoise$	Balanced, 22Hz -20kHz		-101		dBu
Maximum Output Level	Vo_{MAX}	0.1% THD+N		27.5		dBu
Slew Rate	SR	$C_L=50\text{pF}$ /output		15		V/ μS
Small Signal Bandwidth		$C_L=50\text{pF}$ /output		10		MHz
Output Common Mode Voltage Offset	V_{OCM1}	w/o Sense capacitors	-250	± 50	250	mV
	V_{OCM2}	w/ Sense capacitors	-15	± 3.5	15	mV
Differential Output Offset	V_{OD}		-15	± 4	15	mV
Output Voltage Swing, Positive		No Load	$V_{CC}-2.9$	$V_{CC}-2.2$		V
Output Voltage Swing, Negative		No Load		$V_{EE}+2.25$	$V_{EE}+2.9$	V
Output Impedance	Z_O		40	50	60	Ω

2. All specifications are subject to change without notice.

3. Unless otherwise noted, all measurements taken with $V_S=\pm 18\text{V}$, $T=25^\circ\text{C}$, $R_L=600\ \Omega$ Balanced, $R_{SOURCE}=0\ \Omega$

1646 Electrical Characteristics (cont'd)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Maximum Capacitive Load		Stable Operation			Unlimited	μF
Quiescent Supply Current	I _S	Unloaded		4.9	5.75	mA
Output Short Circuit Current	I _{SC}	Both outputs to ground		70		mA
Power Supply Voltage Range			±4		±18	V

1606 Electrical Characteristics³

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Impedance	Z _{IN}		4.00	5.00		kΩ
Gain	G1	R _L =100 kΩ per output Balanced Single Ended	5.80 5.76	6.00 5.96	6.20 6.16	dB dB
Gain	G2	R _L = 600 Ω Balanced Single Ended	5.00 4.96	5.30 5.26	5.60 5.56	dB dB
Gain Error	G1	R _L =100 kΩ / output, Balanced		0.02	0.20	dB
DC Power Supply Rejection Ratio	PSRR	±4V to ±18V	85	107		dB
Output Common-Mode Rejection Ratio	CMRR _{OUT}	f=1kHz, BBC Method	46	65		dB
Input Common-Mode Rejection Ratio	CMRR _{IN}	f=1kHz	40	60		dB
Output Signal Balance Ratio	SBR	f=1kHz, BBC Method	35	54		dB
THD+N (Balanced)	THD+N ₁	V _O =10 V _{RMS} , R _L =600 Ω 20Hz-5kHz 20kHz		0.0007 0.002	0.005	% %
THD+N (Single Ended)	THD+N ₂	V _O =10 V _{RMS} , R _L =600 Ω 20Hz-5kHz 20kHz		0.0010 0.0060	0.0090	% %
Output Noise	Onoise	Balanced, 22Hz -20kHz		-101		dBu
Maximum Output Level	V _O MAX	0.1% THD+N		27.5		dBu
Slew Rate	SR	C _L =50pF/output		15		V/μS
Small Signal Bandwidth		C _L =50pF/output		10		MHz
Output Common Mode Voltage Offset	V _{OCM1} V _{OCM2}	w/o CM coupling capacitor w/ CM coupling capacitor	-250 -20	±50 -5	250 20	mV mV
Differential Output Offset	V _{OD}		-15	±4	15	mV
Output Voltage Swing, Positive		No Load	V _{CC} -2.9	V _{CC} -2.2		V
Output Voltage Swing, Negative		No Load		V _{EE} +2.25	V _{EE} +2.9	V
Output Impedance	Z _O		40	50	60	Ω
Maximum Capacitive Load		Stable Operation			Unlimited	μF
Quiescent Supply Current	I _S	Unloaded		4.9	5.75	mA

1606 Electrical Characteristics (cont'd)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Short Circuit Current	I_{sc}	Both outputs to ground		70		mA
Power Supply Voltage Range			± 4		± 18	V

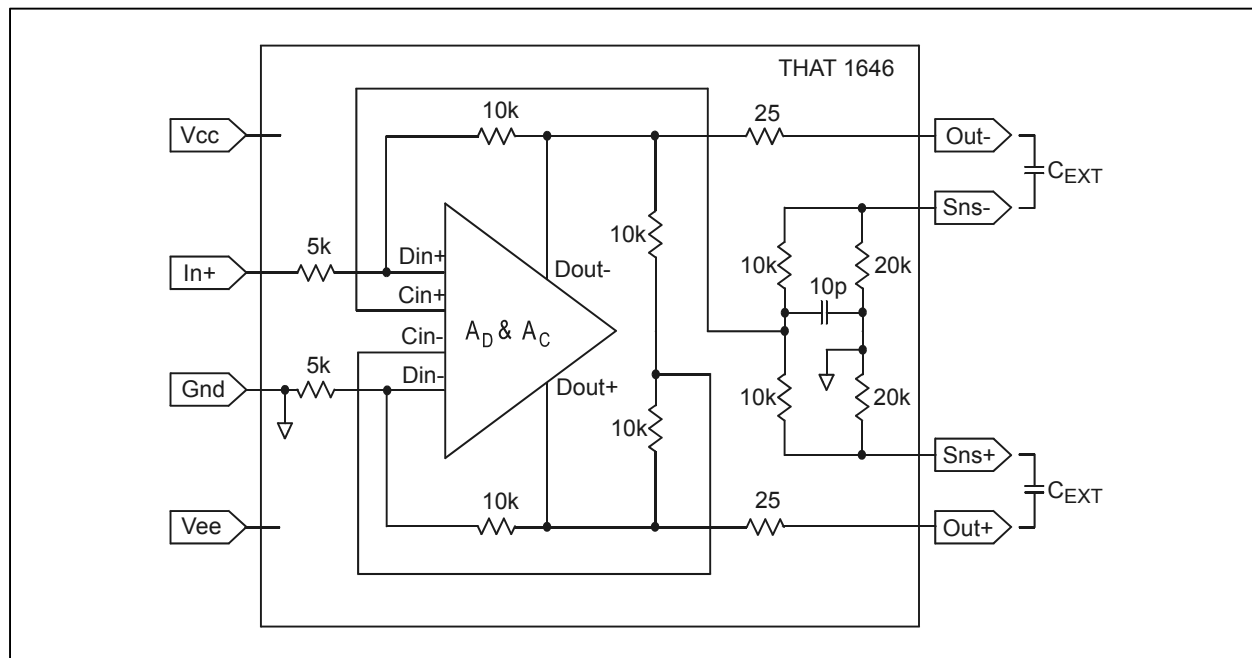


Figure 2. THAT 1646 Equivalent Circuit Diagram

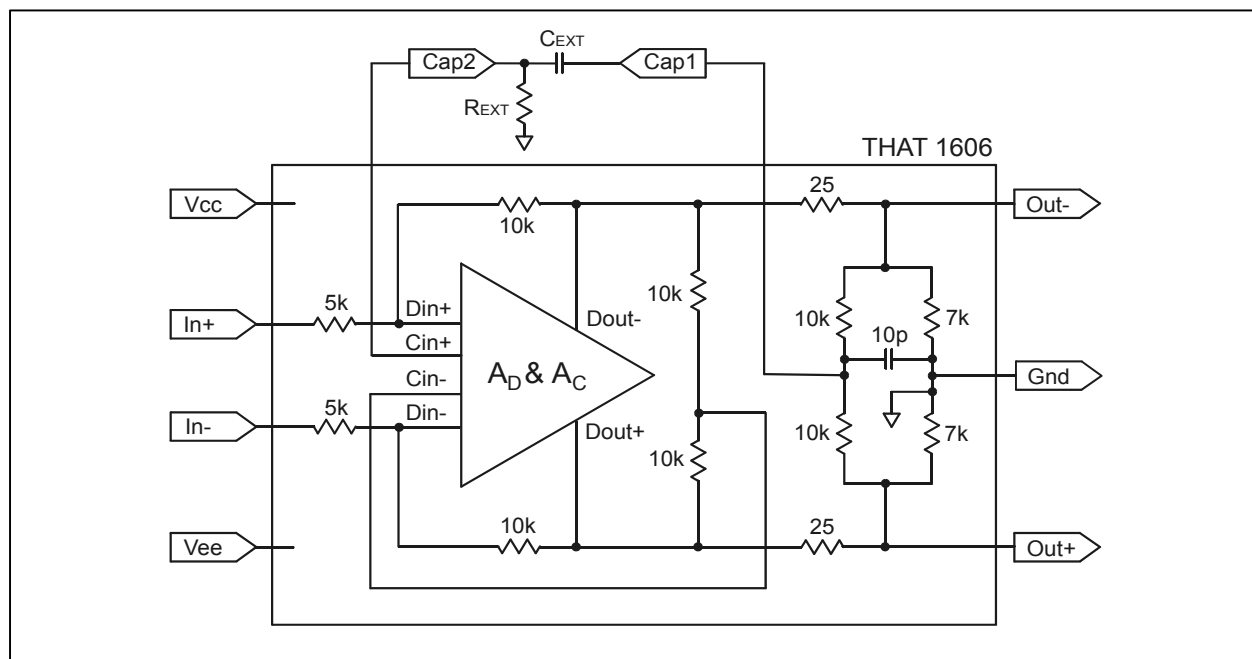


Figure 3. THAT 1606 Equivalent Circuit Diagram

Theory of Operation

OutSmarts® technology

The THAT 1606 and 1646 family employs the OutSmarts topology, a variation of circuitry originally developed by Chris Strahm at Audio Teknology Inc., (and later acquired by Audio Toys, Inc.). THAT's OutSmarts topology employs two negative-feedback loops -- one to control the differential signal, and a separate loop to control the common mode output levels.

Figures 2 and 3 show the gain core common to the 1606 and 1646. The gain core is a single amplifier that includes two differential input pairs, $C_{in+/-}$ and $D_{in+/-}$, and complementary outputs, V_{out+} and V_{out-} , related to each other by two gain expressions, $A_D(s)$ and $A_C(s)$. The first pair of differential inputs, $D_{in+/-}$, is connected to the differential feedback network between the outputs and the input signal. The second differential input pair, $C_{in+/-}$, is connected to a bridge circuit which generates an error signal used to servo the common-mode behavior of the outputs. The loop equations are then:

$$D_{OUT+} - D_{OUT-} = \Delta D_{OUT} = A_D(D_{IN+} - D_{IN-}) ,$$

where AD is the differential open-loop gain, and

$$D_{OUT+} + D_{OUT-} = \Sigma D_{OUT} = A_C(C_{IN+} - C_{IN-}) ,$$

where AC is the common-mode open-loop gain.

These equations can be solved much like standard op-amp loop equations.

For the differential case, using superposition, we can see that this results in:

$$D_{IN+} = \frac{1}{3} D_{OUT-} + \frac{2}{3} In_+ , \text{ and}$$

$$D_{IN-} = \frac{1}{3} D_{OUT+} + \frac{2}{3} In_- ,$$

Substituting and simplifying into the equation that defines differential operation yields:

$$\Delta D_{OUT} = \left[A_D \frac{-\Delta D_{OUT}}{3} + \frac{2}{3} (In_+ - In_-) \right] ,$$

Dividing through by AD (assuming that $AD \gg 3$) and simplifying yields

$$\Delta D_{OUT} = 2(In_+ - In_-) ,$$

as one would expect for a +6 dB line driver.

For the 1646, In_- is hard-wired to ground (0v), so the differential equation above simplifies to:

$$\Delta D_{OUT} = 2(In_+) ,$$

The common mode equation is more complicated in that it is dependent on the attached load, and in any event doesn't yield much insight into the device's operation. For those who are interested, a more complete discussion is given in the reference mentioned in note 1.

In op-amp analysis using negative feedback loops, the combination of negative feedback and high open-loop gain usually results in the open-loop gain "dropping out" of the equation, and the differential inputs being forced to the same potential. This is true for the core of the 1606 and 1646 ICs. If we start with that assumption, the operation of the common-mode feedback loop can be intuited as follows:

Referring again to Figures 2 and 3, the common-mode input actually senses the sum of each IC's output currents by way of two 25 Ω resistors and the bridge network⁴. The resulting error signal is amplified and then summed into both outputs, with the net effect being to force the sum of the currents to be zero, and thus the common mode output current to zero.

To see why this is important, consider what happens when the IC is loaded with a single-ended load, which shorts one or the other output to ground. Suppose Out- is grounded. In this case, the differential feedback loop increases the voltage at D_{out+} to make up for most of the signal lost to the short at Out-. The common-mode feedback loop forces the current from Out- to be equal and opposite to that from Out+. But, during peak signals which drive D_{out+} into clipping (exceeding its maximum output voltage capability), the differential loop is starved for feedback. Without the common-mode feedback, the result would be for the voltage at D_{out-} to decrease in an attempt to satisfy the differential loop's demand for feedback. This is one significant weakness of conventional cross-coupled output designs – common-mode feedback is lost when one output is clipped while the other is grounded.

With OutSmarts, however, the common mode feedback loop senses this happening because of the increase in current at Out- (compared to that at Out+), and prevents the voltage at Out- from rising out of control. This causes the OutSmarts design to more closely mimic the behavior of a true floating balanced source (such as a transformer), compared to the behavior of a conventional CCOS design.

4. The 10 pF capacitor can be ignored for the purposes of this analysis. It simply limits the maximum frequency at which the current-sensing action occurs.

Applications

1. Circuit implementations using the 1606 and 1646 are relatively straightforward. A quiet, solid ground reference, stiff voltage supplies, and adequate supply bypassing are all that are required to achieve excellent performance out of both ICs.

2. Both devices must be driven from a low-impedance source, preferably directly from opamp outputs, to maintain the specified performance.

3. Please refer to Figure 8 for a complete applications circuit.

Stability and Load Capacitance

The devices are stable into any capacitive load, and the maximum capacitance is limited only by slew rate and frequency response considerations.

For the purposes of the frequency response calculation, the line driver's 25Ω sense resistors can be lumped into a single 50Ω resistor. The correct cable capacitance to use for the balanced-signal case is the sum of the inter-conductor capacitance and the two conductor-to-shield capacitances in series. Some manufacturers only specify the inter-conductor capacitance and the capacitance of one conductor to the other while connected to the shield, and some extraction may be required.

As an example, Belden 8451 is specified as having with 34 pF/ft of inter-conductor capacitance and 67 pF/ft of conductor to "other conductor + shield capacitance". Thus, we can assume a single

conductor-to-shield capacitance of 33 pF/ft (the difference between 67 and 34) for each conductor. For balanced signals, the load capacitance across the 1646 outputs will be $34 \text{ pF/ft} + 16.5 \text{ pF/ft} = 50.5 \text{ pF/ft}$. The corner frequency of the THAT 1646 driving 500 ft of this cable (25.25 nF) will be 126 kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot 50\Omega \cdot 500 \left(34 \frac{\text{pF}}{\text{ft}} / f_t + 16.5 \frac{\text{pF}}{\text{ft}} / f_t \right)} = 126 \text{ kHz}$$

One must also consider the slew rate limitations posed by excessive cable and other capacitances. We know that

$$i = C \frac{dv}{dt}$$

and that

$$\frac{dv}{dt} = V_{Peak} 2 \cdot \pi \cdot f$$

Dennis Bohn of Rane Corporation has published work specifying some of the requirements for a balanced line driver, including a) stability into reactive loads, b) differential output voltage swing of at least ± 11 volts peak (+20dBu), and c) reliability⁵. This work suggests a reasonable rule by which to calculate the output current requirements at 20 kHz. The author concludes that the actual worst case peak level for various types of music and speech will be flat out to 5 kHz, and roll off at 6dB/octave above this frequency. Thus the peak levels at 20 kHz will be 12 dB below those at 5 kHz.

Using these, we can calculate the required slew rate and current drive. For the +26 dBu output

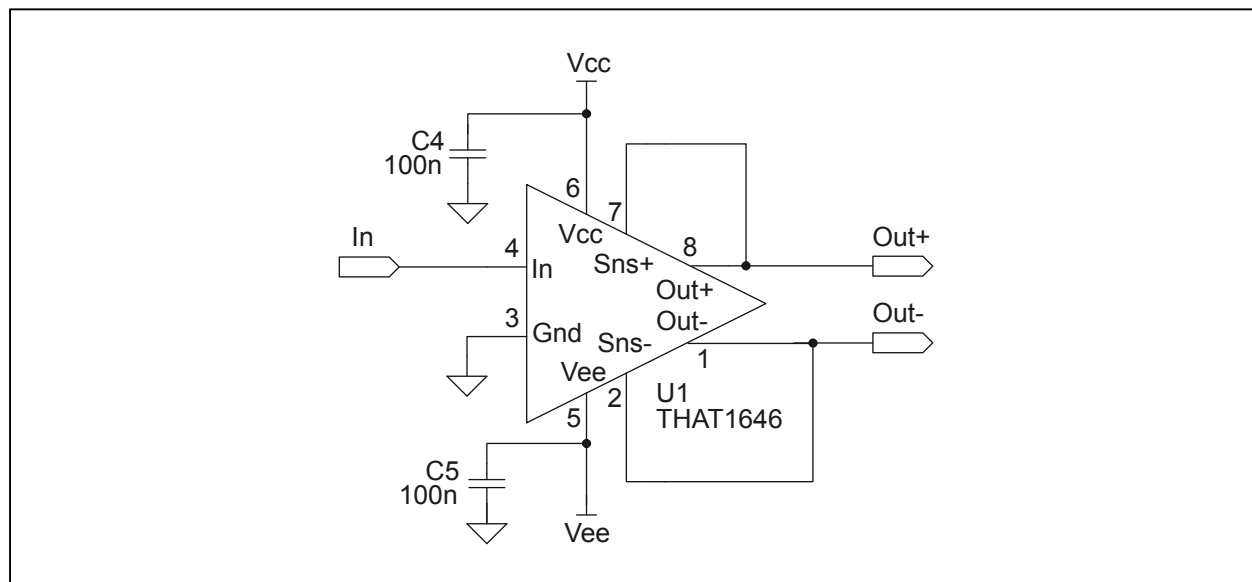


Figure 4. THAT 1646 without common-mode offset reduction

5. Dennis A. Bohn, "Practical Line-Driving Current Requirements"(Rane Note 126), Rane Corporation, 1991, revised 5/1996. Available at www.rane.com/note126.html.

levels that the 1646 is capable of, V_{Peak} is 22 V (below 5 kHz), and at 20 kHz, V_{Peak} is 5.5 V. Therefore,

$$\frac{dV}{dt} = 2\pi \cdot 5.5V \cdot 20kHz = 0.69 \frac{V}{\mu s}$$

As a consequence,

$$i = 500ft \cdot \left(34 \frac{pF}{ft} + 16.5 \frac{pF}{ft}\right) \cdot 0.69 \frac{V}{\mu s} = 17.5mA$$

Thus, driving this 25.25 nF cable requires 17.5 mA_{Peak}, which is well within the capability of the 1606 and 1646.

Gain structure

The 1606 and 1646 both provide +6 dB gain (factor of 2) between their inputs and differential outputs. This is appropriate, since with a balanced output, twice the voltage between the power supply rails is available at the output of the stage. The single-ended input of the 1646 can accept signals that swing to nearly the power supply rails without distortion, when driving into a differential (floating) load. The balanced input of the 1606 can accept signals at each input that swing to nearly one-half the power supply rails without distortion, when driving into differential loads.

Both devices, when driving single-ended loads, will clip at about half the output voltage as compared to a differential load. This is because only one of the two output signals will be available. Despite the output clipping, the input to the devices does not need to be constrained - they will work without

undue problems being overdriven at their inputs when the outputs are clipping into single-ended loads.

1646 circuits

Figure 4 shows the most basic connection for a 1646. The only external components needed are the local 100 nF bypass capacitors. These should be within 1 inch of the 1646 pins.

Output DC offset

Because the 1646's outputs are connected directly to their respective sense inputs, this circuit may produce up to 250 mV of common-mode dc offset at its outputs. As shown, the outputs are DC coupled to the output connector, so this dc will appear directly at the output of the system.

The output common-mode offset of a 1646 may be reduced by adding capacitors in the feedback loop, as shown in Figure 5. Capacitors C1 and C2 decouple the common-mode feedback loop. This changes the loop operation from servoing the common-mode output current at audio frequencies to servoing the common-mode output voltage to 0 at DC. This results in much lower common-mode output offset voltage, as indicated in the specifications section. C1 and C2 are typically high quality non-polarized electrolytic capacitors.

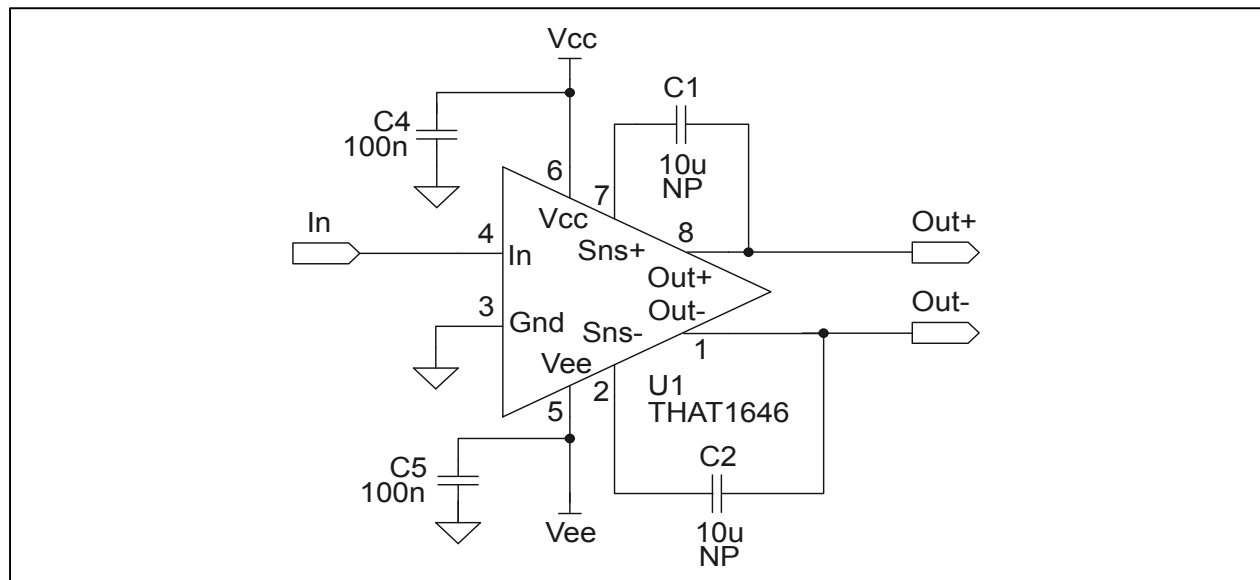


Figure 5. THAT 1646 with common-mode offset reduction

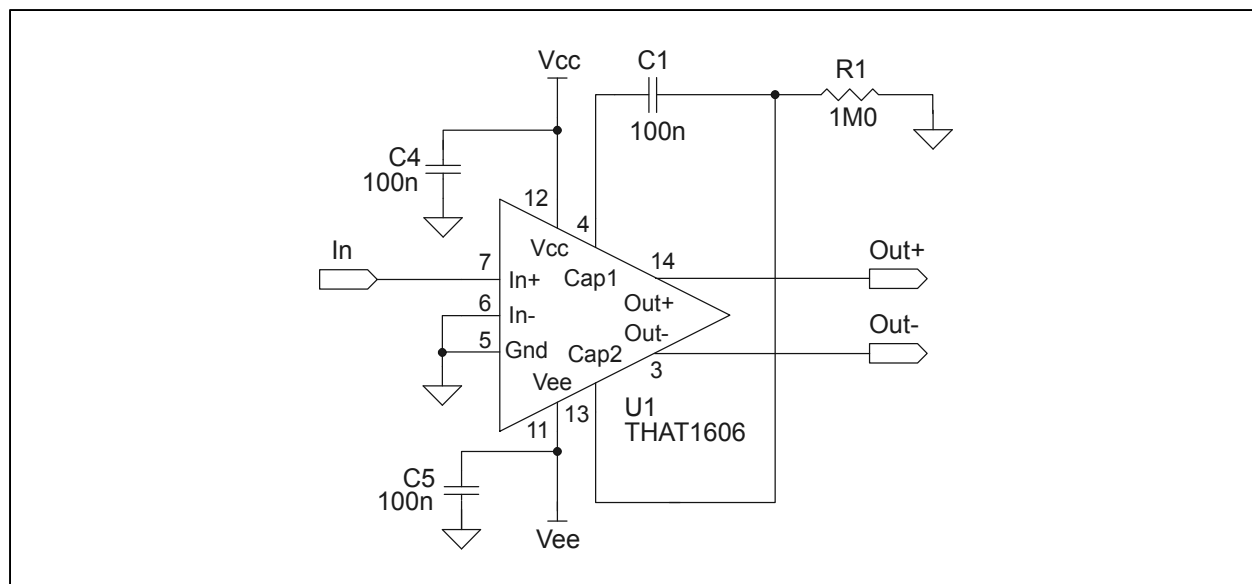


Figure 6. THAT 1606 with output common-mode offset reduction and single-ended input drive

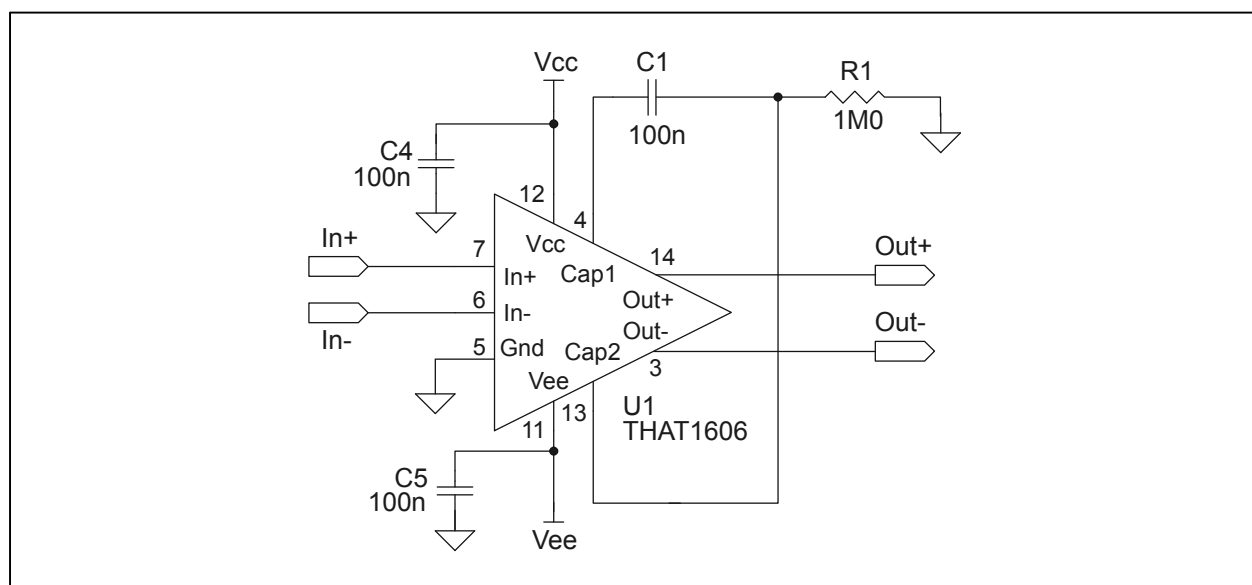


Figure 7. THAT 1606 with output common-mode offset reduction and differential input drive

1606 circuits

Figures 6 and 7 show the basic amplifier configurations for a 1606. The 1606 differs from the 1646 in two respects. First, the 1606 includes a negative-sense input pin (pin 6), so offers a differential input. This can be useful in connecting the output driver to the output of modern D/A converters, which usually present differential outputs. Second, instead of two 10 μ F capacitors, the 1606 uses an 0.1 μ F capacitor (C1) and 1 M Ω (R1) resistor to reduce common-mode dc offset. Generally, these components will cost less, and take

up less space on the circuit board than the two large capacitors required for the 1646. C1 should be a high-quality film type capacitor to minimize low-frequency distortion when driving single-ended loads.

RFI protection

These line drivers can easily drive cables hundreds of feet in length without becoming unstable, but such long cables can act as antennae which can pick up RFI and direct it into the circuit. The circuit of Figure 8 includes two 100 pF bypass capacitors (C3 and C8) and two ferrite beads, whose purpose is to redirect this RF energy to the chassis

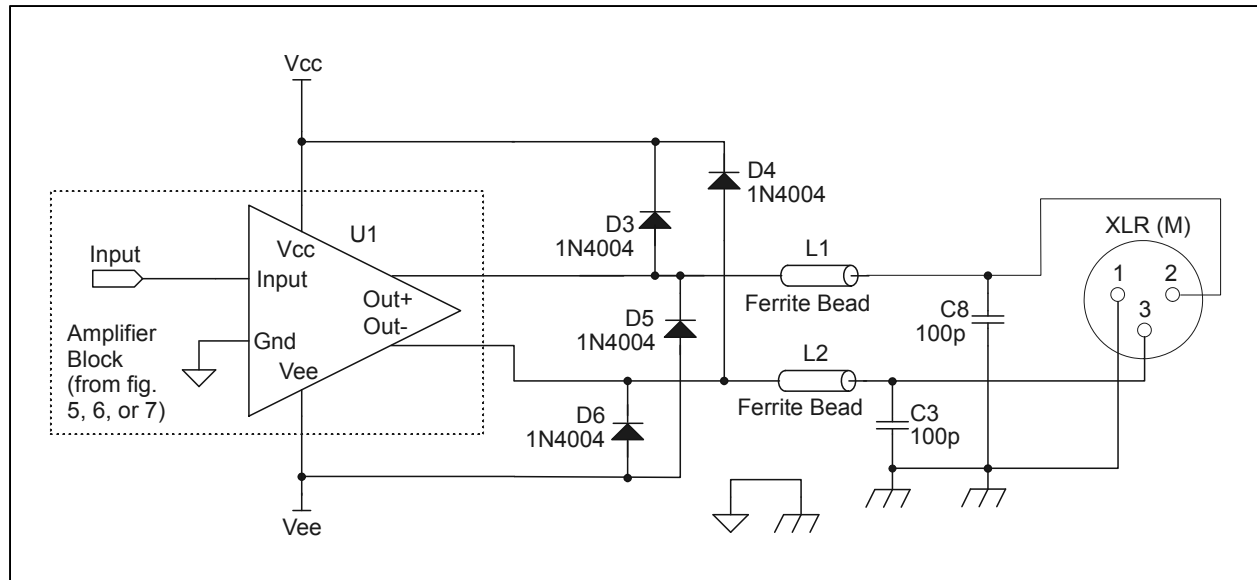


Figure 8. THAT 16x6 applications circuit with output common-mode offset protection, RFI protection, and surge protection

before it can circulate inside the product's box and couple RF into other portions of the circuit. The capacitors should be located as close as possible to the output connector and connected via a low-inductance path to chassis ground, with the ferrite beads placed very nearby. These components ensure that RFI current is directed to the chassis and not through the relatively low-impedance output of the 1606/1646. The bypass capacitors and ferrite beads will have no effect on the gain error of these line drivers at audio frequencies.

Output protection

The 1606 and 1646 each incorporate a proprietary internal protection scheme, which will suffice for many situations seen in the field. However, one might foresee having the line driver's output mistakenly plugged directly into a microphone preamplifier input that has +48V phantom power applied. When this happens, the ac coupling capacitors on the preamp's input will discharge into the low-impedance output of the 1606/1646. This can result in surge currents of over 2 amperes⁶. The amount of energy stored in these capacitors is directly proportional to the capacitor value, which is, of course, not under the 1606/1646 designer's

control. The 1606/1646's internal protection network will withstand this abuse for coupling capacitors up to about 33 μ F.

To protect against microphone preamplifiers that incorporate larger values of capacitance, a pair 1N4004 diodes from each output to the supply rails, as shown in Figure 8, is recommended. This shunts the discharge current to the power supply bypass and filter capacitors, thus protecting the output of the 1606 or 1646.

Closing thoughts

The integrated balanced line driver is one of those highly useful, cost-effective functional blocks that can provide significant improvement over discrete designs. The THAT 1646 goes a step or two further by improving over existing components. Both incorporate OutSmarts technology to tame the aberrant single-ended clipping behavior of conventional cross-coupled output stages.

For more information on these or other THAT Corporation integrated circuits, please contact us directly, or through one of our international distributors.

6. Hebert, Gary K., Thomas, Frank W., "The 48V Phantom Menace", presented at the 110th Audio Engineering Society Convention, May, 2001

Package and Soldering Information

<u>Package Characteristics</u>				
Parameter	Symbol	Conditions	Typ	Units
SO-8				
Package Style		See Fig. 9 for dimensions		8 Pin SO
Thermal Resistance	θ_{JA}	SO package soldered to board	150	°C/W
Environmental Regulation Compliance		Complies with July 21, 2011 RoHS 2 requirements		
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 °C)		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	MSL-1	
DIP-8				
Package Style		See Fig. 10 for dimensions		8 Pin DIP
Thermal Resistance	θ_{JA}	DIP package soldered to board	100	°C/W
Environmental Regulation Compliance		Complies with July 21, 2011 RoHS 2 requirements		
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 °C)		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	MSL-1	
SO-16				
Package Style		See Fig. 11 for dimensions		16 Pin SO
Thermal Resistance	θ_{JA}	SO package soldered to board	80	°C/W
Environmental Regulation Compliance		Complies with July 21, 2011 RoHS 2 requirements		
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 °C)		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	MSL-1	
QSOP-16				
Package Style		See Fig. 12 for dimensions		16 Pin QSOP
Thermal Resistance	θ_{JA}	QSOP package soldered to top-side ground plane of 1 sq in or larger	125	°C/W
Environmental Regulation Compliance		Complies with July 21, 2011 RoHS 2 requirements		
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 °C)		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	MSL-1	

The THAT1646 is available in 8-pin SO, 8-pin mini-DIP and 16-pin wide SOIC packages. The 1606 comes in a 16-pin QSOP package. Package dimensions are shown in Figures 9, 10, 11, and 12, while pinouts are given in Table 1.

Thermal Considerations

As mentioned, the 1646 is available in an 8-pin DIP, and 16-pin wide SO, and an 8-pin SO, with junction-to-ambient thermal resistances of 100°C/watt, 80°C/watt, and 150°C/watt, respectively, assuming a 2-sided PCB with no ground planes. Users of the SO-8 package should recognize driving 600 Ω loads or very long cables (several hundred feet) at high ambient temperatures (above 55°C) continuously could lead to internal die temperatures that exceed the maximum rating and result in performance degradation.

The 1606 is supplied in a 16-pin QSOP package in which pins 1, 8, 9, and 16 are fused to the die paddle to assist in conducting heat away from the die. These pins are connected to the die substrate, which is, in turn, connected to the ground pin of the device. When these pins are connected to a top-side ground plane of 1 square inch area, the junction-to-ambient thermal resistance is 125°C/watt. Internal planes on multi-layer PCBs will reduce the thermal resistance further.

Model	SO8 Pkg	DIP8 Pkg	SO16W Pkg	QSOP16 Pkg
1646	1646S08-U	1646P08-U	1646W16-U	—
1606	—	—	—	1606Q16-U

Table 2. Order Number Information

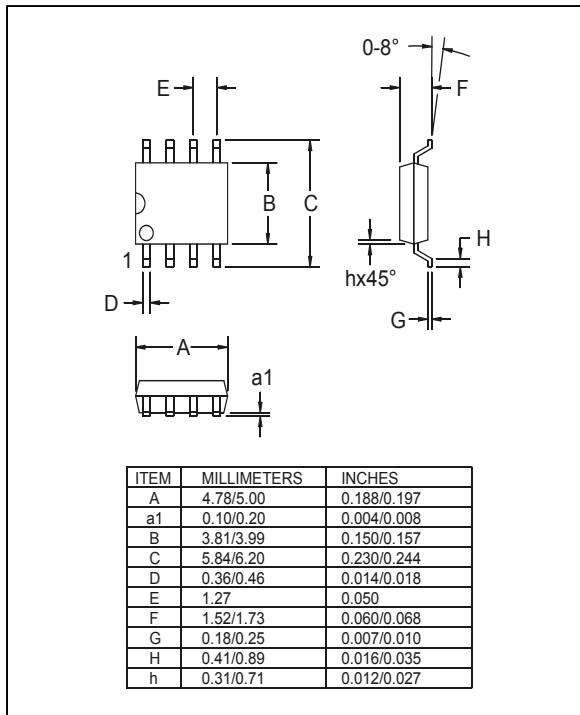


Figure 9. 8 pin SO package outline drawing

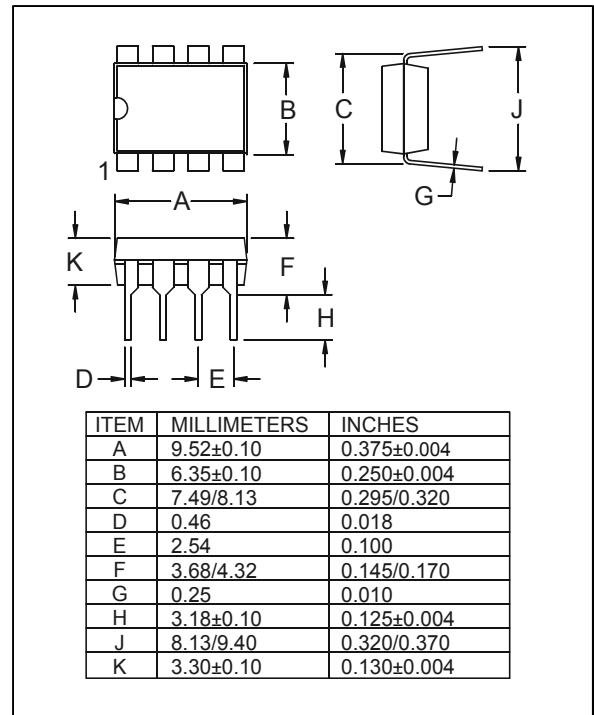


Figure 10. 8 pin DIP package outline drawing

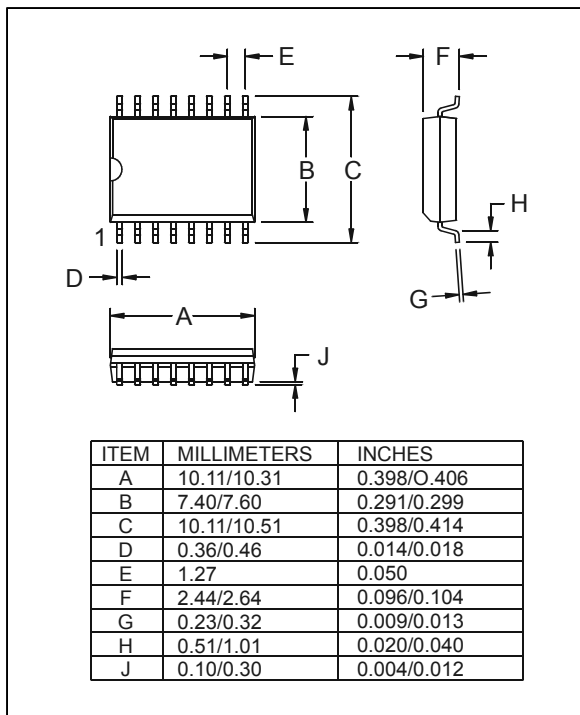


Figure 11. 16 pin wide SO package outline drawing

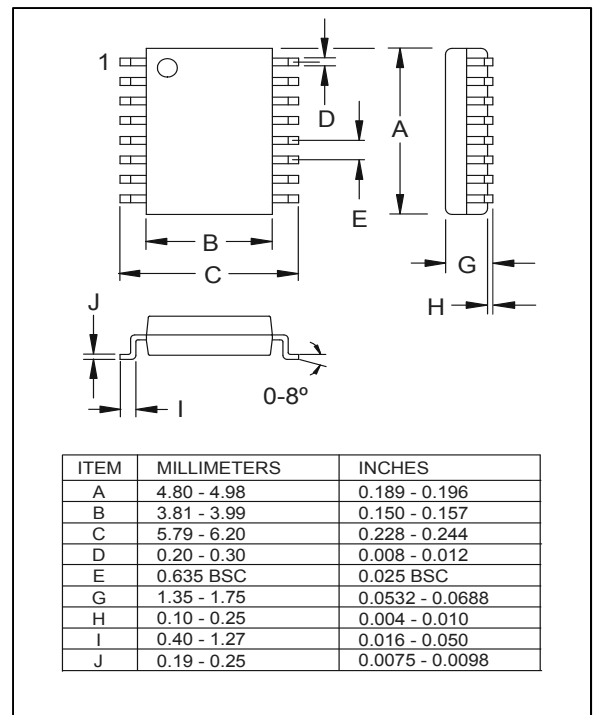


Figure 12. 16 pin QSOP package outline drawing

Revision History

Revision	ECO	Date	Changes	Page
00	—	9/26/2006	Released	—
01	—	1/12/2007	- Changed 1606 THD+N specification. - Changed the XLR orientation in Figures 4 - 9. - Changed the recommendation for common-mode offset capacitors to be high quality film type.	3 6 - 9 8
02	—	8/6/2007	Reversed the SNS+ and SNS- pins in Figure 1 and 2.	1, 4
03	—	9/24/2007	- Changed the Quiescent Supply Current specification. - Correction to the output pins in figures 4 through 9	2, 3 6 - 9
04	2323	10/16/2009	Changed Table 1. to include all the pin numbers including unused and ground pins.	1
05	2526	5/11/2011	Revised Figures 4 - 9 and accompanying text to clarify the recommended application circuits.	6 - 10
06	2765	2/19/2013	Changed the spec. for THD+N (Single-ended) @20kHz.	2, 3
07	2932	7/7/2015	Added the Package Characteristics table.	10