

Figure 19 shows the glitch associated with upper DAC bit 2. The digital input data is a computer generated, 4x oversampled, 1 kHz sinewave 100 dB below fullscale and offset to operate around upper bit 2. The oscilloscope filter is set at 30 kHz.

Figure 20 shows the glitch associated with the lower DAC bit 2 and measured in the same way.

These photographs (Figures 19 and 20) depict an artificial condition necessary to observe the minute glitches. Under natural playing conditions, these bit transitions are only exercised when the signal is 6 dB below FS or larger and the glitches are completely masked.

Figure 21 is a plot of four early production samples measured over temperature. These results were obtained with computer generated 20 bit data and measured using a Shibasoku WL12 automatic THD meter set at 30 kHz low pass and 400 Hz high pass.

## CONCLUSIONS

The major impetus for this design was the need to overcome the low level problems associated with conventional digital audio converters, while still providing excellent full scale THD and high SNR. These improvements had to be achieved without any undue cost penalty or sacrifice of user convenience. The results show that these requirements have been met. Figure 12 (110 dB signal) demonstrates, beyond doubt, that the low level problem has been eliminated. This is achieved without trimming and is typical of any part regardless of grade. It is inherent in the architecture. Figures 19 and 20 demonstrate the efficacy of the delay matching procedure, showing a worst case glitch energy of < 300 picoVoltSecs. As noted above, these small glitches are only present at large signal levels, where they will be completely masked. The full scale performance is, at least, equivalent to other high-end, digital audio DACs and for the high grade units, is equivalent to true 16 bit resolution. Figure 21 confirms the consistency of this performance over a wide temperature range. This product will, thus, allow the full potential of the digital audio medium to be enjoyed.

OEMs will undoubtedly wish to use this device with digital interpolating filters for various reasons. However, they must select very carefully to avoid compromising the system, since the limitations of certain filters were exposed during the evaluation of this device.

Oversampling, noise shaping converters will doubtlessly be pursued because potentially they offer the lowest cost solution. At present, however, certain performance compromises must be made in achieving this potential. Figure 16 demonstrates the large amount of noise associated with one of these converters while Figure 18 displays the rising THD+N versus frequency characteristic typical of noiseshaping converters.

The "Colinear" DAC represents a significant improvement over currently available, acceptably priced converters. CD player manufacturers will now be able to move much closer to theoretical performance limits and the listening public may truly benefit from the professional controversy sparked in this forum.

## ACKNOWLEDGMENTS

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## REFERENCES

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## ELECTRICAL SPECIFICATIONS

All Specifications at 25°C, and  $\pm V_{CC} = \pm 5.0V$  unless otherwise noted.

PARAMETER	CONDITIONS	PCM63P/P-J/P-K			UNITS
		MIN	TYP	MAX	
RESOLUTION				20	BITS
DYNAMIC RANGE			120		dB
INPUT					
DIGITAL INPUT					
Logic Family		TTL/CMOS Compatible			V
Logic Level:	$V_{H1}$	+2.0		+V <sub>CC</sub>	V
	$V_{L1}$	0.0		0.8	V
	$I_{H1}$			+1.0	μA
	$I_{L1}$			-50	μA
Data Format			Serial BTC <sup>(1)</sup>		
Input Clock Frequency		18.9	20		MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N <sup>(2)</sup>	Without MSB Adjustments				
PCM63P:					
f = 991Hz (0dB) <sup>(3)</sup>	f <sub>s</sub> = 352.8kHz <sup>(4)</sup>		-82	-88	dB
f = 991Hz (-20dB)	f <sub>s</sub> = 352.8kHz		-80	-74	dB
f = 991Hz (-60dB)	f <sub>s</sub> = 352.8kHz		-40	-36	dB
PCM63P-J:					
f = 991Hz (0dB)	f <sub>s</sub> = 352.8kHz		-96	-92	dB
f = 991Hz (-20dB)	f <sub>s</sub> = 352.8kHz		-82	-78	dB
f = 991Hz (-60dB)	f <sub>s</sub> = 352.8kHz		-44	-40	dB
PCM63P-K					
f = 991Hz (0dB)	f <sub>s</sub> = 352.8kHz		-100	-96	dB
f = 991Hz (-20dB)	f <sub>s</sub> = 352.8kHz		-88	-82	dB
f = 991Hz (-60dB)	f <sub>s</sub> = 352.8kHz		-48	-44	dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±2	%
Bipolar Zero Error <sup>(5)</sup>			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR <sup>(6)</sup>	20Hz to 20kHz at BPZ <sup>(7)</sup>	+115	+120		dB
POWER SUPPLY REJECTION			+88		dB
OUTPUT					
ANALOG OUTPUT					
Output Range		±1.98	±2.0	±2.04	mA
Output Impedance			670		Ω
Internal Feedback			1.5		kΩ
Settling Time	1mA Step		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
±V <sub>CC</sub> Supply Voltage		±4.75	±5.00	±5.50	V
Supply Current +I <sub>CC</sub>	+V <sub>CC</sub> = +5.0V		10	15	mA
-I <sub>CC</sub>	-V <sub>CC</sub> = -5.0V		35	45	mA
Power Dissipation	±V <sub>CC</sub> = ±5.0V		225	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		-40		+85	°C
Storage		-60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion<sub>rms</sub> + Noise<sub>rms</sub>) / Signal<sub>rms</sub>. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (8 x 44.1kHz; 8 times oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

**TABLE I (PRELIMINARY SPECIFICATIONS)**

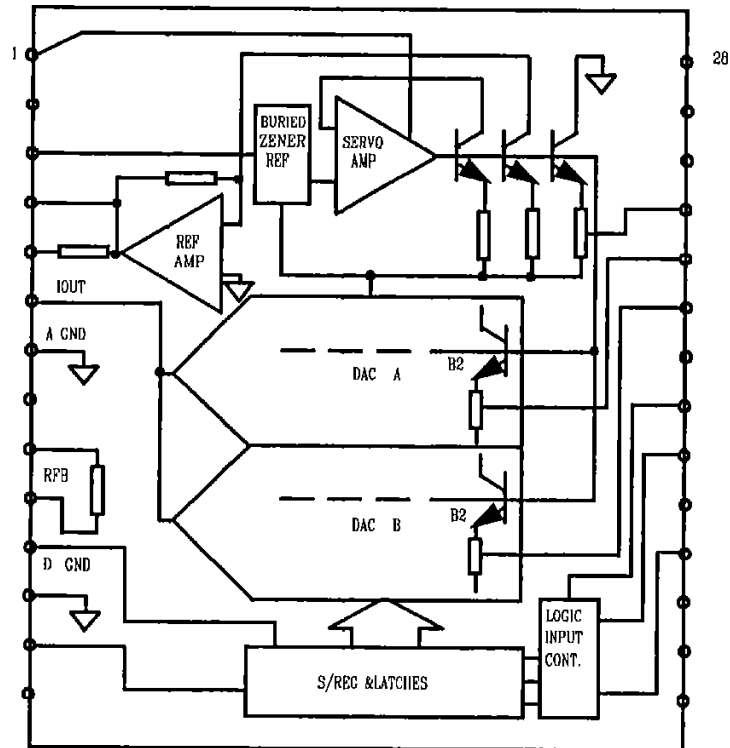


FIG. 1 COLINEAR DAC BLOCK DIAGRAM

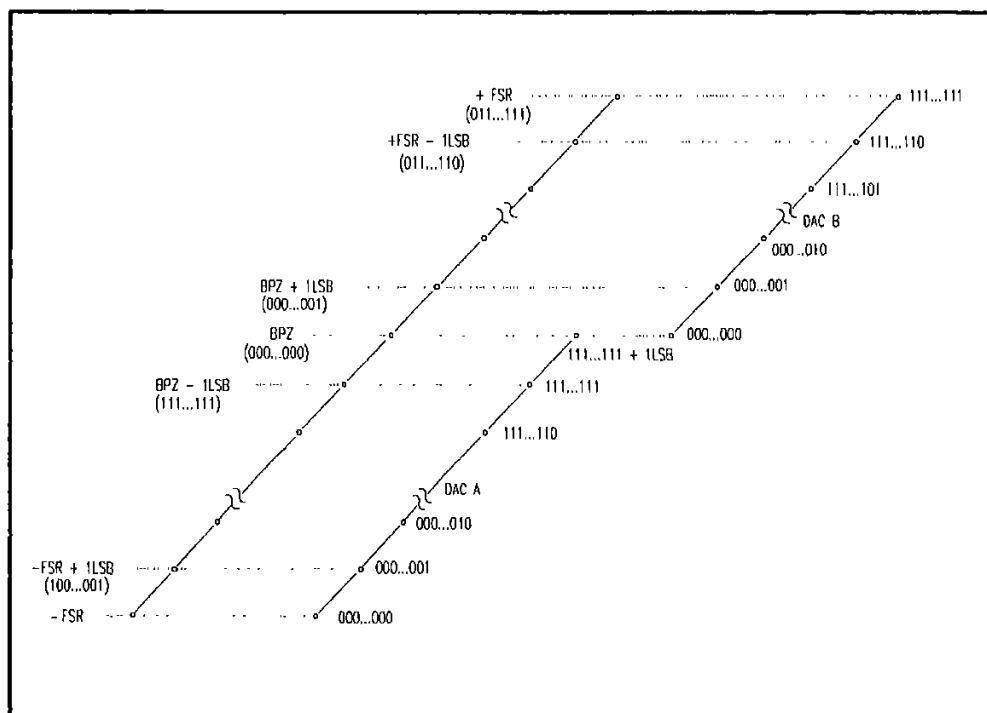


FIG. 2 BTC TO COLINEAR CONVERSION

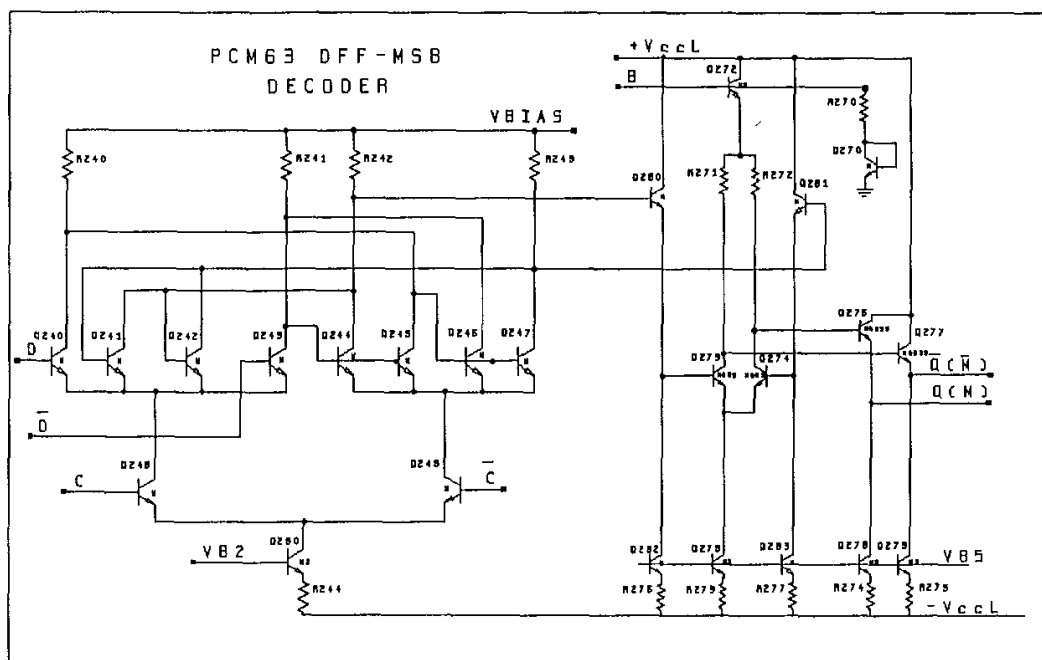


FIG. 3 MSB DECODER

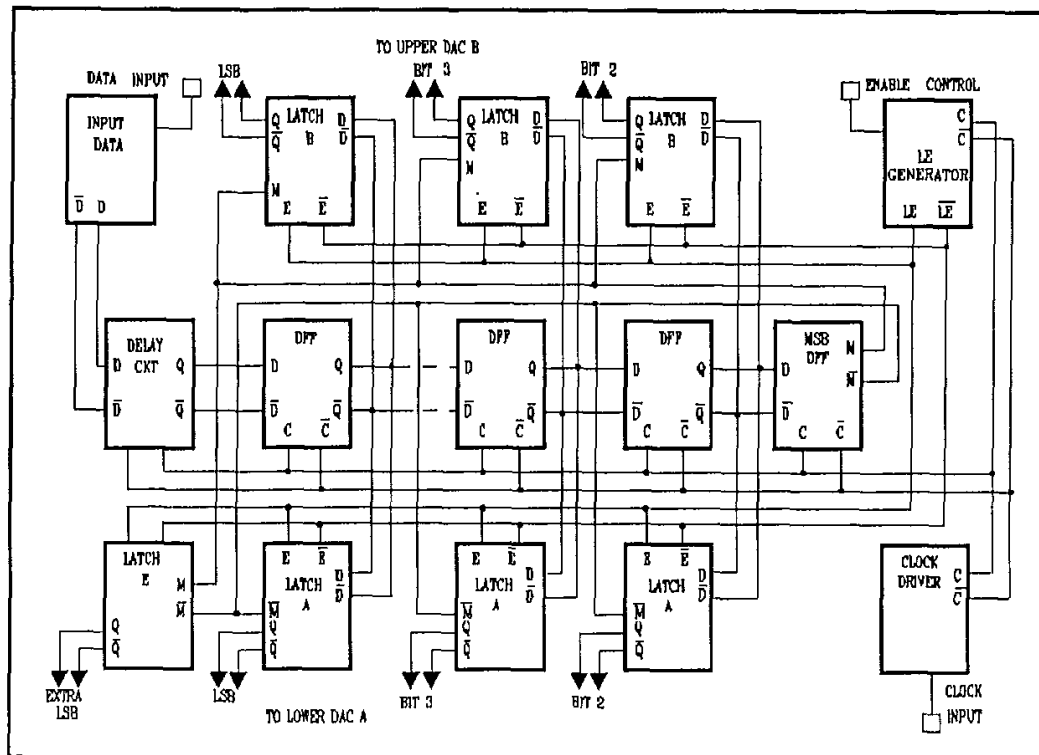


FIG. 4 LOGIC BLOCK DIAGRAM

