



Matched N-Channel JFET Pairs

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
2N5564	-0.5 to -3	-40	7.5	-3	5
2N5565	-0.5 to -3	-40	7.5	-3	10
2N5566	-0.5 to -3	-40	7.5	-3	20

FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 3 pA
- Low Noise: 12 nV/√Hz @ 10 Hz
- Good CMRR: 76 dB
- Minimum Parasitics

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals
- Maximum High Frequency Performance

APPLICATIONS

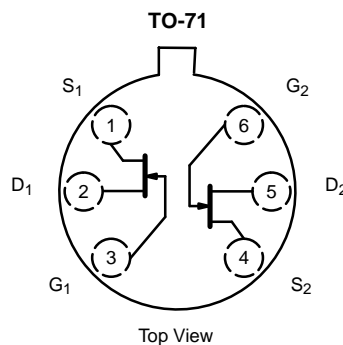
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters
- Matched Switches

DESCRIPTION

The 2N5564/5565/5566 are matched pairs of JFETs mounted in a TO-71 package. This two-chip design reduces parasitics for good performance at high frequency while ensuring extremely tight matching. This series features high breakdown voltage ($V_{(BR)DSS}$ typically > 55 V), high gain (typically > 9 mS), and <5 mV offset between the two die.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information).

For similar products see the low-noise U/SST401 series, and the low-leakage 2N5196/5197/5198/5199 data sheets.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-40 V
Gate-Gate Voltage	±80 V
Gate Current	50 mA
Lead Temperature ($1/16$ " from case for 10 sec.)	300 °C
Storage Temperature	-65 to 200 °C

Operating Junction Temperature	-55 to 150 °C
Power Dissipation :	Per Side ^a 325 mW
	Total ^b 650 mW

Notes

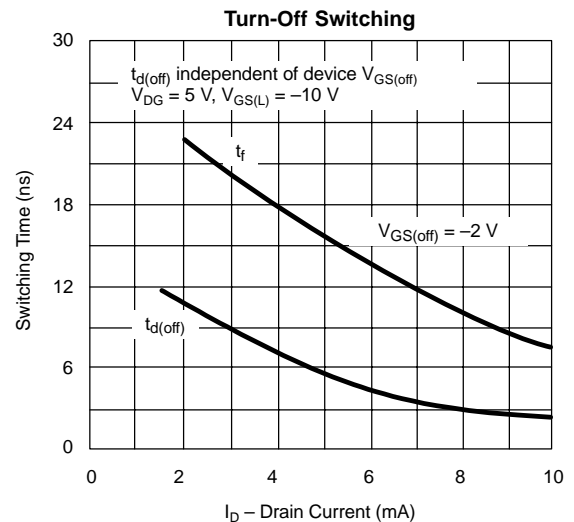
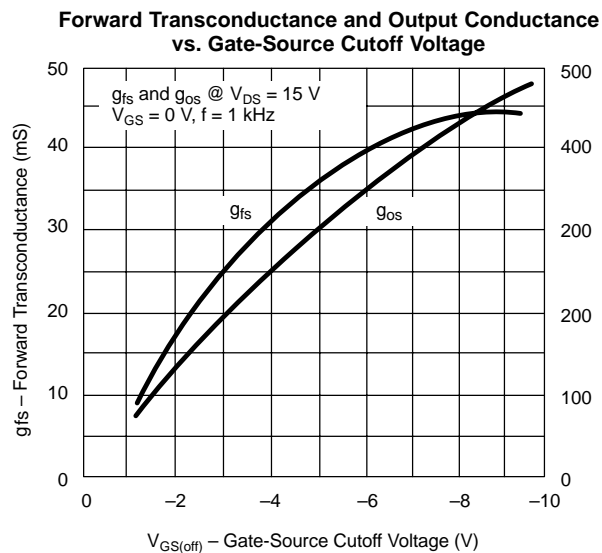
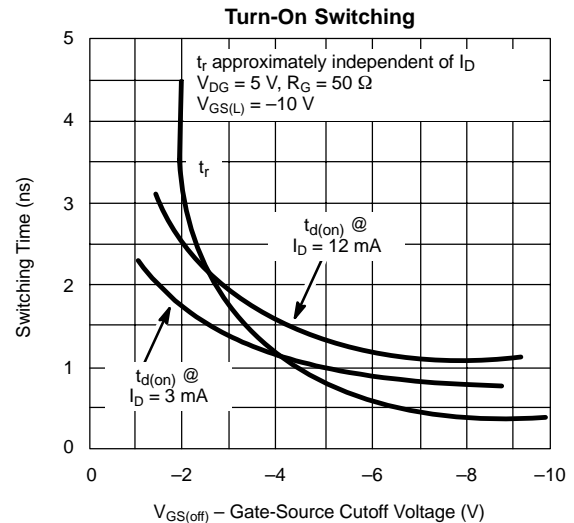
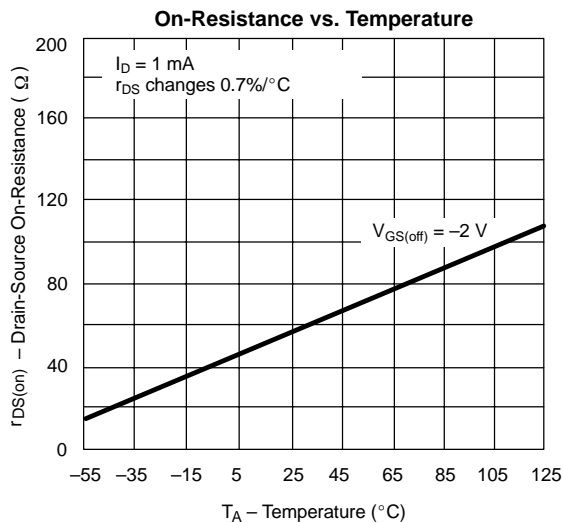
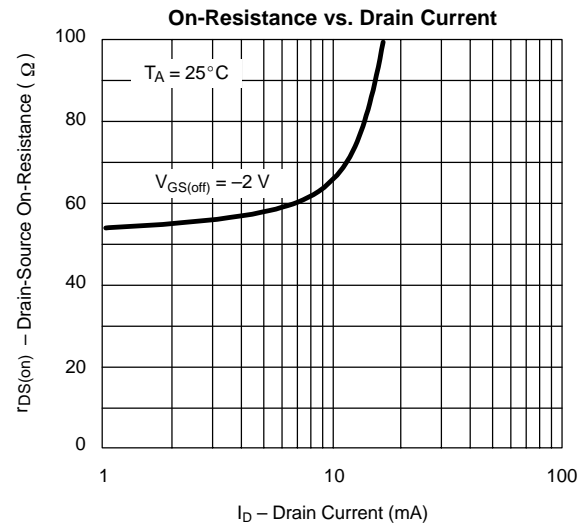
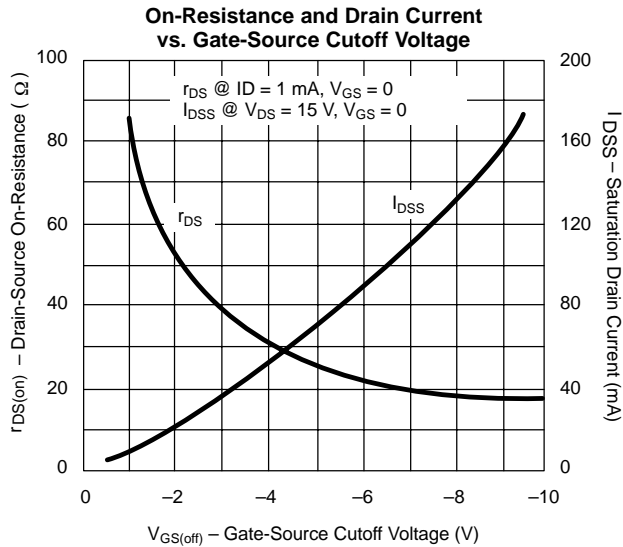
- Derate 2.6 mW/°C above 25 °C
- Derate 5.2 mW/°C above 25 °C

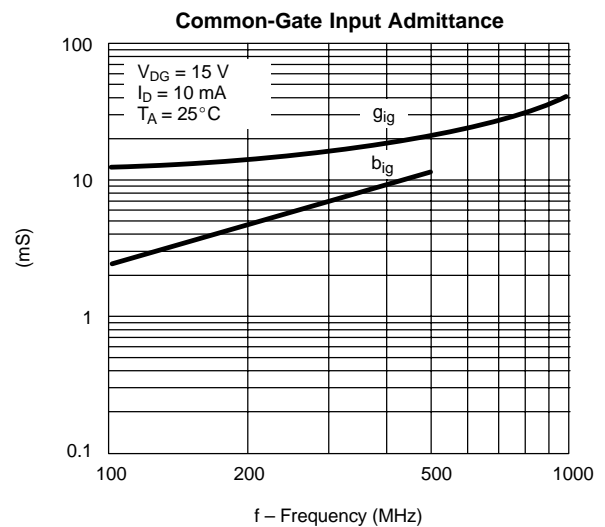
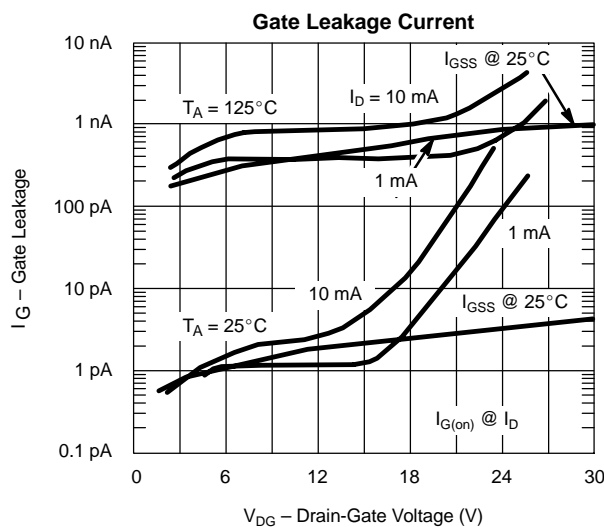
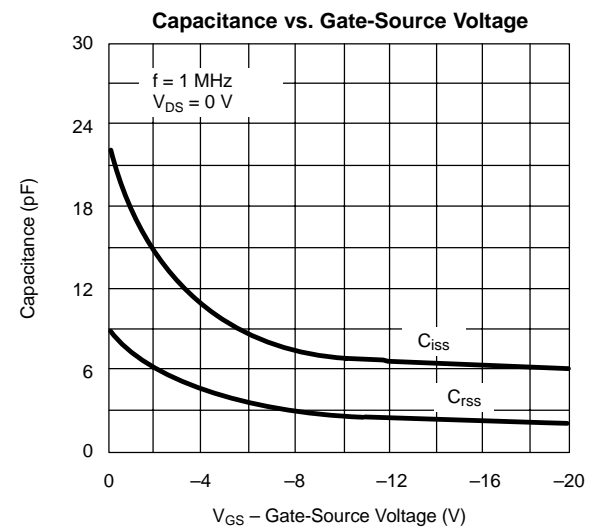
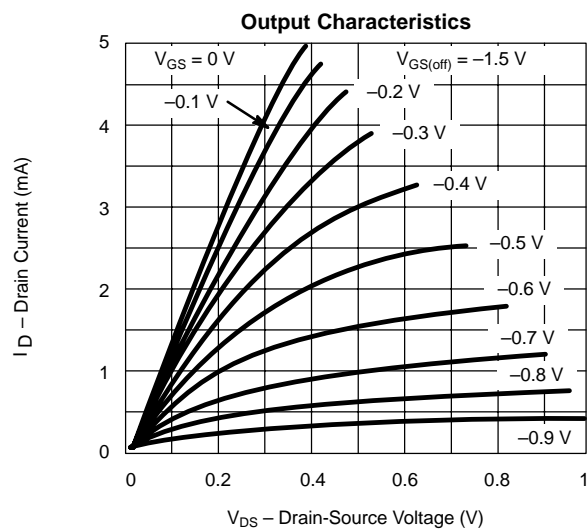
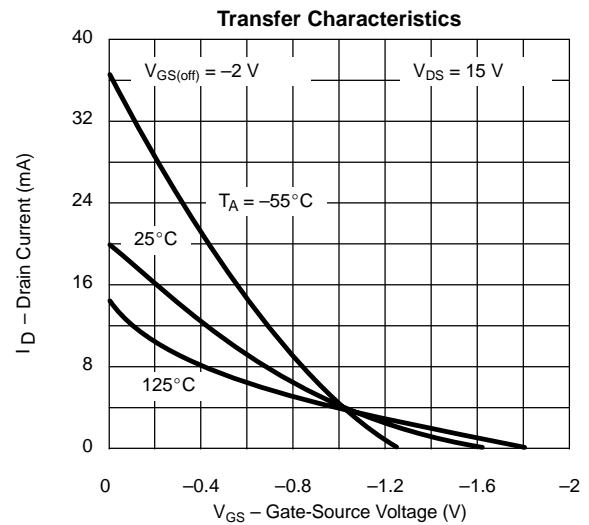
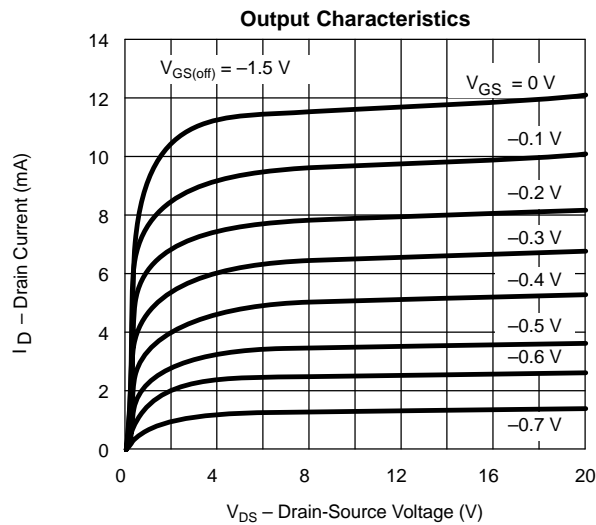
SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit
				2N5564		2N5565		2N5566		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 15 V, I _D = 1 nA	-2	-0.5	-3	-0.5	-3	-0.5	-3	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 15 V, V _{GS} = 0 V	20	5	30	5	30	5	30	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -20 V, V _{DS} = 0 V	-5		-100		-100		-100	pA
		T _A = 150 °C	-10		-200		-200		-200	nA
Gate Operating Current ^c	I _G	V _{DG} = 15 V, I _D = 2 mA	-3							pA
		T _A = 125 °C	-1							nA
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, I _D = 1 mA	50		100		100		100	Ω
Gate-Source Voltage ^c	V _{GS}	V _{DG} = 15 V, I _D = 2 mA	-1.2							V
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 2 mA , V _{DS} = 0 V	0.7		1		1		1	
Dynamic										
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 15 V, I _D = 2 mA f = 1 kHz	9	7.5	12.5	7.5	12.5	7.5	12.5	mS
Common-Source Output Conductance	g _{os}		35		45		45		45	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 15 V, I _D = 2 mA f = 100 MHz	8.5	7		7		7		mS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 15 V, I _D = 2 mA f = 1 MHz	10		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		2.5		3		3		3	
Equivalent Input Noise Voltage	e _n	V _{DS} = 15 V, I _D = 2 mA f = 10 Hz	12		50		50		50	nV/ √Hz
Noise Figure	NF		R _G = 10 MΩ			1		1		1
Matching										
Differential Gate-Source Voltage	V _{GS1} -V _{GS2}	V _{DG} = 15 V, I _D = 2 mA			5		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	V _{DG} = 15 V, I _D = 2 mA T _A = -55 to 125 °C			10		25		50	μV/ °C
Saturation Drain Current Ratio ^c	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 15 V, V _{GS} = 0 V	0.98	0.95	1	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 15 V, I _D = 2 mA f = 1 kHz	0.98	0.95	1	0.90	1	0.90	1	
Common Mode Rejection Ratio ^c	CMRR	V _{DG} = 10 to 20 V I _D = 2 mA	76							dB

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
c. This parameter not registered with JEDEC.

NCBD

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)


**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**