File Number **64**

2N3439, 2N3440, 2N4063, 2N4064

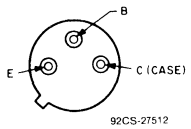
High-Voltage Silicon N-P-N Planar Transistors

For High-Speed Switching and Linear-Amplifier Applications

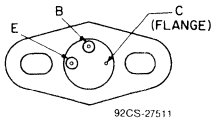
Features:

- *High voltage ratings:*
  V_{CBO} = *450 V max. (2N3439, 2N4063)*
  = *300 V max. (2N3440, 2N4064)*
  $V_{CEO}(sus)$ = *350 V max. (2N3439, 2N4063)*
  = *250 V max. (2N3440, 2N4064)*
- *Maximum safe-area-of-operation curves*
- *Low saturation voltages*

TERMINAL DESIGNATIONS



JEDEC TO-205AD



JEDEC TO-205AD WITH FLANGE

The 2N3439*, 2N3440**, 2N4063 and 2N4064 are epitaxial-base silicon n-p-n planar transistors with high breakdown voltages, high-frequency response, and fast switching speeds.

These transistors are intended for industrial, commercial, and military equipment. Typical applications include high-voltage differential and operational amplifiers, high-voltage inverters, and high-voltage, low-current switching and series regulators.

The 2N3439 and the 2N3440 differ primarily in their voltage ratings. They are supplied in the JEDEC TO-205AD hermetic package.

The 2N4063 and 2N4064 have the same voltage ratings as the 2N3439 and 2N3440 respectively, but employ a flange package.

*Formerly RCA Dev. No. TA2458.
**Formerly RCA Dev. No. TA2470.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	2N3439 2N4063	2N3440 2N4064	
* V_{CBO}	450	300	V
* $V_{CEO}(sus)$	350	250	V
* V_{EBO}	7	7	V
* I_C	1	1	A
* I_B	0.5	0.5	A
P_T:			
$T_C \leq 25°C$	10	10	W
* $T_A \leq 50°C$	1 (2N3439)	1 (2N3440)	W
$T_C > 50°C$ ... Derate linearly at	0.057		W/°C
* T_{stg}, T_J	−65 to +200		°C
* T_L (During soldering) At distance 1/32 in. (0.8 mm) from case for 10 s max.	255		°C

*2N-types in accordance with JEDEC registration data.

2N3439, 2N3440, 2N4063, 2N4064

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

	CHARACTERISTIC	TEST CONDITIONS				LIMITS				UNITS
		VOLTAGE V dc		CURRENT mA dc		2N3439 2N4063		2N3440 2N4064		
		V_{CE}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	
*	I_{CBO} $I_E = 0$	360 250				– –	20 –	– –	– 20	μA
	I_{CEO}	300 200			0 0	– –	20 –	– –	– 50	μA
	I_{CEV}	450 300	–1.5 –1.5			– –	0.5 –	– –	– 0.5	mA
*	I_{EBO}		–6	0		–	20	–	20	μA
*	h_{FE}	10 10		20[a] 2[a]		40 30	160 –	40 –	160 –	
	V_{CEO}(sus)			50[a]	0	350[b]	–	250[b]	–	V
	V_{BE}(sat)			50[a]	4	–	1.3	–	1.3	V
	V_{CE}(sat)			50[a]	4	–	0.5	–	0.5	V
*	$Re(h_{ie})$ f = 1 MHz	10		5		–	300	–	300	Ω
*	h_{fe} f = 1 kHz	10		5		25	–	25	–	
*	$\|h_{fe}\|$ f = 5 MHz	10		10		3	–	3	–	
*	C_{obo} $V_{CB} = 10$ V, $I_E = 0$ f = 1 MHz					–	10	–	10	pF
	C_{ib} f = 1 MHz		–5	0		–	75	–	75	pF
	$I_{S/b}$ t = 1 s, nonrep.	200				50	–	50	–	mA
	$R_{\theta JC}$					–	17.5	–	17.5	°C/W
	$R_{\theta JA}$ 2N3439, 2N3440					–	150	–	150	

* 2N-types in accordance with JEDEC registration data.

[a] Pulsed, pulse duration = 300 μs, duty factor ≤ 2%.

[b] *CAUTION:* Sustaining voltage V_{CEO}(sus) *MUST NOT* be measured on a curve tracer.

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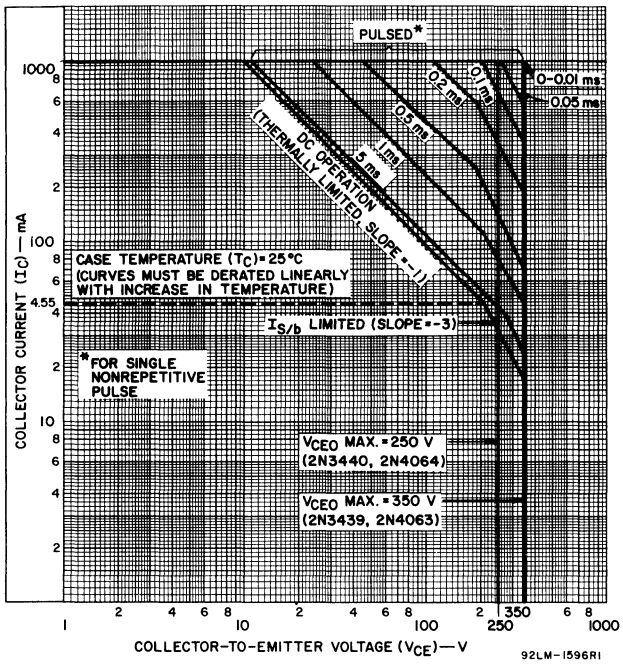

Fig. 1 – Maximum operating areas for 2N3439, 2N3440, 2N4063, and 2N4064.

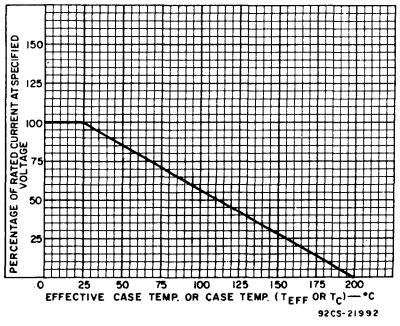

Fig. 2 – Current derating curve for all types.

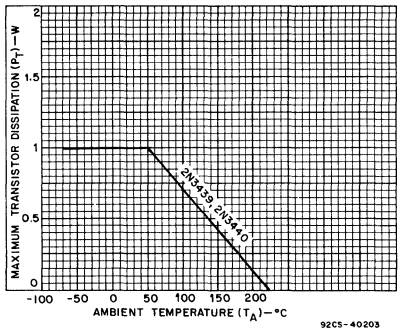

Fig. 3 – Dissipation derating curve for 2N3439 and 2N3440.

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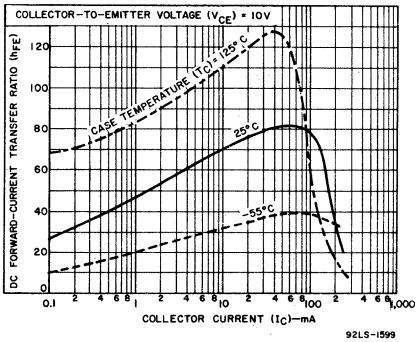


Fig. 4 – Typical dc beta characteristics for all types.

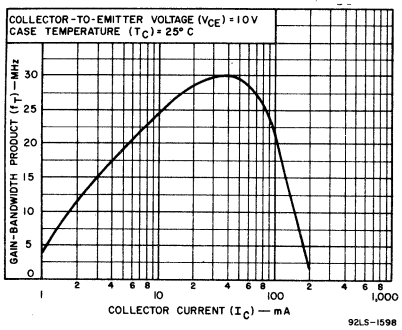


Fig. 5 – Typical gain bandwidth product for all types.

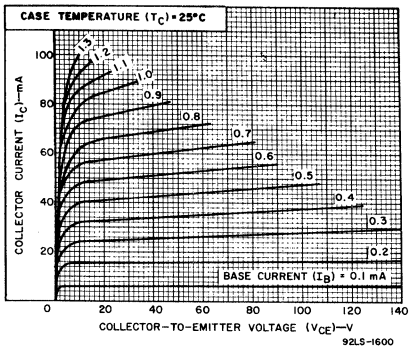


Fig. 6 – Typical output characteristics for all types.

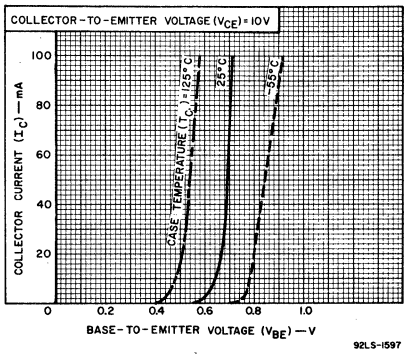


Fig. 7 – Typical transfer characteristics for all types.

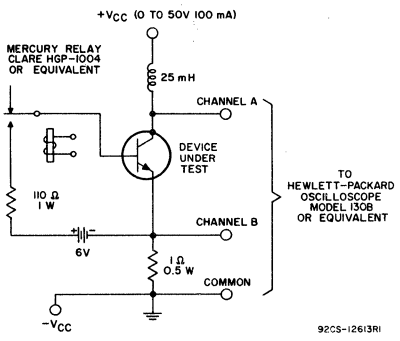
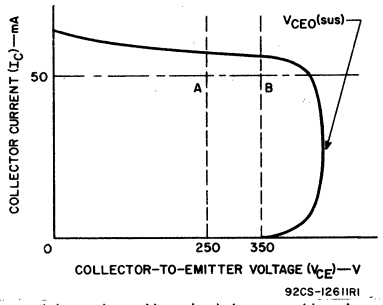


Fig. 8 – Circuit used to measure sustaining voltage V_{CEO}(sus) for all types.



The sustaining voltage V_{CEO}(sus) is acceptable when the trace falls to the right and above point "A" for types 2N3440 and 2N4064. The trace must fall to the right and above point "B" for types 2N3439 and 2N4063.

Fig. 9 – Oscilloscope display for measurement of sustaining voltages.