

32 BIT shift register for aerial to parallel DATA  
up to 32 bit Data word and WCK=2x32 bit=64bit length

Inverter

ALL unused inputs to GND (or +V)

ALL unused outputs left open

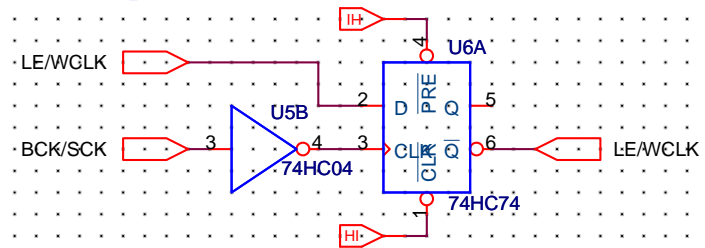
all inter ICs couple with R  
and trim with scope for good signal integrity

proper power pins decoupling and power suplu

I2S to LEFT JUSTIFIED  
1bit WCLK delay

(for channel SWITCH L/R  
use Q.out)

I2S input



LJust

