32 BIT shift register for aerial to parallel DATA
up to 32 bit Data word and WCK=2x32 bit=64bit length

Inverter
ALL unused inputs to GND (or +V)
ALL unused outputs left open

all inter ICs couple with R
and trim with scope for good signal integrity

proper power pins decoupling and power suplu

I2S to LEFT JUSTIFIED
1bit WCLK delay

(for chanel SWITCH L/R
use Q out)

I2S input

LE/WCLK
BCK/SCK
U5B
74HC04
U6A
74HC74
D PRE Q CLR Q
HI

LJust

BCK/SCK
LE/WCLK
LEFT JUSTIFIED

74HC164
U1
U2
U3
U4
CLK A B CLR
QA QB QC QD QE QF QG QH
msb-8
msb-9
msb-16
msb-17
msb-24
msb-25
LSB
U5A
74HC04
MSB
MSB_ALL
16BIT_LSB
24BIT_LSB
32BIT_LSB
BCK/SCK
DATA