

A Class-D Amplifier with Digital PWM and Digital Loop-Filter using a Mixed-Signal Feedback Loop

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Abstract—A digital class-D audio amplifier is presented that is based on digital pulse-width modulation (PWM) and a combination of digital and analog feedback. Unlike other recent implementations for low-power applications this amplifier directly accepts digital input as the digital-to-analog conversion is an inherent feature of the presented topology.

The feedback topology uses a hybrid scheme with digital feedback to improve the performance of the PWM and analog-feedback to mitigate analog imperfections and to improve power supply rejection. Because of the proposed feedback scheme, the requirements on the analog-to-digital converter (ADC) in the feedback loop are greatly relaxed allowing the use of a continuous-time $\Delta\Sigma$ -modulator with low power consumption.

The class-D amplifier was realized in a standard 180 nm CMOS technologies and drives 1.2 W into an 8 Ω load and achieves a total harmonic distortion plus noise (THD+N) of -96 dB, a signal-to-noise ratio (SNR) of 99.9 dB having an efficiency of 91 %.

Index Terms—audio, class-D, delta-sigma, digital pulse-width modulation, EMI, low-power

I. INTRODUCTION

Class-D amplifiers are used in mobile applications because of their high efficiency that results in a long battery lifetime. As a result cooling requirements are low and a very compact design is possible. In order to avoid bulky filter structures at the output of the class-D amplifier and to retain a small footprint often a BD-modulation scheme is used that reduces the ripple current and enables so-called filterless operation.

As the filter is removed the PWM-signal is directly used to drive the speaker which results in increased electromagnetic emissions, which is one of the reasons why class-AB amplifiers are still being used. The electromagnetic emissions (EMI) created by BD-modulation is known to not only have a differential-mode but also a strong common-mode component, which is much more difficult to handle. Various solutions to this problems are known, like spread-spectrum modulation and slew-rate control. Those additional EMI-reduction measures usually have some impact on the audio quality of the signal. Using digital techniques a significant EMI-reduction can be achieved [1]. Using a digital input signal has the advantage that errors introduced by a digital EMI-reduction method can be compensated in the digital domain, giving rise to the need for a digital interface for the input signal.

Since many signal sources in the targeted application are digital already, the use of a digital input class-D amplifier is an additional advantage since no dedicated D/A-converter is

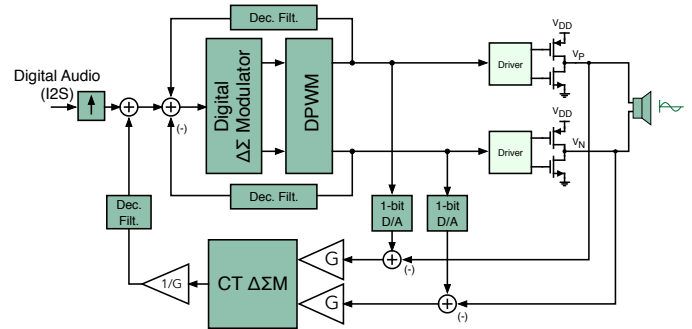


Fig. 1. Topology of the proposed class-D amplifier.

required. It also eliminates the need to place the class-D amplifier close to the analog signal source, because interference no longer is an issue, as the digital signal is much more robust.

Digital class-D amplifiers are readily obtained if an open-loop architecture is chosen, but the problem is that, imperfections in the output stage and disturbances on the power-supply rails are not suppressed. Therefore closed-loop solutions are generally preferred. Closing the loop in the digital domain introduces the need for high resolution ADCs with low-latency for stability reasons [10].

In this work a class-D amplifier is presented that uses a digital loop filter (Fig. 1), using a hybrid feedback concept in order to reduce distortion and also mitigate the requirements on the A/D-converter.

Using the A/D-converter to process the full signal, the system performance is limited by the performance of the A/D-converter [6]. In [10] a higher power consumption for the ADC (30 mW) was used in order to achieve better performance. However, for applications targeted at a lower output power, the contribution of the ADCs power consumption needs to be minimized. Processing the difference between a reference audio signal and the output-signal can be used to reduce the requirements as shown in [5], where a quiescent current of 20.52 mA is reported.

In this work a design for a lower output power is presented. We propose to cancel the PWM signal before the A/D-converter and convert only the small error signal. In order to avoid additional filtering, a continuous-time $\Delta\Sigma$ -modulator is implemented, because of its inherent anti-aliasing filtering. The tradeoff between performance and power consumption

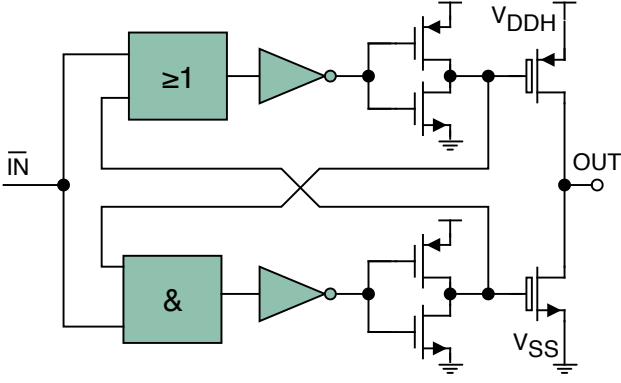


Fig. 2. Halfbridge used in the power-stage of the class-D amplifier.

was made to achieve a THD+N of -96 dB in our design with an ADC that consumes only 0.72 mA (1.3 mW).

II. DIGITAL-LOOP CLASS-D AMPLIFIER ARCHITECTURE

The topology of the proposed class-D amplifier is shown in Fig. 1. It uses a digital implementation of a pulse-width modulator. In the analog domain the pulse-width modulation would be realized using a triangle or a saw-tooth signal as reference for a comparison with the audio signal. This principle cannot be easily transferred into the digital domain because the timing resolution in order to achieve the required SNR would require unfeasibly high clock frequencies [2]. The resolution of the pulse-width modulator in the audio band can be effectively increased by using an additional noise-shaper as proposed in [3]. In this implementation a fifth-order $\Delta\Sigma$ -modulator is used to reduce the resolution of the 24-bit audio signal down to a 7-bit value. The quantized output is then compared to a digital triangular waveform in order to produce a PWM-signal. Because of the noise-shaping an effective resolution of more than 16-bit in the band of interest is obtained.

The resulting signal is then used to control the drivers of the H-bridge. Without further measures the signal quality suffers from distortion produced by the digital PWM and the distortion introduced by the imperfections in the power-stage. On top of this, interferers on the power-supply will degrade the performance even further. Therefore the proposed system uses a feedback concept that is shown in more detail in the next section.

III. FEEDBACK CONCEPT

A digital $\Delta\Sigma$ -modulator is used to increase the effective resolution of the digital PWM. It has a fifth-order loop filter that was realized without multipliers using quantized coefficients. A simple realization with shift/add-operations is therefore possible. Since stability is a critical issue with higher-order modulators the order of the modulator can be dynamically reduced to recover from overload.

The DPWM generator is realized as a simple up-/down-counter generating a digital triangular wave. The DPWM uses the highest available clock-frequency on chip, which is

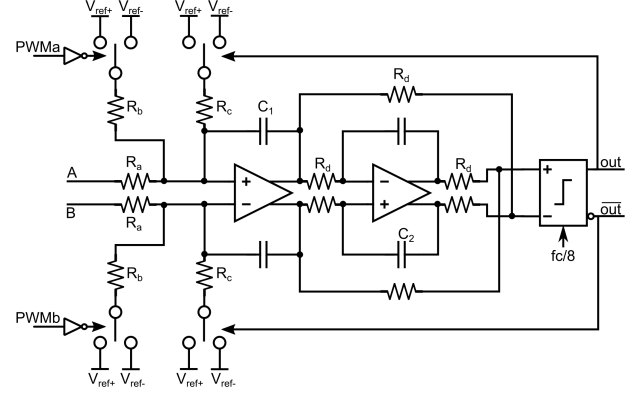


Fig. 3. Error feedback ADC. The supply voltage is used for V_{ref} .

100 MHz in the current design. Each ramp consists of 128 cycles, resulting in a period of $100 \text{ MHz} / 256$ of the PWM-signal equaling 390.625 kHz. During each period the output signal of the loop-filter is sampled twice in order to reduce distortion.

As the DPWM is known to introduce distortion [2], the DPWM signal is filtered and feed back to the input of the digital $\Delta\Sigma$ -modulator which reduces the distortion in the digital domain. As pointed out in [2] the modulator would have to be operated at the DPWM frequency which would result in a high power-consumption. Therefore the signal is decimated in order to reduce the frequency of the digital $\Delta\Sigma$ -modulator, which then operates at $1/8$ th of the clock frequency, reducing the power consumption by the same factor.

The power stage is realized as an H-bridge topology consisting of two identical half-bridges (see Fig. 2). Each half-bridge consists of an NMOS and a PMOS power transistor operated at a 5 V supply. To avoid cross-conduction, a small dead-time is implemented by sensing the gate voltage of the power transistors with logic gates (AND / OR) and delaying the driving circuit.

The transistors are standard CMOS transistors with a thicker oxide and they are not optimized for switching operation. Using a different 180 nm technology (e.g. BCD 180 nm) and a smaller package (with less parasitics) a further increase in performance can be expected, which was confirmed using circuit simulation of the output stage.

IV. FEEDBACK ADC

The imperfections of the output-stage and possible interferers on the supply line are reduced by feedback of the error-signal using a continuous-time $\Delta\Sigma$ -modulator (CT-DSM). Continuous-time modulators have the advantage that the sampling of the signal occurs after loop-filter which inherently provides anti-aliasing filtering of the sampled signal. This has the advantage that the output signal can be tracked continuously without the need for a dedicated anti-aliasing filter, as it would be necessary for a discrete-time implementation.

Placing an ADC in the feedback loop often makes the ADC the performance limiting block [6]. For continuous-time delta-

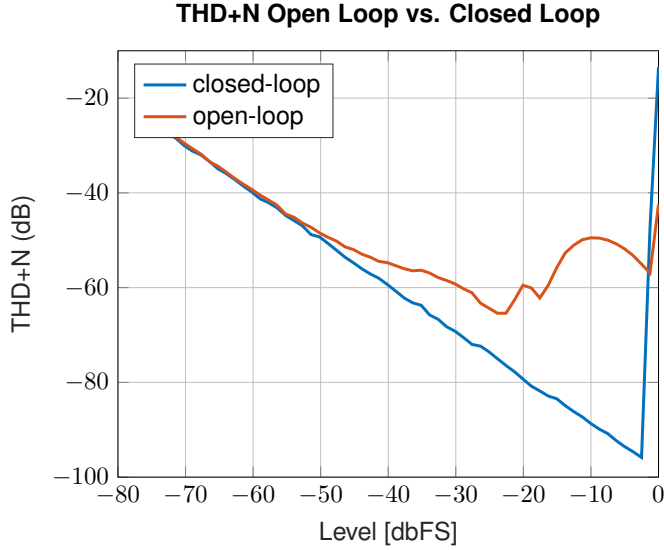


Fig. 4. Measured THD+N of the system without and with feedback. It can be seen, that feedback improves the performance at higher power levels.

sigma modulators this is a critical issue as clock-jitter reduces the performance and has to be taken into consideration when designing such as system. In order to relax the requirements on the ADC only the error-signal is processed which is usually very small. This opens the possibility to scale the input signal to the ADC in the analog domain, then perform the A/D-conversion and scale down the signal in the digital domain.

The input stage of the CT-DSM is illustrated in Fig. 3. It consists of an integrator that senses the differential output voltage of the H-bridge (inputs A and B). The resistors convert the sensed-voltage into a current which is integrated by the first stage of the CT-DSM. At the same time a digitally controlled switch produces a replica of the PWM-signal (labeled PWMa and PWMb) that cancels the major part of the sensed signal. In this way only the error between the digital PWM signal and the analog output needs to be processed in the feedback loop. The output voltage of the H-bridge contains a large common-mode component that needs to be handled by the amplifier in the first stage. Using this kind of signal cancellation the common-mode voltage is reduced by a large part, leaving only residual spikes that can be explained by timing and slope differences.

V. MEASUREMENTS

The proposed class-D amplifier is realized in a 180nm CMOS technology that offers 5V-transistors for the power stage. The active chip area is about 1.5 mm^2 . The chip is packaged in a CLCC-package. The chip photograph is shown in Fig. 6 where the power stage can be seen on the right side.

The measurement shown in Fig. 4 demonstrates the effectiveness of the proposed feedback concept. The feedback input can be disabled, operating the amplifier basically in an open-loop configuration in order to demonstrate the distortion introduced by the power-stage.

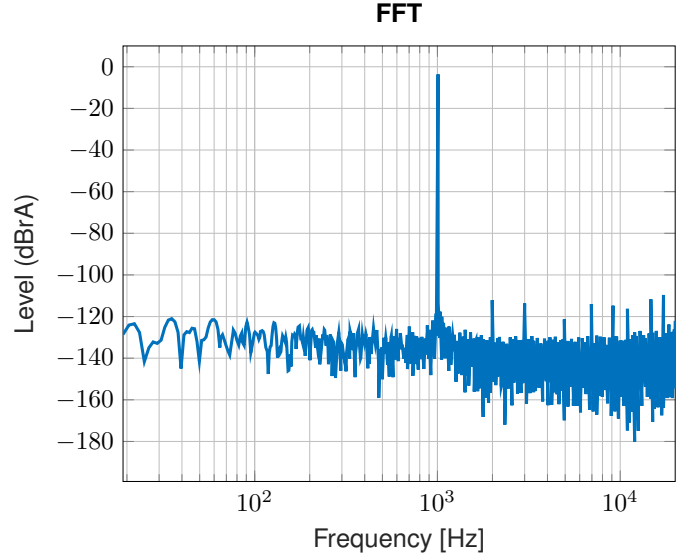


Fig. 5. FFT plot of the measured output signal of the class-D amplifier.

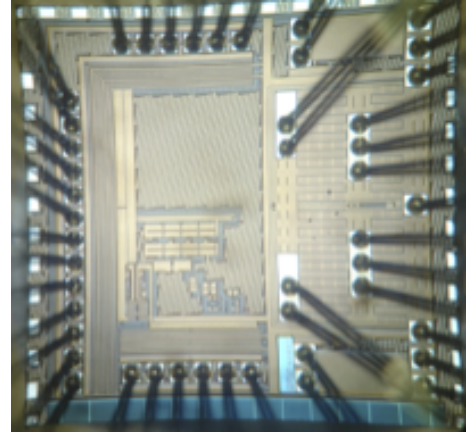


Fig. 6. The proposed concept was implemented in a standard 180nm CMOS technology. The right side of the chip contains the transistors of the H-bridge, the left side contains the signal processing blocks.

The performance of the chip was evaluated using an Audiotprecision APx555 system using the digital output (I2S) to drive the chip. The amplifier was measured with a load of $8\ \Omega$ plus $44\ \mu\text{H}$ corresponding to a typical $8\ \Omega$ speaker. A plot of the output spectrum can be seen in Fig. 5.

In Table I an overview of current state-of-the-art implementations of class-D amplifiers is given. Most audio sources are digital therefore in the case of a class-D with an analog input an additional DAC would be required, which increases the power consumption and decreases the overall efficiency. For a class-D amplifier that directly accepts a digital input no additional DAC is needed.

A direct comparison is rather difficult because for the low-power range typical for portable devices mainly analog loop filters are used. Nevertheless two digital input class-D amplifiers could be found in the literature. Compared to [3] a higher THD+N is achieved at a similar efficiency. The

TABLE I
STATE-OF THE ART IMPLEMENTATIONS OF CLASS-D AMPLIFIERS

	This work	ESSCIRC '11 [3]	JSSC '15 [8]	JSSC '14 [7]	JSSC '16 [11]	JSSC '16 [9]	JSSC '18 [4]
Input	digital		analog				
Filter	digital	digital	analog	analog	analog	analog	analog
PWM	digital	digital	digital	analog	analog	analog	analog
THD+N [dB]	-96	-76.5	-90	-91.5	-103.5	-88	-90
Load [Ω]	8	4	8	8	4	8	8
Power [W]	1.2	2.7	1.5	0.85	3.1	1.02	1.45
Efficiency [%]	91	90	80	94	89.5	92	94
I _q [mA]	3.1	-	2.8	3.1	1.45	2.4	0.96
Switching Frequency [kHz]	390	384	2133	320	650	200	215
Process [nm]	180	140	55	65	153	500	500

implementation presented in [8] achieves a comparable, yet lower THD+N, however the efficiency is much lower, which can be attributed to a higher switching frequency. Simulations suggest that with the presented topology a higher THD+N can be achieved as well using a higher switching frequency since the ADC is not the limiting factor in the design, however the efficiency would decrease. Since the design was targeted at portable devices the trade-off was made in favor of the power consumption.

Extending the comparison to include also analog implementations still a comparable performance as in [7, 9] can be found. The solution presented in [11] shows better performance. However, an additional DAC would be required if a digital source was used.

VI. CONCLUSION

A 1.2 W class-D amplifier with digital input, digital loop filter and digital PWM generation was presented. The PWM signal in the feedback path is cancelled to relax the requirements on the ADC. The PWM generator uses a digital feedback loop to suppress distortion introduced by the PWM generation.

The whole system achieves a THD+N of -96dB and an SNR of 99.9 dB achieving a better performance than all comparable digital input implementations and some of the analog input solutions in this output power class. Since digital solutions benefit from a transition to smaller feature sizes the proposed solution is a viable candidate for future implementations, in particular when digital techniques are used to reduce electromagnetic emissions.

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