

A General Relationship Between Amplifier Parameters and its Application to PSRR Improvement

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Abstract— A general relationship between the gains of multiterminal amplifiers is derived in this paper. It reveals a constraint for the simultaneous improvement of the common-mode and the power-supply rejection ratios of the simple operational amplifier. This constraint can be relaxed by either adding a supplementary input terminal to the amplifier circuit or using a fully differential design. The method can be used to improve the power-supply rejection ratios in operational amplifiers. Several implementations of a two-stage operational amplifier illustrate this technique.

I. INTRODUCTION

AN important parameter of operational amplifiers is the differential gain, A_d , which is the ratio between the single-ended output voltage and the difference of the two input voltages. Additional specifications describe the signal transfer from the supply terminals to the output, A_{dd} and A_{ss} , and the common-mode gain from the input terminals to the output, A_{cm} . For an ideal amplifier these parasitic gains should be zero, and it is the aim of a good amplifier design to achieve this goal as nearly as possible. We show in this paper, however, that these gains are not independent of each other and that their sum is close to unity in practical configurations. Expressed in terms of the (frequency-dependent) common-mode rejection ratio, $CMRR(s) = A_d(s)/A_{cm}(s)$, the (frequency-dependent) power-supply rejection ratios, $PSRR^+(s) = A_d(s)/A_{dd}(s)$ and $PSRR^-(s) = A_d(s)/A_{ss}(s)$, and the differential gain, $A_d(s)$, we find more exactly that

$$\frac{1}{CMRR(s)} + \frac{1}{PSRR^+(s)} + \frac{1}{PSRR^-(s)} = \frac{1}{A_d(s)} \frac{Z_{L0}}{Z_{L0} + Z_{out}} \quad \text{or} \quad (1a)$$

$$A_{cm}(s) + A_{dd}(s) + A_{ss}(s) = \frac{Z_{L0}}{Z_{L0} + Z_{out}} \quad (1b)$$

where Z_{out} denotes the output impedance of the considered operational amplifier and Z_{L0} is the reference load for which the differential gain and the various rejection ratios are measured. Equation (1b) states that in absence of

a load, $Z_{L0} \rightarrow \infty$, the common-mode gain and the gains from the power supplies to the output sum to unity. Simple operational amplifier models often assume that only the differential signal is amplified, but according to (1) this is physically impossible. A related result is found in filter theory, cf. e.g. Fialkow and Gerst [1] and Hilberman [2], where it is shown that for a passive three-terminal network, having no internal connection to ground, the voltage transfer function from one input to the output is the one's complement of the transfer function from the other input to the output. More generally, [2] proves, based on Kirchhoff's and Ohm's law, that a multi-terminal network with no connection to the common terminal exhibits complementary transfer functions. We use a more general method namely a gauge-invariance argument to establish our relationship (1) and its generalizations. With this relationship, which seems not to be well known in amplifier theory, we derive implications for the design of differential amplifiers featuring good rejections of the parasitic signals.

In practice (1) implies that at least one of the parasitic gains is in the order of magnitude of unity. In the classical two-stage operational amplifier scheme this usually concerns the gain from one power-supply terminal. Ripple or other parasitic signals at this supply terminal are, at mid frequencies, fully transferred to the output through the integrator capacitor. This weakness of the classical operational amplifier scheme is well known. A remedy against this parasitic signal-transfer path has been proposed in [3] by introducing a cascode structure and an additional terminal. We show that this solution is just a special realization of a more general idea which is based on relationship (1) and that alternative and even better results are obtainable.

This paper is structured as follows: In Section II we outline our arguments that lead to (1) and extend the results for more advanced amplifier configurations including operational amplifiers with an additional input terminal, differential amplifiers with differential outputs, differential amplifiers with balanced outputs, and differential difference amplifiers (DDAs) [4] [5]. In Section III we illustrate the use of relationship (1) by specific circuit examples: adding an input terminal with unity gain to the output of the amplifier circuit yields small values of the remaining parasitic gains. With a balanced output amplifier, even if only one output is used, even better performance in rejecting parasitic signals is achieved. In the Appendix we present the derivation of the general relationship for multiple-input

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multiple-output amplifiers from which we obtain the results of Section II.

II. GAIN RELATIONSHIP FOR VARIOUS AMPLIFIER TYPES

The electrical notation-conventions adopted in this paper closely follow [6]. Signals are generally designated as a symbol with a subscript. The symbol as well as the subscript are each either upper or lower case according to the following conventions illustrated in the case of a voltage signal: v_X denotes the total instantaneous value of the voltage, V_X denotes the operating-point value of the voltage, whereas v_x stands for its small signal value $v_X - V_X$. Finally, the (bilateral) Laplace transformation of v_x is denoted by V_x : $v_x(t) \bullet \bullet V_x(s)$.

For a proof-outline of (1) we consider a conventional two-input one-output amplifier with inputs v_P and v_N , output v_O , and two power supplies v_{DD} and v_{SS} . Note that these amplifiers have *no separate ground terminal*. We assume that the amplifier circuit is biased into an operating point where the amplifier is described by an equivalent lumped, linear, time-invariant circuit. To be able to describe the effect of time varying power supplies, the equivalent linear circuit is assumed to have four (small) signal inputs v_p , v_n , v_{dd} , and v_{ss} , and one output v_o . As is common practice in amplifier theory, we introduce the differential-mode voltage $v_d \stackrel{\text{def}}{=} v_p - v_n$ and the common-mode voltage $v_{cm} \stackrel{\text{def}}{=} (v_p + v_n)/2$ to describe the signal inputs. In terms of these signals and the supply voltages, the linear time-invariant circuit is described in the Laplace domain by

$$V_o = A_d(s)V_d + A_{cm}(s)V_{cm} + A_{dd}(s)V_{dd} + A_{ss}(s)V_{ss} \quad (2)$$

where $A_i(s)$, $i \in \{d, cm, dd, ss\}$, denote the differential-mode, the common-mode, and the power-supply gains, respectively.

Our argument that (1) must hold is based on a gauge transformation: Because the origin of the potential scale against which the voltages are measured cannot be fixed absolutely, we expect that all physically meaningful equations remain invariant if this origin is globally shifted (this is called gauge invariance or gauge symmetry) [7, p.220]. Applied to any equation characterizing the amplifier, this means that the addition of the same arbitrary time-varying voltage signal to all terminal voltages should yield the same equation. For (2) the addition of a gauge signal $v_{\text{gauge}}(t) \bullet \bullet V_{\text{gauge}}(s)$ leads to $V_o + V_{\text{gauge}} = A_d(s)V_d + A_{cm}(s)(V_{cm} + V_{\text{gauge}}) + A_{dd}(s)(V_{dd} + V_{\text{gauge}}) + A_{ss}(s)(V_{ss} + V_{\text{gauge}})$ and subtracting from this equation the amplifier's original description (2) leads to an equation containing the gauge-transformation signal $V_{\text{gauge}}(s)$, $V_{\text{gauge}} = (A_{cm}(s) + A_{dd}(s) + A_{ss}(s))V_{\text{gauge}}$. This in turn leads, because $v_{\text{gauge}}(t)$ and hence $V_{\text{gauge}}(s)$ are arbitrary small-signal quantities, to the following relationship between the parasitic amplifier gains for open circuit loads ($Z_{L0} \rightarrow \infty$) or ideal amplifiers in the sense of $Z_{\text{out}} \equiv 0$:

$$A_{cm}(s) + A_{dd}(s) + A_{ss}(s) = 1. \quad (3)$$

In amplifier practice, the usual description is not in terms of the gains $A_i(s)$, $i \in \{d, cm, dd, ss\}$, as introduced above, but instead, the differential-mode gain, $A_d(s)$, together with common-mode and power-supply *rejection ratios*, $CMRR(s)$, $PSRR^+(s)$, $PSRR^-(s)$, are used. In terms of these rejection ratios we can express (3) alternatively by

$$\frac{1}{CMRR(s)} + \frac{1}{PSRR^+(s)} + \frac{1}{PSRR^-(s)} = \frac{1}{A_d(s)}. \quad (4)$$

This is the essential part of (1) and holds for open-circuit loads ($Z_{L0} \rightarrow \infty$) or ideal amplifiers in the sense of $Z_{\text{out}} \equiv 0$. More generally, it approximately holds for amplifier/load combinations for which $|Z_{\text{out}}/Z_{L0}| \ll 1$ in the relevant frequency ranges. The more general relationship presented in the Appendix can be specialized for concrete amplifiers as follows:

Operational Amplifiers with a Reference Input. For operational amplifiers which have an additional input terminal v_{REF} , we obtain

$$A_{cm}(s) + A_{dd}(s) + A_{ss}(s) + A_{\text{ref}}(s) = 1 \quad (5)$$

where $A_{\text{ref}}(s)$ is the transfer function from the additional terminal to the output. We note from (3) that for a simple operational amplifier at least one of the parasitic gains must be nonzero, whereas for an operational amplifier with a reference input we obtain an additional degree of freedom for the choice of a nonzero-gain path. Therefore, if the additional terminal can be chosen so that the gain to the output is unity, the remaining parasitic gains add to zero which is the necessary condition that these gains become zero individually. Examples 3 and 4 in Section III illustrate that this favorable situation actually exists in real circuits. If the reference terminal v_{REF} is connected to a noise-free potential against which the signals are defined, then $A_{\text{ref}}(s) \approx 1$ has no influence on the output signal, i.e. we have $V_{\text{ref}} \equiv 0$ and in turn $A_{\text{ref}}(s)V_{\text{ref}} \equiv 0$. Note that designing such a reference terminal into the amplifier circuit must not deteriorate the signal gain $A_d(s)$.

Equation (5) leads to a generalization of (3) for finite loads or nonzero output impedances of the amplifier. This reflects the practical situation where the gains $A_d(s)$, $A_{cm}(s)$, $A_{dd}(s)$, and $A_{ss}(s)$ are measured with a *finite* load impedance Z_{L0} to ground. This situation is now analyzed by connecting one side of the load Z_{L0} to the amplifier's output terminal and considering the other side, which for usual *gain measurements* is connected to an external ground, as an additional input terminal v_{REF} of the amplifier circuit. With Z_{out} denoting the amplifier's output impedance, the gain from this newly introduced terminal to the output is then seen to be $A_{\text{ref}}(s) = Z_{\text{out}}/(Z_{L0} + Z_{\text{out}})$. Inserting this into (5) leads to

$$A_{cm}(s) + A_{dd}(s) + A_{ss}(s) = \frac{Z_{L0}}{Z_{L0} + Z_{\text{out}}}, \quad (6)$$

which generalizes (3) for loaded amplifiers. Equation (6) easily transforms into (1a) when it is rewritten in terms of the differential gain and the rejection ratios.

Operational Amplifiers with Differential Outputs. For differential-output operational amplifiers there are parasitic gains from the common-mode input and the supply inputs to the differential-mode output as well as to the common-mode output voltage. Denoting by $A_i^o(s)$, $i \in \{cm, dd, ss\}$ and $o \in \{dm, cm\}$, the gains from the inputs i to the outputs o , the following two relationships between the parasitic gains are valid:

$$A_{cm}^{dm}(s) + A_{dd}^{dm}(s) + A_{ss}^{dm}(s) = 0, \quad (7a)$$

$$A_{cm}^{cm}(s) + A_{dd}^{cm}(s) + A_{ss}^{cm}(s) = 1. \quad (7b)$$

From (7) it is seen that the gains to the *differential*-mode output, $A_i^{dm}(s)$, can individually become zero, but that at least one of the gains to the *common*-mode output, $A_i^{cm}(s)$, must be nonzero.

Operational Amplifiers with Balanced Outputs. Balanced-output amplifiers are amplifiers with differential outputs that have an additional input, v_{BAL} , to control the common-mode output voltage v_{OCM} . With a notation corresponding to that used in (7), the parasitic gain relationships for these amplifiers are

$$A_{cm}^{dm}(s) + A_{dd}^{dm}(s) + A_{ss}^{dm}(s) + A_{bal}^{dm}(s) = 0, \quad (8a)$$

$$A_{cm}^{cm}(s) + A_{dd}^{cm}(s) + A_{ss}^{cm}(s) + A_{bal}^{cm}(s) = 1 \quad (8b)$$

where $A_{bal}^o(s)$, $o \in \{dm, cm\}$ denote the gains from the balance input to the respective outputs. Usually $A_{bal}^{cm}(s)$ is set to unity (the common-mode output voltage v_{OCM} tracks the balance signal v_{BAL}), allowing the remaining parasitic gains in (8b) to become zero individually. As is shown by Example 5 in Section III, the gains $A_{cm}^{cm}(s)$, $A_{dd}^{cm}(s)$, and $A_{ss}^{cm}(s)$ actually become very small for a practical amplifier with $A_{bal}^{cm}(s) \approx 1$. Even if the signal of only one output terminal is used against the reference v_{BAL} , an amplifier with a very good isolation of the supply terminal signals is obtained. This property holds in the frequency range where $A_{bal}^{cm}(s) \approx 1$, which extends for the considered example from dc to an upper frequency limit.

Differential Difference Amplifiers. The differential difference amplifier (DDA) described in [4] and [5] is an amplifier with four signal inputs designated v_{PP} , v_{PN} , v_{NP} , and v_{NN} , one signal output v_O , and two power supplies v_{DD} and v_{SS} . Ideally, it amplifies the difference between the *port* voltages $(v_{PP} - v_{PN})$ and $(v_{NP} - v_{NN})$, i.e. the differential signal $v_D \stackrel{\text{def}}{=} (v_{PP} - v_{PN}) - (v_{NP} - v_{NN})$, and suppresses the three common-mode signals $v_{CP} \stackrel{\text{def}}{=} (v_{PP} + v_{PN})/2$, $v_{CN} \stackrel{\text{def}}{=} (v_{NP} + v_{NN})/2$, and $v_{CN} \stackrel{\text{def}}{=} [(v_{PP} - v_{PN}) + (v_{NP} - v_{NN})]/2$. For this amplifier the relationship between the (small-signal) parasitic gains is

$$A_{cp}(s) + A_{cn}(s) + A_{dd}(s) + A_{ss}(s) = 1 \quad (9)$$

where $A_i(s)$, $i \in \{cp, cn, dd, ss\}$, denote the gains from the respective input to the output. Note that the gain from the common-mode voltage v_{cd} , $A_{cd}(s)$, does not enter into

the relationship. As for the simple operational amplifier (cf. (3)), at least one of the parasitic gains in (9) must be nonzero.

III. DISCUSSION AND EXAMPLES

In the following we illustrate our result with specific circuit examples, and discuss principles which aim to improve the rejection of parasitic signals. Because the relationship is simpler in terms of gains than in terms of rejection ratios, most of the discussion is in terms of gains and we take care that the differential gains of compared amplifiers are equal. Except for Example 1, which analytically demonstrates the basic relationship (6), our examples fulfill $|Z_{out}/Z_{L0}| \ll 1$ in the relevant frequency ranges. Thus the terms that account for nonzero output impedances are unessential, and the simplified relationship given in Section II applies.

As mentioned above it is according to (3) *not possible* to design a simple operational amplifier that has all parasitic gains, i.e., the common-mode gain and power-supply gains, equal to zero. Therefore, the frequently used assumption for ideal operational amplifier models that *only* the differential signal is amplified is *physically impossible*.

We further conclude that if there is no power-supply dependence of the output, the common-mode gain must be unity, or, stated otherwise, the common-mode rejection ratio and the differential gain must be identical.¹ Tracking effects of this kind are frequently observed in operational amplifiers. Note that (4) is a relationship among complex-valued functions; data sheets of actual amplifiers, however, specify only the *magnitudes* of the differential gain and the rejection ratios. By applying the triangle inequality to (4), four relations among the corresponding frequency-response magnitudes are obtained which imply various tracking effects.² Example 2 below illustrates tracking for a practical amplifier.

The relationship (3) developed in Section II and its extension to amplifiers with an additional input terminal that allows for the reduction of the parasitic gains is now illustrated by some practical examples.

While the first example illustrates (3) by analytical expressions for the various gains of a simple buffered differential amplifier, the next example concerns the SPICE simulation of the gains of a two-stage general purpose operational amplifier proposed in the literature [6]. Examples 3 to 5

¹Of course, corresponding statements are true if two other parasitic gains are zero and, in turn, the rejection ratio of the remaining gain is identical to the differential gain.

²The relations are of the form $1/w \leq 1/x + 1/y + 1/z$ where w is one of the four parameters $|A_d(s)|$, $|CMRR(s)|$, $|PSRR^+(s)|$, and $|PSRR^-(s)|$, and x, y, z represent, for a selected w , the remaining parameters. From these inequalities we conclude that, at any given frequency, it is impossible for exactly *one* of the four parameters to be much worse (i.e. much lower) than the others, because each inverse parameter is upper bounded by the sum of the remaining inverse parameters. Furthermore, if *two* of the four parameters are much worse (i.e. much lower) than the others, this implies that the magnitudes of the latter parameters must be very similar. This is explained by the fact that according to the above inequalities these parameters are approximate upper bounds for each other. This tracking effect can be observed in many amplifier circuits in the mid-frequency range and is also found in the data sheets of many practical amplifiers.

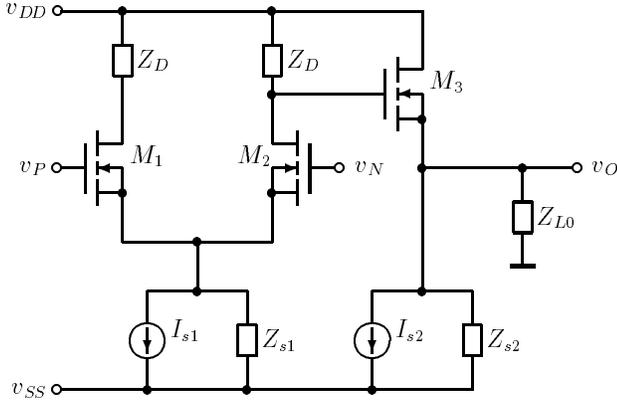


Fig. 1. Schematic of a simple MOS differential stage which is buffered by a source follower.

show three approaches for the reduction of the parasitic gains with the help of an additional terminal. Thereby, the Examples 3 and 4 use conventional single-ended amplifiers and obtain improved rejections in the mid frequency ranges. In contrast Example 5 makes use of a differential output structure and gives rejection improvements even down to dc. To compare the various amplifier circuits on the basis of gains (rather than on the basis of rejection ratios) the amplifier circuits in Examples 2 to 5 have been designed to have an equal differential gain of 85 dB. Finally, Example 6 compares these amplifiers in a negative feedback circuit and shows that the amplifier of Example 5 outperforms the other presented solutions.

Example 1 (Simple Amplifier) In order to illustrate (6) by analytic expressions we consider the simple differential stage with two load impedances Z_D buffered by a source follower as shown in Fig. 1. We assume that the MOS transistors are simply modeled by linear voltage-controlled current sources with real transconductances g_{m1} for the differential stage transistors and g_{m3} for the follower transistor, respectively. Then the relevant frequency responses are easily derived to be

$$\begin{aligned} A_d(s) &= g_{m1}g_{m3} \frac{Z_D}{2} \frac{Z_{L0}Z_{out}}{Z_{L0} + Z_{out}}, \\ A_{cm}(s) &= -g_{m1}g_{m3} \frac{Z_D}{1 + 2g_{m1}Z_{S1}} \frac{Z_{L0}Z_{out}}{Z_{L0} + Z_{out}}, \\ A_{dd}(s) &= g_{m3} \frac{Z_{L0}Z_{out}}{Z_{L0} + Z_{out}}, \\ A_{ss}(s) &= \left(g_{m1}g_{m3} \frac{Z_D}{1 + 2g_{m1}Z_{S1}} + \frac{1}{Z_{S2}} \right) \frac{Z_{L0}Z_{out}}{Z_{L0} + Z_{out}} \end{aligned} \quad (10)$$

where the output impedance is $Z_{out} = Z_{S2}/(1 + g_{m3}Z_{S2})$. Substituting the frequency responses given in (10) for the corresponding variables in (6) shows that the derived relationship is actually fulfilled. \square

Example 2 (Two Stage Op Amp) Whereas the above example, made for analytical demonstration purposes only, could be considered an oversimplification, the next example is closer to practice. It is the first example in a series which

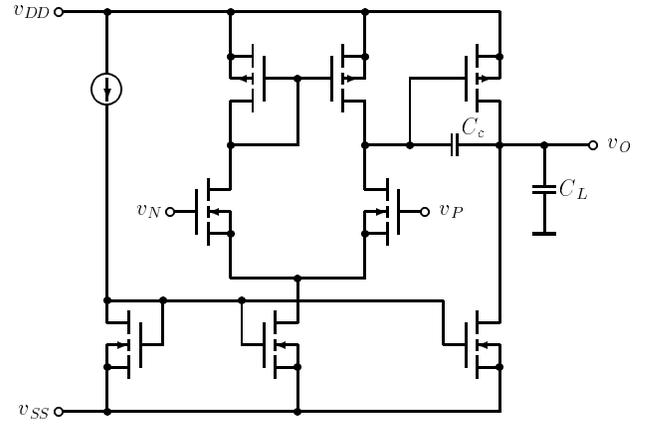


Fig. 2. Schematic of a two stage CMOS operational amplifier with n-channel input pair (from [6, Fig. 8.3-2]).

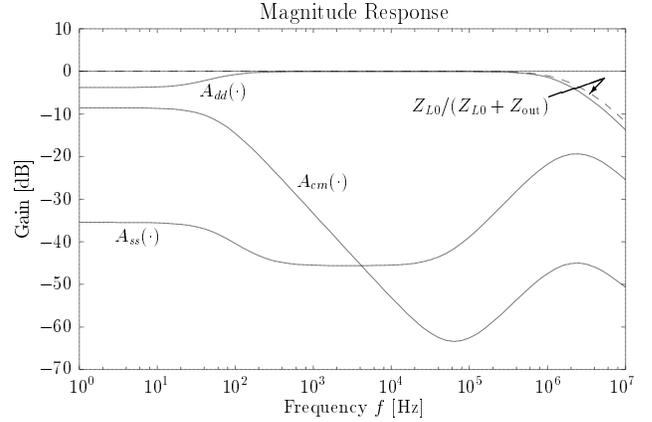


Fig. 3. Magnitude responses of the common-mode gain $A_{cm}(\cdot)$, the positive power-supply gain $A_{dd}(\cdot)$, and the negative power-supply gain $A_{ss}(\cdot)$ for the two stage op amp of Fig. 2. Also shown is the term $|Z_{L0}/(Z_{L0} + Z_{out})|$ (dashed line) which indicates that its value is close to unity below 100 kHz justifying the use of the simplified equations (3) or (4).

illustrate some improvement strategies that are based on our relationship. Instead of symbolically computing the relevant frequency responses we have now to resort to numerical computations.

We consider the two stage CMOS operational amplifier, taken from [6, p. 396], which is shown in Fig. 2 and consists of a differential stage cascaded with an integrator. A SPICE computation of all parameters in relationship (6) for the component values of the design example in [6, pp. 393 ff.] numerically confirms our relationship. The frequency dependence of the parameters involved in (6) are plotted in Fig. 3. The most interesting feature in these plots is that $A_{dd}(\cdot)$ is approximately equal to unity over a broad frequency range which corresponds to a close tracking of the differential gain and the positive power-supply rejection ratio. The weak positive supply rejection illustrated by these curves is well known in operational amplifier practice (cf. e.g. [8]) and is attributed to the virtual ground at the integrator input which tracks the changes of the positive supply voltage v_{DD} . These variations are fully transferred to the

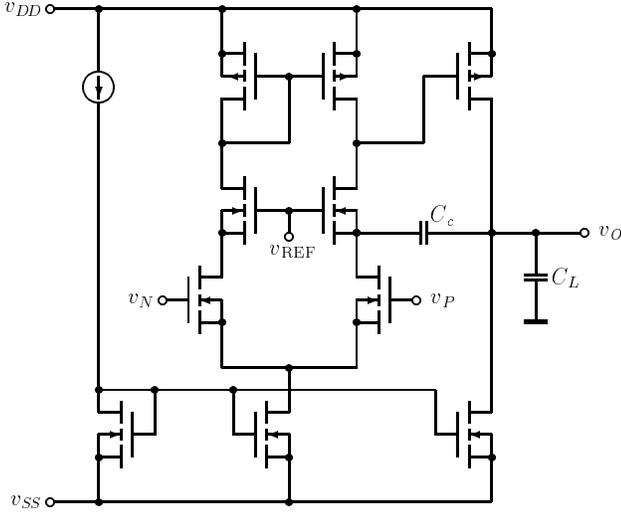


Fig. 4. Schematic of a cascode CMOS operational amplifier using an auxiliary terminal (from [3, Fig. 2]).

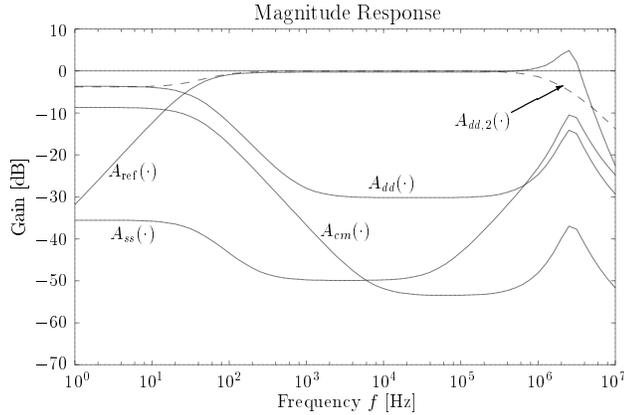


Fig. 5. Magnitude responses of the common-mode gain $A_{cm}(\cdot)$, the gain from the reference terminal $A_{ref}(\cdot)$, the gain from the positive power-supply $A_{dd}(\cdot)$, and the gain from the negative power-supply $A_{ss}(\cdot)$ for the cascode op amp of Fig. 4. For comparison, the positive power-supply gain that results for the original operational amplifier of Fig. 2 is also shown by the curve labeled $A_{dd,2}(\cdot)$ (dashed line).

output through the integrator capacitor C_c and the integrator load at medium and high frequencies. The observation of $A_{dd}(\cdot) \approx 1$ and low values of the $A_{cm}(\cdot)$ and $A_{ss}(\cdot)$ is consistent with our relationship (3). \square

The following Examples 3 and 4 illustrate ways to improve the positive supply rejection through the introduction of a supplementary control terminal as indicated in the above discussion.

Example 3 (Cascode Op Amp) In the circuit illustrated in Fig. 4 the return point of the integrator capacitor C_c is isolated from the positive supply terminal by a common gate stage as proposed in [3, Fig. 2]. In the mid-frequency range the “ $A_{dd}(\cdot) \approx 1$ path” of the circuit in Fig. 2 is now replaced by a path with an $A_{ref}(\cdot) \approx 1$ transfer function from the gate of the common-gate stage to the output. This is the necessary condition for low values of the other parasitic gains $A_{dd}(\cdot)$, $A_{ss}(\cdot)$, and $A_{cm}(\cdot)$. The results of

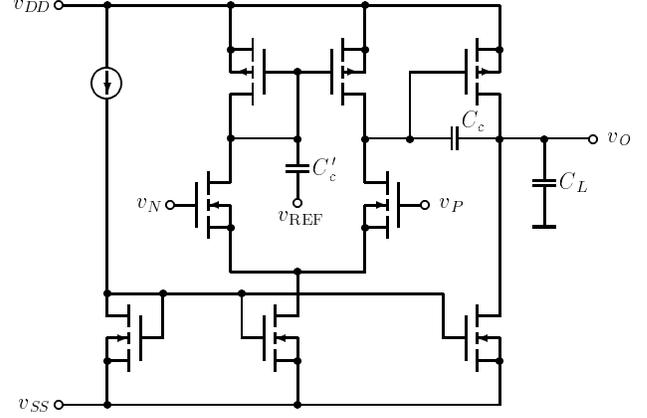


Fig. 6. Schematic of a current injection CMOS operational amplifier using an auxiliary terminal.

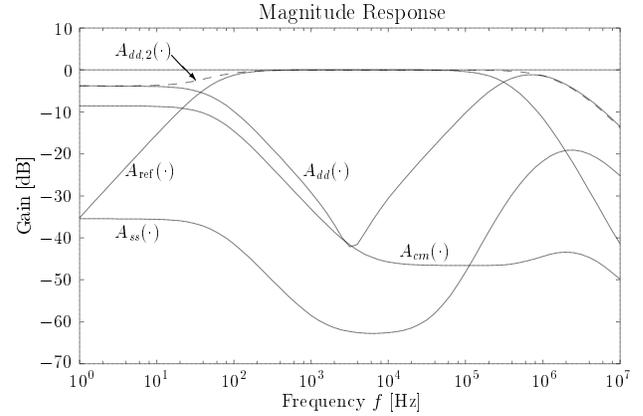


Fig. 7. Magnitude responses of the common-mode gain $A_{cm}(\cdot)$, the gain from the auxiliary terminal $A_c(\cdot)$, the gain from the positive power-supply $A_{dd}(\cdot)$, and the gain from the negative power-supply $A_{ss}(\cdot)$ for the current injection op amp of Fig. 6. For comparison, the positive power-supply gain that results for the original operational amplifier of Fig. 2 is also shown by the curve labeled $A_{dd,2}(\cdot)$ (dashed line).

a simulation in Fig. 5 show that this goal is achieved by this circuit modification. We recall that connecting the reference terminal to a noise-free voltage source does not add any disturbing signal component to the output signal although the gain $A_{ref}(\cdot)$ is near to unity. We note, however, that this cascode structure (cf. Fig. 4) requires an additional noise-free dc supply and has the disadvantage of limiting the input common-mode voltage range. \square

Example 4 (Current Injection Op Amp) An alternative method for the creation of a “gain one path” from a supplementary terminal to the output is shown in Fig. 6. Connecting a capacitor C'_c from the input of the current mirror to ground in the classical two stage operational amplifier of Fig. 2 is an easily applicable solution to the problem which does not influence the common-mode voltage range and does not require a supplementary dc supply. In this configuration, C'_c injects a correction current via the current mirror into C_c which compensates for the variations at the integrator input with v_{DD} . By choosing $C'_c \equiv C_c$ an idealized model of the path from

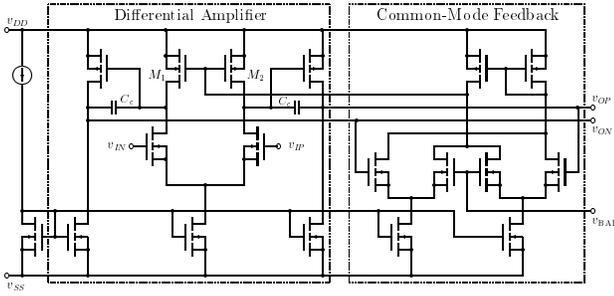
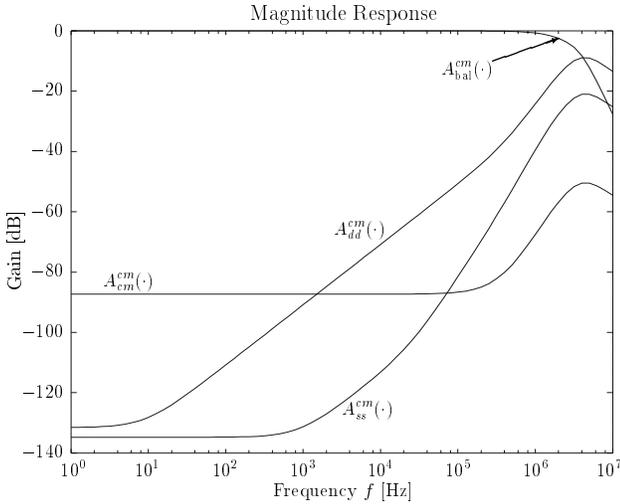


Fig. 8. Schematic of a balanced-output CMOS operational amplifier.

Fig. 9. Magnitude responses of the common-mode gain $A_{cm}^{cm}(\cdot)$, the gain from the balance terminal $A_{bal}^{cm}(\cdot)$, the gain from the positive power-supply $A_{dd}^{cm}(\cdot)$, and the gain from the negative power-supply $A_{ss}^{cm}(\cdot)$ for the balanced-output op amp of Fig. 8.

the ground (reference) terminal to the output leads to $A_{ref}(s) = (s/p_d)/[(1 + s/p_d)(1 + sC_c/g_m)]$ where p_d denotes the amplifier's dominant pole magnitude and g_m the current-mirror transconductance. Small values of the other parasitic gains in the frequency interval limited by p_d and g_m/C_c are now possible according to (5). SPICE simulations of the respective circuit shown in Fig. 7 illustrate that in the mid-frequency range where the gain from the reference terminal approaches unity, the positive power supply rejection is substantially improved (i.e. the gain $A_{dd}(\cdot)$ is lowered). The frequency range for A_{dd} -suppression can be enlarged by enlarging the current-mirror transconductance g_m as is seen from the above expression for $A_{ref}(\cdot)$. \square

Our next example proposes a fully differential amplifier with a balanced-output, similar to [9], to improve the rejection of parasitic signals.

Example 5 (Balanced Output Op Amp) The circuit design starts from the original differential amplifier of Fig. 2 and symmetrically applies this design to a balanced-output amplifier. The common-mode output voltage is regulated with a differential difference amplifier (DDA) [4] [5] to an external voltage v_{BAL} by sensing the two differential output lines. The obtained circuit is shown in Fig. 8. The resulting common-mode gains shown in Fig. 9 indicate that $A_{bal}^{cm}(\cdot)$ is unity over a broad frequency range which, in con-

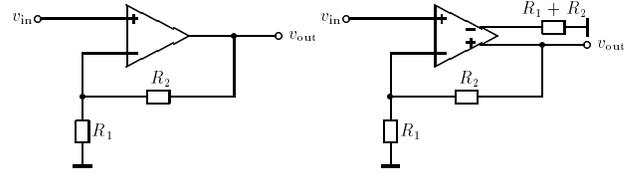


Fig. 10. Non-inverting amplifier configurations.

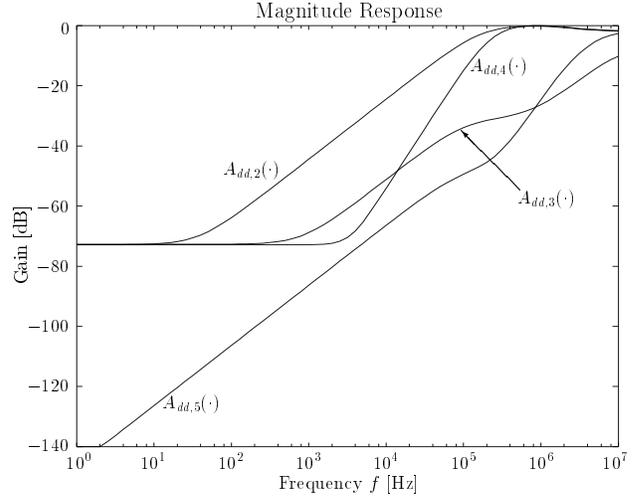


Fig. 11. Magnitude responses of the positive power-supply gains in the non-inverting amplifier of Fig. 10. The subscripts indicate the number of the example where the amplifier is introduced.

trast to the single-ended counterparts of the cascode and current-injection operational amplifier, extends down to dc. It forces the remaining parasitic gains $A_{cm}^{cm}(\cdot)$, $A_{dd}^{cm}(\cdot)$, and $A_{ss}^{cm}(\cdot)$ to very small values in this broad frequency range. The differential output signal is almost completely independent of the supply and common-mode voltages in this fully symmetric circuit, which means that the gains $A_i^{dm}(\cdot)$, $i \in \{cm, dd, ss\}$, are practically zero. Furthermore, the parasitic gains with respect to a *single-ended output* (one of the output lines with respect to v_{BAL}) are significantly improved as compared to the cascode and current injection operational amplifier examples. Like the current-injection operational amplifier, correction currents are supplied to the integrator capacitors C_c in order to compensate for the variations of the integrator inputs at v_{DD} . However, in this case the currents are supplied by the current sources M_1 and M_2 which are controlled by the common-mode feedback circuit. \square

Example 6 (Closed Loop Circuits) We use the amplifiers presented in the Examples 2, 3, 4, and 5 in a non-inverting, single-ended, amplifier configuration with feedback as shown in Fig. 10, and compare their power-supply rejection performance. Note that the amplifier load of the balanced-output amplifier is reproduced at the nonused output terminal. The SPICE simulations of the resulting gains from the positive power supply in Fig. 11 clearly indicate that the balanced-output amplifier of Example 5 outperforms the other amplifier designs. Similar results have been obtained for the gains from the negative power supply

but are not presented here because in the considered amplifiers the negative power supply rejection is less critical. \square

IV. SUMMARY AND CONCLUSIONS

We have shown that a constraint exists for the gains which are measured between the input terminals of an amplifier and its outputs. Applied to a simple operational amplifier with a differential input, two supply terminals and one output, this means that a relationship exists between the so called parasitic gains (i.e. the common-mode gain and the gains from the supply terminals to the output): their sum approaches unity in practical circuits. Therefore, supply- and common-mode rejection ratios cannot simultaneously assume high values. This conclusion is confirmed by practical operational amplifier designs where usually one of the supply terminals is critical and exhibits a relatively high parasitic transfer to the output. Our derivation of the presented general relationship is based on the physical law of gauge invariance of the electrical potential.

Adding to the amplifier circuit a supplementary reference terminal which is connected to a noise-free voltage and the use of differential-output structures adds a degree of freedom to the above mentioned gain relationship and can be used to maximize common-mode and power-supply rejection simultaneously. The practical use of this idea is demonstrated with four different implementations of a basic two-stage CMOS operational amplifier. Designing the supplementary terminal such that its transfer to the output is unity increases the supply rejection of the critical terminal. While two of the presented designs show this improvement only in the mid-frequency range, a differential-output amplifier with common-mode feedback exhibits this favorable property down to dc even when used as a single-ended output amplifier. Adding an external feedback to these amplifiers conserves the improvement of the open-loop performance as is demonstrated with a noninverting amplifier configuration.

Whereas we have mainly considered amplifiers with two signal inputs, we would like to point out that the results are more general. Moreover, generalizations with respect to the number of power-supply lines and output terminals are straightforward and we expect that our ideas are applicable to other circuit configurations as well.

APPENDIX

APPENDIX: DERIVATION OF THE GENERAL RELATIONSHIP

An easy way to establish the relationships in Section II is to use a gauge-invariance argument to obtain the relationship for a more general situation which can easily be specialized for the needed amplifier types. This is best done in a vector-space formalism. To avoid confusion with the electrical notation-conventions we represent the arising vectors by a symbol delimited by a left vertical bar and a right angular bracket (e.g. $|a\rangle$).³ The special vector $(1, 1, \dots, 1)^T$

is denoted $|\mathbf{1}\rangle$. Matrices are written as upper case, bold face symbols; the identity matrix being \mathbf{I} . The following general proof is illustrated with the differential-output operational amplifier as an example after each intermediate step.

The considered amplifier circuits have a number of input-terminals the voltages of which are collected in the terminal-voltage input vector $|\mathbf{v}_{IT}\rangle$. To be able to describe the effects of nonideal (time varying) power supplies, this vector contains, besides the signal voltages also the power supply voltages. Correspondingly, the output voltages are collected in the terminal-voltage output vector $|\mathbf{v}_{OT}\rangle$. For the amplifiers of Section II this vector contains a single voltage in the case of single-ended amplifiers or a pair of voltages in the case of differential-output amplifiers.

Generally, the transfer function from the input, $|\mathbf{v}_{IT}\rangle$, to the output, $|\mathbf{v}_{OT}\rangle$, of an amplifier circuit is specified by a set of nonlinear differential equations of the input and the output variables. Because we are interested in the amplifier's approximate linear behavior which results for small input-voltage variations when the amplifier circuit is biased into an operating point, we introduce the corresponding small-signal quantities (operating point quantities subtracted) transformed to the frequency domain: $|\mathbf{V}_{it}(s)\rangle$ and $|\mathbf{V}_{ot}(s)\rangle$. The amplifier could now be characterized by a gain matrix summarizing the gains from the input-terminal to the output-terminal voltages. However, it is common practice to specify the gains between the input and output *mode voltages* rather than the terminal voltages; thus we have

$$\mathbf{M}_O|\mathbf{V}_{ot}\rangle = \mathbf{A}(s)\mathbf{M}_I|\mathbf{V}_{it}\rangle. \quad (11)$$

The matrices \mathbf{M}_I and \mathbf{M}_O transform the terminal voltages to mode voltages and $\mathbf{A}(s)$ is the matrix containing the mode gains.

Example: The notation is clarified with the example of the differential-output operational amplifier. This amplifier has two signal inputs, v_{IP} and v_{IN} , and two power-supply inputs, v_{DD} and v_{SS} , thus the input vector has four components. There are two outputs, v_{OP} and v_{ON} . Equation (11) then specializes to

$$\begin{pmatrix} 1 & -1 \\ 1/2 & 1/2 \end{pmatrix} \cdot \begin{pmatrix} V_{op} \\ V_{on} \end{pmatrix} = \begin{pmatrix} A_{dm}^{dm}(s) & A_{cm}^{dm}(s) & A_{dd}^{dm}(s) & A_{ss}^{dm}(s) \\ A_{dm}^{cm}(s) & A_{cm}^{cm}(s) & A_{dd}^{cm}(s) & A_{ss}^{cm}(s) \end{pmatrix} \cdot \begin{pmatrix} 1 & -1 & 0 & 0 \\ 1/2 & 1/2 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} V_{ip} \\ V_{in} \\ V_{dd} \\ V_{ss} \end{pmatrix}.$$

The matrices \mathbf{M}_I and \mathbf{M}_O transform the terminal input and output signals into differential-mode and common-mode signals, while the power-supply voltages are used directly. The gain matrix contains eight values, only the one relating the input differential mode with the output differential mode, $A_{dm}^{dm}(s)$, is desired. \square

³This is Dirac's bra-ket notation, cf. [10, p.18], [11, p.7].

If we shift the origin of the potential scale of (11) by adding a gauge signal $V_{\text{gauge}}(s) \bullet \bullet v_{\text{gauge}}(t)$, we obtain $\mathbf{M}_O(|\mathbf{V}_{ot}\rangle + V_{\text{gauge}}|\mathbf{1}\rangle) = \mathbf{A}(s)\mathbf{M}_I(|\mathbf{V}_{it}\rangle + V_{\text{gauge}}|\mathbf{1}\rangle)$. We subtract from the new equation the original equation and make use of the fact that $V_{\text{gauge}}(s) \bullet \bullet v_{\text{gauge}}(t)$ is an arbitrary small-signal⁴ voltage. The resulting general relationship in vector notation is

$$\mathbf{A}(s)\mathbf{M}_I|\mathbf{1}\rangle = \mathbf{M}_O|\mathbf{1}\rangle. \quad (12)$$

Example: For the differential-output operational amplifier relationship (12) becomes

$$\begin{pmatrix} A_{dm}^{dm}(s) & A_{cm}^{dm}(s) & A_{dd}^{dm}(s) & A_{ss}^{dm}(s) \\ A_{dm}^{cm}(s) & A_{cm}^{cm}(s) & A_{dd}^{cm}(s) & A_{ss}^{cm}(s) \end{pmatrix} \cdot \begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \end{pmatrix}$$

where the two vectors are obtained by summing the column vectors of the corresponding mode matrices \mathbf{M}_I and \mathbf{M}_O . Rewriting the equation in scalar notation yields (7). \square

The above relationship is correct for any output loads connected to v_{DD} and v_{SS} . In practice, however, the gains are measured for an external reference load connected between the outputs of the amplifier and a noise-free ground voltage V_{gg} . In this case the whole system, amplifier and load, can be viewed as a circuit having one more input terminal than the amplifier alone, namely the ground terminal. Thus the relationship between the gains measured with an external load can be obtained by extending the formula for the V_{gg} input and calculating the corresponding transfer functions, $|\mathbf{A}_{gg}\rangle$, from this input to all outputs.

Equation (11), extended for the ground terminal, reads $\mathbf{M}_O|\mathbf{V}_{ot}\rangle = \mathbf{A}(s)\mathbf{M}_I|\mathbf{V}_{it}\rangle + \mathbf{M}_O|\mathbf{A}_{gg}\rangle V_{gg}$. If \mathbf{Y}_{L0} denotes the load admittance matrix and \mathbf{Z}_{out} the output-impedance matrix of the amplifier, we obtain the additional gains as $|\mathbf{A}_{gg}\rangle = [\mathbf{I} - (\mathbf{I} + \mathbf{Z}_{\text{out}}\mathbf{Y}_{L0})^{-1}]|\mathbf{1}\rangle$. Performing the gauge transformation and subsequent derivations as carried out above for this extended equation leads to the final and most general relationship presented in this paper:

$$\mathbf{A}(s)\mathbf{M}_I|\mathbf{1}\rangle = \mathbf{M}_O(\mathbf{I} + \mathbf{Z}_{\text{out}}\mathbf{Y}_{L0})^{-1}|\mathbf{1}\rangle. \quad (13)$$

If we have $(\mathbf{I} + \mathbf{Z}_{\text{out}}\mathbf{Y}_{L0}) \approx \mathbf{I}$ in the relevant frequency ranges, the gains for load and the gains for no load do not differ by much and we can use the simpler relationship (12). For single-ended amplifiers the matrices \mathbf{Z}_{out} and \mathbf{Y}_{L0} degenerate to scalars and the correction term in (13) is $1/(1 + Z_{\text{out}}Y_{L0}) = Z_{L0}/(Z_{L0} + Z_{\text{out}})$ as in (6).

Example: For our example with the differential output operational amplifier we assume that the two outputs are independent and that each output is loaded with a separate load Z_{L1} and Z_{L2} . Thus the output-impedance matrix and the load-admittance matrix are

$$\mathbf{Z}_{\text{out}} = \begin{pmatrix} Z_{O1} & 0 \\ 0 & Z_{O2} \end{pmatrix}, \quad \mathbf{Y}_{L0} = \begin{pmatrix} 1/Z_{L1} & 0 \\ 0 & 1/Z_{L2} \end{pmatrix}.$$

⁴There is actually no constraint with respect to the amplitude of the gauge signal, since it does not disturb the operating point.

Specializing (13) for the differential-output operational amplifier and the above load situation yields the following vector equation

$$\begin{pmatrix} A_{dm}^{dm}(s) & A_{cm}^{dm}(s) & A_{dd}^{dm}(s) & A_{ss}^{dm}(s) \\ A_{dm}^{cm}(s) & A_{cm}^{cm}(s) & A_{dd}^{cm}(s) & A_{ss}^{cm}(s) \end{pmatrix} \cdot \begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \end{pmatrix} = \begin{pmatrix} 1 & -1 \\ 1/2 & 1/2 \end{pmatrix} \begin{pmatrix} \frac{Z_{L1}}{Z_{L1} + Z_{O1}} & 0 \\ 0 & \frac{Z_{L2}}{Z_{L2} + Z_{O2}} \end{pmatrix} \begin{pmatrix} 1 \\ 1 \end{pmatrix}.$$

Rewritten in scalar notation this is

$$A_{cm}^{dm}(s) + A_{dd}^{dm}(s) + A_{ss}^{dm}(s) = \frac{Z_{L1}}{Z_{L1} + Z_{O1}} - \frac{Z_{L2}}{Z_{L2} + Z_{O2}},$$

$$A_{cm}^{cm}(s) + A_{dd}^{cm}(s) + A_{ss}^{cm}(s) = \frac{1}{2} \left(\frac{Z_{L1}}{Z_{L1} + Z_{O1}} + \frac{Z_{L2}}{Z_{L2} + Z_{O2}} \right).$$

Note that in order for the differential-output gain terms to become zero (first equation) the combination of load and output impedance has to fulfill certain symmetry conditions, also compare Example 6. \square

Instead of the parasitic gains used above, common-mode and power-supply rejection ratios are sometimes more practical. The relationships (12) and (13) can easily be transformed into equations of rejection ratios by dividing the whole equation by the desired (non-parasitic) gain. In our example of the differential-output operational amplifier this gain is $A_{dm}^{dm}(s)$. Furthermore, it is straightforward to specialize the general formula (12) for the amplifier types presented in Section II.

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REFERENCES

- [1] Aaron Fialkow and Irving Gerst. The transfer function of general two terminal-pair rc networks. *Quarterly of Applied Mathematics*, X(1):113–127, April 1952.
- [2] Dan Hilberman. Input and ground as complements in active filters. *IEEE Trans. Circuits Syst.*, CT-20(5):540–547, September 1973.
- [3] David B. Ribner and Miles A. Copeland. Design techniques for cascaded CMOS op amps with improved PSRR and common-mode input range. *J. Solid-State Circuits*, SC-19(6):919–925, December 1984.
- [4] Eduard Säckinger and Walter Guggenbühl. A versatile building block: The CMOS differential difference amplifier. *J. Solid-State Circuits*, SC-22(2):287–294, April 1987.
- [5] Eduard Säckinger. Theory and monolithic CMOS integration of a differential difference amplifier. In W. Fichtner, W. Guggenbühl, H. Melchior, and G. S. Moschytz, editors, *Series in Microelectronics, Vol. 1*. Hartung-Gorre Verlag, Konstanz, Germany, 1989.
- [6] Phillip E. Allen and Douglas R. Holberg. *CMOS Analog Circuit Design*. Holt, Rinehart and Winston, New York, 1987.
- [7] John David Jackson. *Classical Electrodynamics*. John Wiley & Sons, 2nd edition, 1962.

- [8] Paul R. Gray and Robert G. Meyer. MOS operational amplifier design — a tutorial overview. *J. Solid-State Circuits*, SC-17(6):969–982, December 1982.
- [9] Sudhir M. Mallya and Joseph H. Nevin. Design procedures for a fully differential folded-cascode CMOS operational amplifier. *J. Solid-State Circuits*, SC-24(6):1737–1740, December 1989.
- [10] Paul A. M. Dirac. *The Principles of Quantum Mechanics*. Oxford University Press, 4 edition, 1958.
- [11] Stephen B. Haley and Karl Wayne Current. Response change in linearized circuits and systems: Computational algorithms and applications. *Proc. IEEE*, Vol. 73(1):5–24, January 1985.

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