A DUAL 3.4V BITSTREAM CONTINUOUS CALIBRATION CMOS D/A CONVERTER WITH 110DB DYNAMIC RANGE

D.W.J. Groeneveld and H.J. Schouwenaars

Philips Research Laboratories, The Netherlands

ABSTRACT

A new generation D/A converter is presented, combining a true 18-bit dynamic range with easy application. This is achieved by introducing oversampling to 96 f_s , digital filtering and noise-shaping. The actual digital-to-analogue conversion is done by a continuously calibrated current D/A converter on the same die. System and circuit design are both optimised to avoid degradation of the analogue performance by digital circuit noise.

1. INTRODUCTION

The required dynamic range of digital audio systems is expanding due to digital signal processing facilities such as tone and volume control. The translation to the analogue domain therefore requires D/A converters featuring high linearity and 18 to 20-bit dynamic range. These converters must succeed in providing such performance in a primarily digital environment while at the same time allowing simple application at low cost.

Bitstream techniques incorporating oversampling, noiseshaping and 1-bit D/A conversion have proven capable of realising superior small signal reproduction (Naus et al (1)). However, single-bit bitstream conversion requires high-order noiseshaping to shift the huge levels of quantisation noise out of the audio band. This massive high frequency noise necessitates high-order but still phase-linear analogue postfiltering which in turn entails relatively costly external circuitry and difficult application. Furthermore this noise can cause intermodulation distortion in the audio band so that the dynamic range which can be actually realised is limited especially in a mixed analog-digital environment.

In this paper, a dual 5-bit bitstream conversion system on a single IC is presented, in which the level of quantisation noise is reduced significantly compared to a one-bit system. The D/A converter is build up bidirectionally and uses current calibration. These system choices and special measures in digital and analogue design result in a high dynamic range and a high linearity without thee need for heavy postfiltering.

2. SYSTEM CONSIDERATIONS

The high requirements for a D/A converter suited for digital signal processing require a careful choice of the converter architecture. Conventional binary weighted converters (Schouwenaars et al (2)) are not suitable because of their poor low signal level behaviour, originating from correlation between signal and quantisation errors when the signal is represented by just a few bits. The well-known bitstream technique in which the original input signal undergoes oversampling and noise shaping does have an obvious advantage concerning low level signal linearity (Naus et al (1)) because of its inherently high differential linearity .

From an applicational point of view, both types of converter have disadvantages. Conventional D/A converters produce spectral components around multiples of the sampling frequency, which must be suppressed by high-order analogue postfiltering. Since the analogue postfilter should also preserve phase linearity, its design is complicated, requires many components and is thus costly.

In bitstream systems, heavy analogue postfiltering is still needed since the enormous quantisation noise of the one-bit quantiser is pushed to high frequencies by the noise-shaper. This is depicted in figure 1a, showing the output spectrum of a 3rd order noise-shaper operating at 5.6 MHz.

Another disadvantage of the 1-bit system is the large susceptibility for modulation of spurious signals back into the audio band by any nonlinearity in the back end of the conversion system, causing whizzles and frizzles in the output signal. Therefore, only a 2-chip solution is able to deliver a true 18-bit dynamic range (Kup et al (3)).

Application of a multi-bit oversampling D/A converter overcomes the problems stated earlier. An increase of the number of bits N creates more analogue levels, thus reducing the high-frequency noise energy and the interference susceptibility. At signal levels below -6N dB, the 1-bit system quality is maintained. The increase in analogue levels when going from 1 to more bits is not exactly linear due to the fact that 1-bit conversion means 2 analogue levels at the top and bottom of the full output range, while 2-bit conversion means 4 levels and a partitioning of the full-scale output range in three parts. Therefore, going from 1

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Table 1: Number of bits and resulting noise reduction

Number of bits	Noise reduction (dB)
1	0.0
2	9.5
3	16.9
4	23.5
5	29.8
6	36.0

to 2-bit yields a noise decrease of $20log3 = 9.5$ dB. In fact, the number of ranges in which a noiseshaper can operate is increased by a factor of $2^N - 1$. In table 1, the noise suppression factors are listed for a system up to 6 bits.

Application in an audio system requires suppression of out-of-band signals down to -35 dB. In the case of figure 1a, this would require a 5th order analogue output filter. By using a 5-bit approach, the analogue output filter demands are relaxed to just a first-order filter, which can easily be added in the output circuitry. The spectrum of a 5-bit system is shown in figure 1b. The problems of on-chip intermodulation

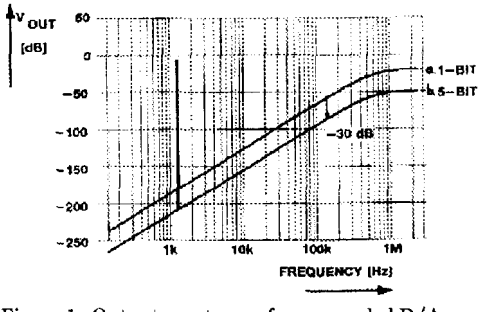

Figure 1: Output spectrum of oversampled D/A converter

are alleviated considerably in the multi-bit approach. However, one problem is left. Low signal levels are concentrated around half of the full-scale level. In unidirectional multi-bit converters this gives rise to noise and interference problems. Figure 2 shows the behaviour of an unidirectional D/A converter which is based on equal current sources. To generate the top of the sine wave, all available current sources are needed. To generate the lowest level of the sine wave, no current sources are needed. At the zero crossings half of all available current sources deliver output current. Thermal noise and substrate crosstalk components from digital circuits are present on these currents, thus restricting the dynamic range of the converter. A principle which is better suited to obtain a high dynamic range is called bidirectional current conversion, see figure 3. In this case, the input data

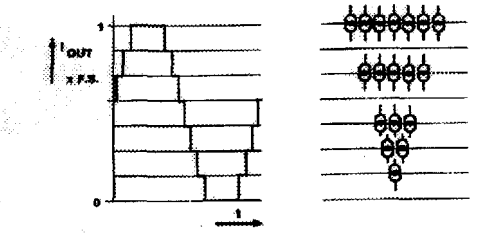

Figure 2: Unipolar current conversion

is converted into a bidirectional code which controls the switching of the current sources. In contradiction to the unidirectional conversion, two different types of current sources are needed. The top of the output sine wave in figure 3 is now called $+0.5F.S.$ and is generated by all sourcing current sources. The lowest part of the sine wave, now called $-0.5F.S.$ is generated by all sinking current sources. Small signal levels, located in the middle of the conversion range, are now generated by only one current source. This guarantees a much higher dynamic range than the unidirectional solution, at the cost of some decoding circuitry and the need for sinking and sourcing types of current sources. In the case of a 5-bit system, bidirectional encoding requires two complementary 4-bit D/A converters, as is shown in figure 4.

The choice for such a conversion setup gives rise to a much more complicated analogue part than the 1-bit case. Both 4-bit D/A converters must be linear, so accuracy in the analogue domain is again needed. Furthermore the current levels of both converters have to match exactly.

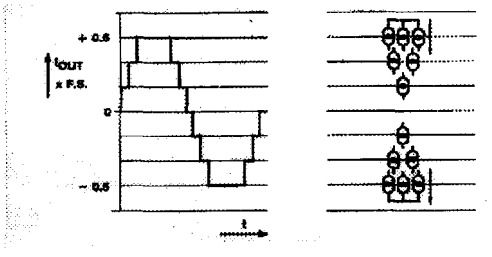

Figure 3: Bidirectional current conversion

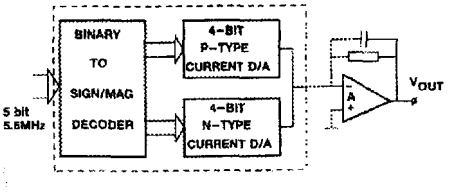

Figure 4: D/A Converter block diagram

3. DIGITAL PART

The digital part of the D/A converter is build up as follows. The digital input accepts four times oversampled serial input data. A 7th order FIR filter and a linear interpolator increase the oversampling rate to 16 times and remove the spectral components around 4fs, 8fs and 12fs. A sample-and-hold section further increases the sampling rate to 96 times and (together with the first order post-filtering) removes the spectral component around 16fs.
The second order noiseshaper converts the 18-bit data at 96fs to a 5-bit bitstream. This is indicated in figure 5. The dynamic range of this digital system is 115dB. The circuit is implemented in standard cell logic in a 1 μm CMOS process. Special precautions are taken in the digital part in order to prevent a too large voltage swing on the substrate, as will be discussed in the next section.

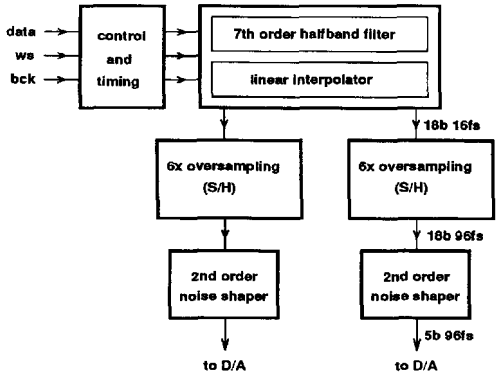

Figure 5: Digital part

4. SUBSTRATE VOLTAGE REDUCTION

Interference of the logic into the analogue circuits via the substrate is likely to be too high for two reasons. Firstly, the analogue noise level should be extremely low: 18-bit dynamic range means a total noise current of a few nA maximum. Secondly, the construction of the substrate implies a direct coupling between the digital and analogue parts, see figure 6. The CMOS substrate is basically split into two layers. The first is an epilayer of only a few (3...10) micrometers thickness having a relatively high resistance of about 10 Ohmcm. The remaining is a low-ohmic bulk of about 380 micrometer thickness and a resistance of only about 10 milliOhmcm or 0.3 Ohms per square. Therefore the bulk material can be approximated by a low ohmic plate, which is present below the digital as well as the analogue circuits.

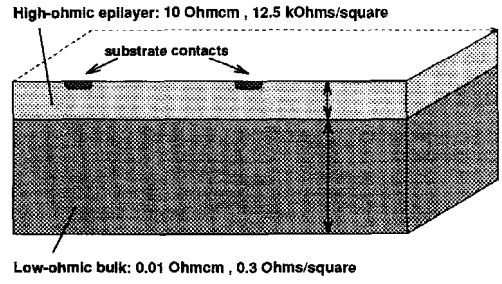

Figure 6: Simplified CMOS substrate cross section

Since most digital cells contain substrate contacts, the substrate voltage on the whole IC will be equal to the digital VSS voltage. Therefore, reduction of digital substrate noise has to be realised inside the digital circuit.
Analysis of the pollution of supply voltages by digital circuits (Su et al (4), Groeneveld (5)) learns that the parasitic inductances of bonding wires and package leads play a large role. Spike currents from digital circuitry which flow through the VSS pin of the IC create a voltage difference between PCB ground and the substrate. Secondly, the series resonance circuit which consists of inductance and resistance in the supply leads and internal capacitance can give problems. The quality of this circuit is defined as:

$$Q_s = \frac{1}{R_{dd} + R_{ss}} \sqrt{\frac{L_{dd} + L_{ss}}{C_{supply}}}$$

If the quality of this circuit is larger than 1, each current spike can cause a damped oscillation which may last until the next spike. This is not acceptable in the case of converters on the IC, because these should switch when the substrate voltage is not active. Q_s should therefore be reduced by increasing R_{dd} while keeping R_{ss} minimal. In this way, the resonance circuit is damped and the VSS and substrate voltages are close to the external ground voltage. Once the value of R_{dd} is increased, the internal capacitance C_{supply} can be increased to filter the current flowing to the outside even further. The digital part of this D/A converter does have an inherent capacitance C_{supply} of 360pF. The supply inductances equal 8nH each. For substrate noise suppression, additional internal capacitance was added to increase C_{supply} to 1 nF. An on-chip resistor of 30 Ohms in the digital supply line is added which results in $Q_s = 0.13$.

5. CURRENT CELL DESIGN

The analogue part of the D/A converter is based on continuous current calibration (Groeneveld et al (6), Schouwenaars et al (7)). This technique is capable of generating an arbitrary number of equal currents. The basic idea is the current copier, which is also the basic block in switched-current circuits. In this case, the input current is not fluctuating, but is well known. This enables an enhancement to the technique, which is shown in figure 7. In parallel to the

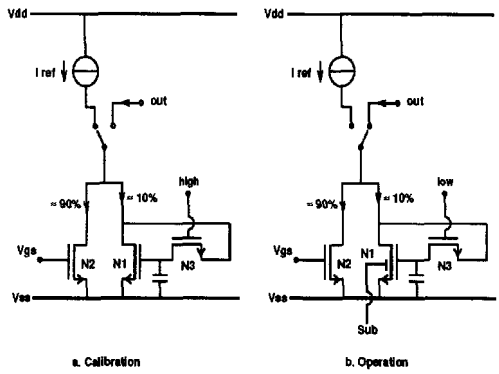

Figure 7: Current calibration technique

current memory transistor N1, a DC current source N2 is placed having a value of about 90% of the reference current. The current flowing through N1 is reduced 10 times and thus its sensitivity for charge injection from switch N3 is reduced. An important property of the basic current cell is its substrate sensitivity. Two effects cause coupling from the substrate into the output current during operation, see figure 7b. The first is the backgate conductance of the current memory transistor N1. Since the voltages at gate, source and drain are stable, the output current due to variations of the substrate equals $i_{ds1} = -g_{mb1}v_{sub}$. The second effect is parasitic coupling from the substrate to the gate of N1 via the drain to substrate diffusion of N3. This causes a residual voltage on the gate of N1 for all frequencies, which is transferred to the output current by N1's transconductance g_m. This effect is smaller than the backgate sensitivity and has an opposite sign. The total effect of the substrate to the output current therefore equals:

$$i_{ds} = -g_{mb1}v_{sub} + g_{m1}\frac{C_{db3}}{C_{gs1} + C_{db3}}v_{sub}$$

Using $I_{ds} = 5uA, W/L_{N1} = 10/10, W/L_{N3} = 1/1$ results in a total substrate transconductance of 10 uA/V. Assuming that 5 nA substrate noise is allowed, the substrate voltage swing must be smaller than 0.5 mV. This is far from reality, since up to hundreds of millivolts can be expected (Su et al (4), Groeneveld (5)). Consequently, an N-type current memory cannot be used in a mixed-mode IC.

The P-type current cell which is used in the D/A converter is shown in figure 8a. It uses a P-type current memory transistor P1, a P-type DC current source P2 and a p-type switch S1. For the generation of N-type equal currents without the use of an N-type current memory, the basic structure of the current cell is changed to the one in figure 8b. N1 acts as the DC current source, which is now set at about 110% of the reference current. This enables the use of a P-type current memory P1, which now carries the surplus of current coming from N1. The substrate sensitivity of N1 is of minor concern. This transistor is part of a current mirror, which is a differential structure with respect to substrate voltage.

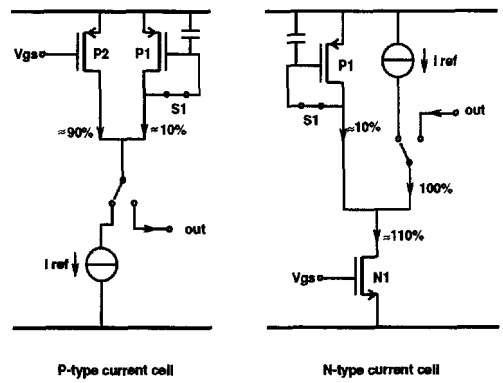

Figure 8: Current cells

6. D/A CONVERTER

Each 4-bit D/A converter is made by 15 current cells in parallel which deliver 15 equal output currents, see figure 9. The cells are calibrated one by one to the value of one single reference current. A spare cell is added which acts as a stand-in for a cell under calibration, so continuous operation of the converter is guaranteed. The calibration time for each current cell equals $1\mu s$.

To match the P-type and the N-type D/A converters, an adjustment loop is added which corrects the reference current of the N-type converter. For measurement of the current level difference between both converters, one more cell is added to each row of cells. The current levels of these 17th cells are compared by connecting the outputs to each other. The difference in current is integrated by means of an internal operational amplifier A_i and a capacitor C_i. The output voltage of the integrator is used to adjust the

reference current source $I_{ref,N}$. In this way, a continuous matching between P-type and N-type converter is guaranteed.
Finally, an amplifier converts the converter output current to a voltage signal capable of driving a line output. Internal reference circuitry ensures that the output signal is proportional to the supply voltage maintaining maximum dynamic range for supply voltages from 3.4V to 5.5V and making the circuit also suitable for battery-powered applications. The first-order postfiltering is realised by one external capacitor. This capacitor is connected in parallel to the internal resistor which is needed for I/V conversion .

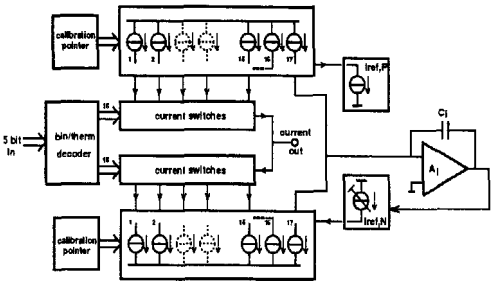

Figure 9: Block diagram of the analogue part

7. COMPLETE IC

A microphotograph of the complete IC is shown in figure 10. It incorporates the digital filtering and noise-shaping, two 5-bit D/A converters and two output amplifiers. Silicon area is 10 square millimeters in a 1 micrometer standard CMOS process. The IC uses 16 pins and three external capacitors. The supplies of the digital part, the analogue D/A and amplifiers are fully separated.

8. MEASUREMENT RESULTS

All presented results are measured unweighted true RMS over a bandwidth of 20kHz at a sampling frequency of 4.2MHz. Most of the converter specifications are listed in table 2.
Figure 11 shows a photograph of the typical output voltage of an oversampling multi-bit D/A converter. A sine-wave of 20kHz is generated at about -20dB compared to full-scale. As can be seen, four current levels are used. The noiseshaper always operates between two of those levels. The ratio between signal level and noise plus distortion components of this signal is 90 dB.
Figure 12 shows the measured S/(N+THD) as a function of output level of the converter. Up to -30 dB signal level, a 110 dB dynamic range is obtained.

Table 2: D/A converter specifications

supply voltage	3.4 to 5.5 V
output voltage at 5V	4.25 V_{pp}
S/(N+THD) at 0dB	90 dB
at -60dB	50 dB
sampling frequency	4.2 MHz
power dissipation at 5V	120 mW
temperature range	-30 to +85° C
process	1μm CMOS
active chip area	10 mm^2

At full-scale 90 dB is measured. Finally, the measured low-level linearity for both channels is shown in figure 13. Clearly, a true 18-bit linearity is obtained.

9. CONCLUSION

A true 18-bit dynamic range has been realised in one circuit combining digital filtering, noise shaping and D/A conversion. Full-scale linearity equals 90 dB. The use of a current calibration technique enables a multi-bit approach, which results in an easy application. Special attention is given to substrate noise in system choice and circuit design.

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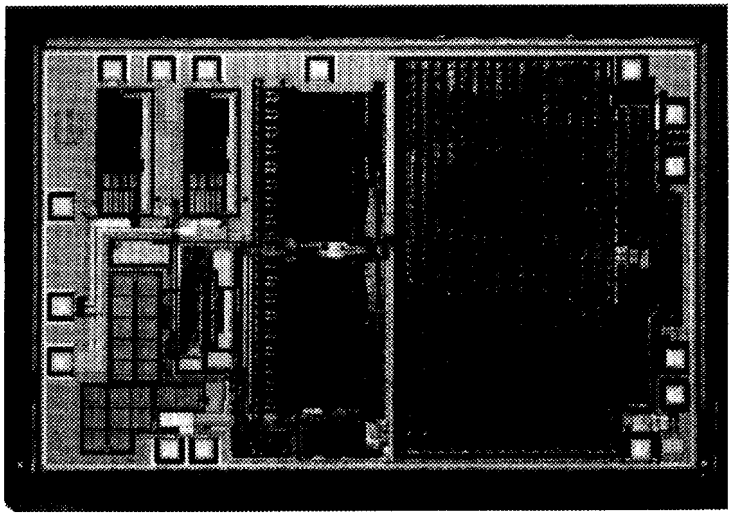

Figure 10: Microphotograph of the dual oversampling D/A converter

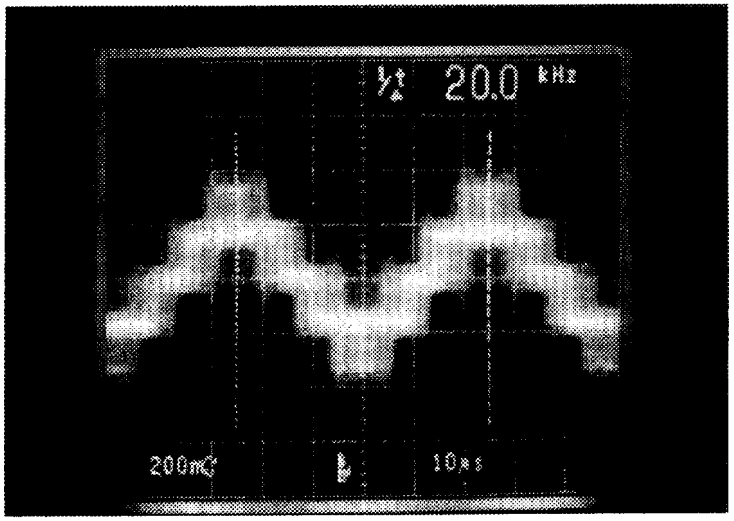

Figure 11: Typical output voltage of oversampled multi-bit D/A converter

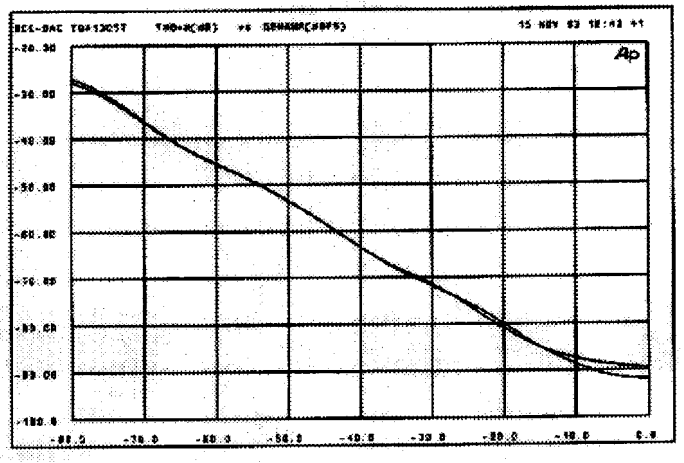

Figure 12: Measured S/(N+THD) as a function of output level

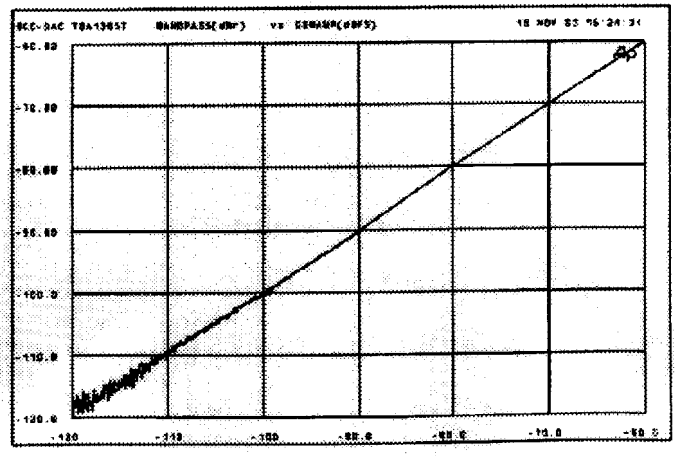

Figure 13: Low-level linearity