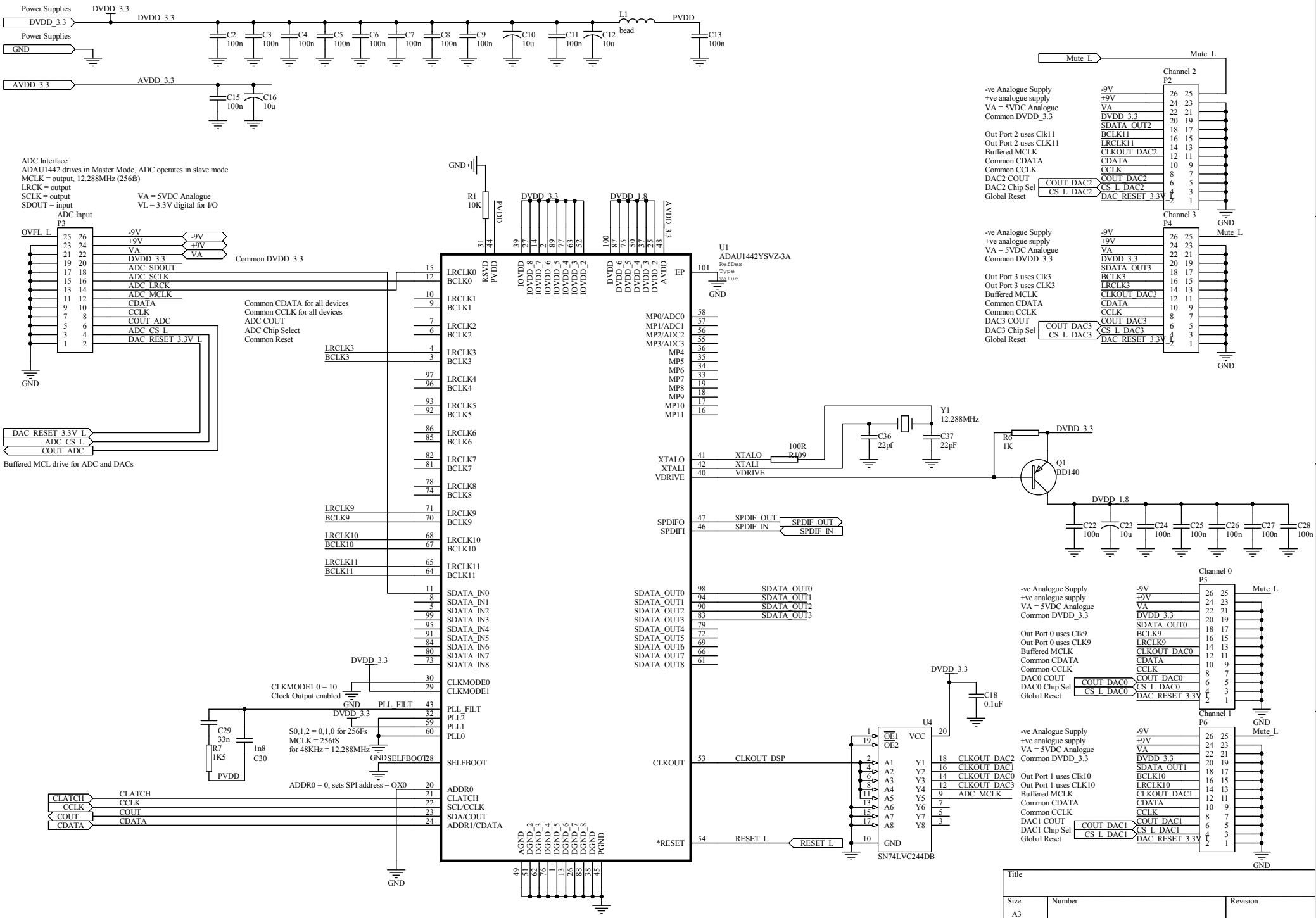
Power Supplies
DVDD_3.3
GND
AVDD_3.3
C2 100n
C3 100n
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 10u
C11 100n
C12 10u
L1 bead
PVDD
C13 100n
C15 100n
C16 10u
ADC Interface
ADAU1442 drives in Master Mode, ADC operates in slave mode
MCLK = output, 12.288MHz (256fs)
LRCK = output
SCLK = output
SDOUT = input
VA = 5VDC Analogue
VL = 3.3V digital for I/O
ADC Input
P3
OVFL_L
-9V
+9V
VA
DVDD_3.3
ADC_SDOUT
ADC_SCLK
ADC_LRCK
ADC_MCLK
CDATA
CCLK
COUT_ADC
ADC_CS_L
DAC_RESET_3.3V_L
Common DVDD_3.3
Common CDATA for all devices
Common CCLK for all devices
ADC COUT
ADC Chip Select
Common Reset
Buffered MCL drive for ADC and DACs
R1 10K
U1
ADAU1442YSVZ-3A
RefDes
Type
Value
LRCLK0
BCLK0
LRCLK1
BCLK1
LRCLK2
BCLK2
LRCLK3
BCLK3
LRCLK4
BCLK4
LRCLK5
BCLK5
LRCLK6
BCLK6
LRCLK7
BCLK7
LRCLK8
BCLK8
LRCLK9
BCLK9
LRCLK10
BCLK10
LRCLK11
BCLK11
SDATA_IN0
SDATA_IN1
SDATA_IN2
SDATA_IN3
SDATA_IN4
SDATA_IN5
SDATA_IN6
SDATA_IN7
SDATA_IN8
CLKMODE0
CLKMODE1
CLKMODE1:0 = 10
Clock Output enabled
PLL_FILT
PLL2
PLL1
PLL0
S0,1,2 = 0,1,0 for 256Fs
MCLK = 256fS
for 48KHz = 12.288MHz
SELFBOOT
ADDR0 = 0, sets SPI address = OX0
ADDR0
CLATCH
SCL/CCLK
SDA/COUT
ADDR1/CDATA
MP0/ADC0
MP1/ADC1
MP2/ADC2
MP3/ADC3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
XTALO
XTALI
VDRIVE
SPDIFO
SPDIFI
SDATA_OUT0
SDATA_OUT1
SDATA_OUT2
SDATA_OUT3
SDATA_OUT4
SDATA_OUT5
SDATA_OUT6
SDATA_OUT7
SDATA_OUT8
CLKOUT
*RESET
Y1 12.288MHz
C36 22pf
C37 22pF
100R R109
R6 1K
Q1 BD140
C29 33n
R7 1K5
1n8 C30
C18 0.1uF
U4
SN74LVC244DB
CLKOUT_DAC2
CLKOUT_DAC1
CLKOUT_DAC0
CLKOUT_DAC3
ADC_MCLK
Mute_L
Channel 2
P2
Channel 3
P4
Channel 0
P5
Channel 1
P6
-ve Analogue Supply
+ve analogue supply
VA = 5VDC Analogue
Common DVDD_3.3
Out Port 2 uses Clk11
Out Port 2 uses CLK11
Buffered MCLK
Common CDATA
Common CCLK
DAC2 COUT
DAC2 Chip Sel
Global Reset
Out Port 3 uses Clk3
Out Port 3 uses CLK3
DAC3 COUT
DAC3 Chip Sel
Out Port 0 uses Clk9
Out Port 0 uses CLK9
DAC0 COUT
DAC0 Chip Sel
Out Port 1 uses Clk10
Out Port 1 uses CLK10
DAC1 COUT
DAC1 Chip Sel
Title
Size
A3
Number
Revision
Date: 11/20/2012
Sheet of
File: C:\Users\..\CODEC and DSP.Sch
Drawn By: