

Another significant cost adder is test and trim time which must be kept below 30 seconds to avoid tying up expensive machinery and thereby limiting capacity. It is very important to minimize the number of trims by relying on inherent matching and to reduce the time of each trim by employing careful layout and efficient trim algorithms.

A further consideration is packaging, which has a large impact on both cost and performance. For a consumer oriented product plastic packaging is mandatory but it does present some problems. Since the package is non hermetic, the chip needs its own protection against moisture to prevent deterioration of sensitive analog circuitry. Also, stresses can be built into the chip during assembly which can affect performance. In fact, these effects were largely responsible for the non-ideal performance of some earlier products addressed in reference [2]. Considerable insight has been gained over the years and passivation methods have been developed which, when combined with careful assembly procedures, provide long term reliability in the most demanding environments. By employing careful circuit layout, optimizing certain process parameters and adhering to specific assembly material and procedures, package induced errors can be virtually eliminated.

Although the preceding factors must be closely controlled, circuit performance, the first factor, is the most important. If certain specifications are not met the product will fail. Fortunately, experience with other high resolution data converters built on this process coupled with the novel "Colinear" approach ensure that the critical specifications can be met.

A target specification is given in table 1.

## CIRCUIT REALIZATION

A block diagram Figure 1 illustrates the internal functions necessary to achieve the targeted specifications. An input shift register accepts the serial data and feeds parallel output latches which control the upper and lower DACs. Decoding of the MSB is used to control the data in the two banks of latches and the switching of the extra LSB required by the code conversion, Figure 2. The lower DAC (DAC A) is switched to provide the negative signal excursion from negative FS (all bits off) to BPZ (all bits + one extra LSB on). For the positive excursion the upper DAC (DAC B) is exercised from BPZ (all bits off) to positive FS (all bits on). DAC A and the extra LSB remain on for the entire positive excursion. The extra LSB is required to make the DAC output swing coincide exactly with the BTC input code. The latches control the DAC current switches that steer the bit currents either to analog ground or via the R-2R ladder to the output. To achieve an accurate current output of +/-2 mA over the temperature range, a buried zener reference and servo amplifier are used to drive the current sources. A nonsegmented current source architecture is employed since superposition errors can be minimized and the extra decoding circuitry and trimming complexity add unnecessary cost [3].

Though the "Colinear" approach completely overcomes low level nonlinearity problems it presents a new challenge to the achievement of full scale linearity. Since the transfer function is made up of two sections, each contributed by a separate DAC, it is extremely important that each section has the identical slope or gain. For example, to achieve a full scale THD of 0.001% the gains must match to better than 0.005%. One obvious way to achieve this, is to employ a gain adjustment trim at the output of the servo amplifier. There are two problems associated with this. Firstly, since the gains must match over the full temperature and supply ranges, a shared servo amplifier is desirable, and it is difficult to provide an adjustable interface to each DAC, while maintaining the low output impedance necessary for glitch elimination. Secondly, any gain adjustment trimmed in at the factory is susceptible to minute package shifts. For these reasons there is no gain adjust as such. Both DACs are laid out as one and the gain adjust is an inherent part of the standard linearity trim. ( This is discussed in more detail below.) To this end each bit of each DAC is physically interleaved and both DACs share the same R-2R ladder network.

The bipolar offset (BPO) current is produced from a reference voltage developed across the BPO resistor. This resistor is connected externally to the summing node of the output inverting amplifier and internally to a reference amplifier. The reference voltage is generated from a matched current source and this trans-resistance, reference amplifier. On the chip is a precision trimmed feedback resistor, which is available for use with the external, output amplifier.

## DIGITAL LOGIC

Differential Current Mode Logic (CML) is employed to minimize area and power while allowing operation at clock rates in excess of 25 MHz. The device is, therefore, easily capable of 16x oversampling. Essentially the digital interface and logic employed is the same as previously described [5] and will not be explained further. The major differences are in the MSB decoder and the latches. Since the data stream comes in MSB first and the word clock (LEC) occurs at the end of the data stream, the only way to identify the MSB is to examine the data in the final shift register stage when the latch pulse occurs. The flip-flop associated with the MSB, now, no longer drives a bit switch but is coupled through an amplifier to drive the latch lines M and Mnot. The MSB decoder circuit is shown in Figure 3 and the logic block diagram is illustrated in Figure 4.

The latches associated with the lower DAC are connected to Mnot while those associated with the upper DAC are connected to M. The way in which the latches are interleaved in the circuitry ensures that M and Mnot run side by side and therefore comply with the general strategy of employing differential logic. This helps considerably in minimizing the effects of digital feedthrough.

The latches are shown in Figure 5, where the tripple emitter coupled configuration determines the latch output. The level of M and Mnot are at least 200 mV

greater and less than D and Dnot respectively. In this way M or Mnot overrides the data input dependant on the polarity of the MSB. For example during the negative excursion of the signal when M is positive, the B latches are forced low and DAC B turns off. Simultaneously Mnot is low, so that the true data D or Dnot is latched in to the A latches which in turn control the output of DAC A. During the positive signal excursion the A latches are all forced high and DAC A remains fully on, while the true data controls DAC B.

The possibility of eliminating the glitches normally associated with this type of DAC has been demonstrated in earlier products. It requires differential switching together with critical timing delays. Although this architecture has no glitch at the critical bipolar zero level, this circuitry is included in order to provide superior full scale THD. The delay is incorporated at the output of the latches associated with the five most significant bits or in this design bits 2 through 6. It consists of a small capacitor differentially connected between the bases of the latch output transistors and an independent scaling of the resistors which set the quiescent current of these same transistors. The values are "tweaked in" after the initial circuit is fabricated to compensate for those minute delays associated with layout and impossible to simulate accurately. Subsequently, these values are incorporated into the layout and are found in practice to give excellent glitch elimination over normal process spreads. This arrangement obviates the need for external deglitching circuitry and often improves performance by avoiding the associated noise and distortion.

Another difference in this architecture is the need for the extra LSB associated with DAC A and required to produce the correct bipolar zero level. The extra bit is activated by a simple cross coupled latch which is driven by the MSB decoder lines M and Mnot. This can be seen in Figure 4.

## CURRENT SOURCES

A nonsegmented architecture is employed, with bits 2 through 13 having identical 250  $\mu\text{A}$  current sources. Bit 2 is comprised of four such sources, bit 3 has two and all subsequent bits have one. Bits 5 through 13 are scaled through an R-2R ladder network. The lower six bits, 14 through 20, utilize current and emitter scaling in a two stage arrangement to minimize the area required. This configuration, shown in Figure 6, is very economical in terms of area but it does introduce a small error over temperature. This is because the base to emitter voltages ( $V_{be}$ 's) associated with the lower bits do not track those of the upper bits. For bits 14 through 16 the emitter degeneration is such that a maximum mismatch of 0.5% occurs over the operating temperature range. For the lowest bits, 17 through 20, the mismatch increases to 5% or a maximum of 0.8 LSB. Since these lower bits remain monotonic to a 20 bit level, it is considered an acceptable degradation. Upper and lower DACs use common lower bit scaling resistors which ensure excellent tracking. The lower seven bits are not trimmed since the inherent matching of the process is sufficient. The trim tabs on bit

resistors 2 through 13 are made considerably larger than on previous designs to provide a finer trim resolution.

In order to achieve operation from  $\pm 5$  Volt supplies it is not possible to use a cascode transistor between the current source and current switches. However, the bit switches perform this function by shielding the current sources from variations in collector to emitter voltage, caused by code dependent drops in the ladder. To keep the switching transient from causing ringing on the current source reference line, it is imperative that the servo amplifier provides a low impedance at all frequencies of concern. Another consequence of the low supply voltage is the reduced degeneration available at the current source emitters, only 2.2 Volts in this case. This makes layout considerations, that concern matching, even more critical. The management of thermal profiles and metal drops are two examples. Experience with previous products suggested that the desired performance was achievable even with this voltage constraint. The lower supply voltage does have some benefits because the reduced power dissipation provides enhanced reliability and stability.

In addition to the simple interleaving of the individual bits of each DAC, the multiple current sources associated with upper bits 2 through 6 are themselves interleaved. The most critical bits are placed in the center of the die where the effects of packaging stress are the least. Other layout considerations include maintaining the switching transistors equidistant from their associated current source transistors and keeping the lumped constant heat sources as far away as possible from these critical components. The shift register and latches, because of their differential configuration, can be treated as constant sources of heat, providing they are sufficiently removed. Voltage drops are managed by using very wide traces, star connecting or matching metal drops where they cannot be eliminated. Matching is also improved by making all critical resistors and transistors identical in shape, size and orientation. Furthermore, trimming time may be considerably reduced if all resistors have the same orientation. The results of these considerations may be observed in the chip layout Figure 7.

In determining the value of the R-2R ladder two major conflicting requirements must be considered. Firstly, the ladder resistor should be as high a value as possible to minimize its own noise contribution and to lower the noise gain of the external amplifier. Secondly, the ladder resistances should be minimized to reduce the code dependent voltage drops occurring at the current switch nodes. These drops can cause superposition errors due to the modulation of the switch transistor current gains. This effect is minimized by maintaining both high current gain and high output impedance. After careful consideration, a value which affords the best compromise, is selected.

## BIT ADJUSTMENT

Although a major feature of this DAC is its guaranteed, adjustment free, low level linearity, it is always possible to improve the performance of large amplitude

signals, by externally adjusting the larger bit values. It is believed that some OEMs will wish to add extra value to their products by making such an adjustment. So to allow further product differentiation, external adjustment potentiometers may be connected between a temperature tracking output of the voltage reference and nodes on the upper and lower bit 2 resistors. Adjustment should be made to improve the overall gain matching of the individual DACs.

## REFERENCE AND SERVO AMPLIFIER

An onboard reference reduces the need for external components and enhances system performance by tracking the temperature changes of the DAC. It is one of the most critical elements since the basic accuracy of the converter is directly dependent on it. A subsurface zener diode is at the heart of the reference and provides a highly stable, low noise, voltage source. The bias current is generated from the zener itself and being held at a constant value, enhances reference voltage stability. Since the zener is used to bias itself, a start-up circuit is required. This is shown in Figure 8, where the N channel epitaxial FET turns on at start-up and supplies the base current to the biasing transistor. This in turn, provides the zener current via a lateral PNP mirror circuit. As the zener turns on and the voltage on the gate of the FET increases, the FET is pinched off and is effectively removed.

A  $V_{be}$  multiplying circuit comprising Q408, Q409, R406 and R407 is required to compensate for the overall negative temperature coefficient of the circuit. The output of the circuit is a current, constant to within  $\pm 25$  ppm over the temperature range. This current is supplied to the servo amplifier, the output of which (VREF) feeds all the DAC current sources. It can be seen that the DAC output current can be increased or decreased with respect to the reference current by trimming R503 or R504. Cascode Q508 simulates the effect of the bit switch associated with the true current sources and, therefore, ensures better tracking. Lateral PNP transistor Q506 prevents any possible latch-up caused by unusual power supply sequencing. The base of output transistor Q505 is brought out to a pad for decoupling. The external decoupling capacitor serves a four-fold purpose: to compensate the amplifier, to improve power supply rejection, to reduce noise and to maintain a low impedance on VREF.

## REFERENCE AMPLIFIER

The trans-resistance, reference amplifier shown in Figure 9 provides a stable reference voltage at the emitter of Q603. This voltage is developed by the reference current flowing through trimmable resistor R605. The reference current is generated in an identical fashion to the bit current and therefore tracks any variations. Trimming of R605 or the bipolar offset resistor, R606, allows bipolar zero to be adjusted up or down.

The offset decoupling capacitor compensates the amplifier and reduces the noise contributed to the converter output.

The three analog components: current reference, servo amplifier and reference amplifier, are placed along one edge of the die as far removed from the critical current sources as possible. This helps to minimize the effects of unequal heating. Also, since the heat from these sources is constant, any remaining effect can be eliminated during the trim phase. Placing these components on the chip, not only removes an enormous burden from the user, but gives improved performance because of their excellent tracking over temperature and process variations.

## NOISE CONSIDERATIONS

The major sources of noise are power supply noise, digital switching noise and thermal noise generated by the circuit components. If sufficient care is taken in external grounding and layout and the recommended decoupling components are employed, supply induced noise can be effectively eliminated. Similarly, thermal noise originating in the reference, servo amplifier and reference amplifier may be externally decoupled. Digital switching noise is minimized by the use of separate digital supplies and grounds and by the use of totally differential switching. In this way, the analog circuitry is separated from the digital. Where connections are made, either directly at the current switches or indirectly through parasitic capacitances, the digital energy is largely cancelled. Consequently, the major noise contributors are the thermal noise sources due to the ladder, bipolar offset and bit resistors and these are fixed by supply voltage and power considerations.

## TRIMMING

To trim a device to the level of accuracy required and still maintain a reasonable trim time demanded a complete change of test hardware. This hardware features high speed and high resolution analog to digital conversion and digital processing. With this new system it is possible to trim routinely to within 5 ppm.

This product requires an unconventional trim algorithm to ensure precise matching of the two DACs. If the usual differential linearity (DL) trim is employed the errors accumulated are too great. Also, to minimize superposition errors, it is imperative that the part be trimmed in the same way it is used. This implies that bits associated with DAC B only turn on when DAC A is already fully on. As a result of these restrictions there are only two ways to achieve the required match: an absolute trim, which takes an enormous amount of calibration time, or a comparative trim using the lower DAC as a reference. The latter is preferred for economical trimming but it presents another problem. Since DAC A turns fully on whenever DAC B is activated another reference DAC is required. By using an external reference (DAC C), as an

adjustable current source, to counteract the weight of DAC A, the problem is solved. Any systematic error between DAC A and DAC C appears as an offset error and is trimmed out later. The circuit is shown in Figure 10. With this algorithm it is possible to achieve the appropriate gain match, but since the upper DAC is trimmed against the lower it is subject to greater accumulated trim errors. At present it is possible to trim the upper DAC to a DL error of within 15 ppm, which provides acceptable full scale performance.

## PERFORMANCE

All measurements were made using an OPA27 operational amplifier and an external 1.5 kohm feedback resistor, unless specified otherwise.

Figures 11 and 12 show a -90 dB and a -110 dB sinewave, respectively, at the output of an ungraded, randomly selected "Colinear" DAC. The input is derived from computer generated 20 bit data at a 4x oversampling rate. This measurement was made using a Tektronix 7A22 vertical scope amplifier with the filter set at 10 Hz high pass and 30 kHz low pass. A passive 20 kHz, single pole, RC filter is placed in series with the scope input.

Figure 13 shows the frequency spectrum out to 20 kHz of the same -90 dB signal using an HP 3580A Spectrum Analyzer. The peak at 15.8 kHz is generated from external, spurious sources and is not a function of the converter.

Figure 14 is the result of playing the fade-to-noise track, of the CBS CD-1 test disc, while employing an NPC 5813 digital filter in conjunction with the HP 3580A, as an analog filter, set at a bandwidth of 30 Hz.

Figure 15 is the result of playing the monotonicity track taken from the test disc and recorded using an HP 3562A Dynamic Signal Analyzer.

Figure 16 is the result of the same track produced by a Matsushita MN 6471 noise shaping converter as found in a commercially purchased Technics brand CD player, model SL-P777. It is recorded on the HP 3562A and included for comparison.

Figure 17 shows plots of THD + noise (dB) against frequency for signal levels of 0 dB, -20 dB, -40 dB and -60 dB referred to FS. The input is computer generated, 20 bit data at a 16x oversampling rate. An OPA627 amplifier is used followed by a third order GIC filter and the output is recorded using an Audio Precision System 1 set at a bandwidth of 22 Hz to 22 kHz.

Figure 18 is a similar plot taken using the SL-P777 at full scale level. The four traces represent left and right channels, each with and without an external 20 kHz brickwall filter.