

6

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

D

C

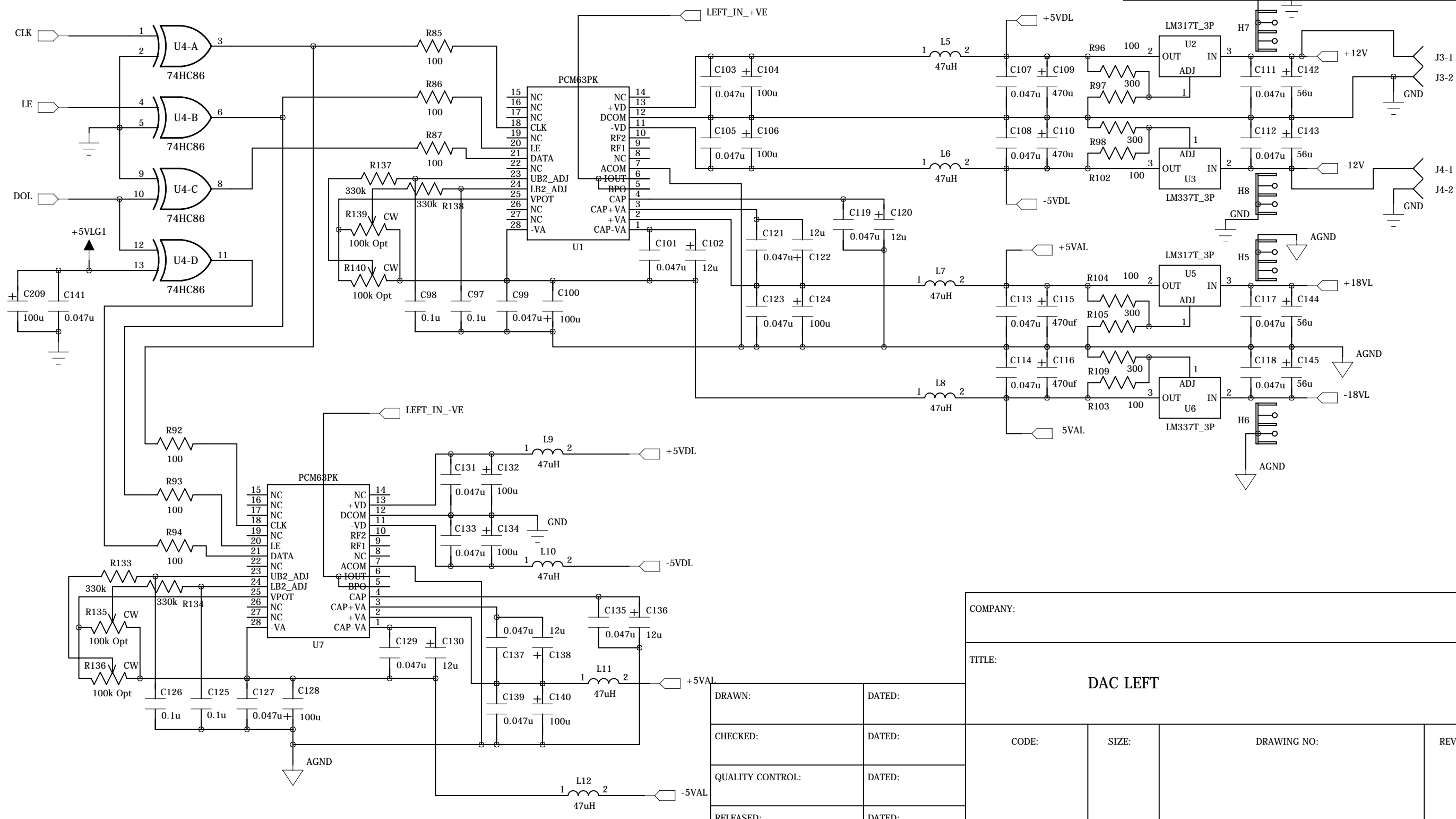
C

B

B

A

A



COMPANY:			
TITLE: DAC LEFT			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:		SHEET: OF 5	

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

6 5 4 3 2 1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

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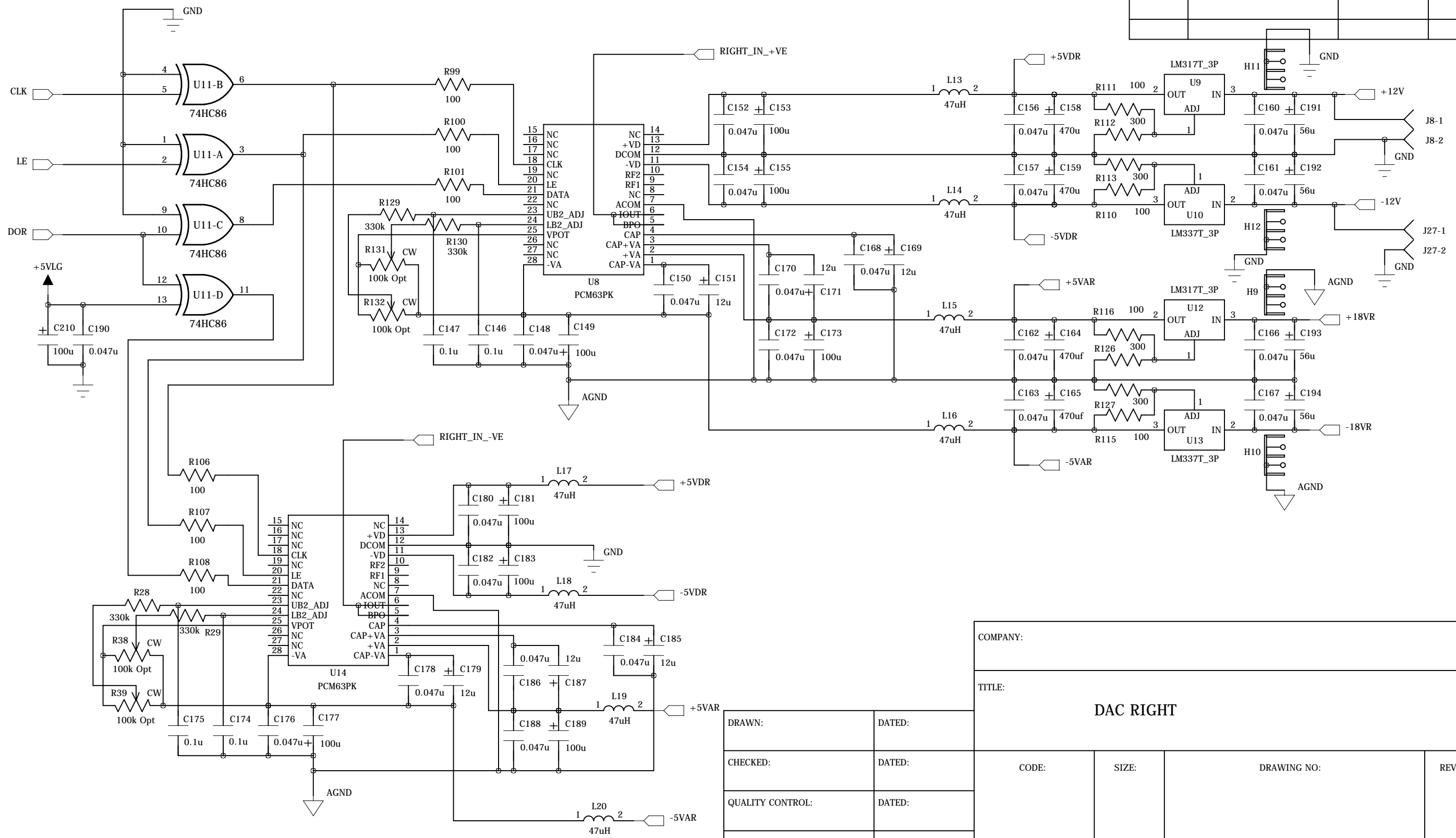
C

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COMPANY:			
TITLE: DAC RIGHT			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:		SHEET: OF 6	

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

6

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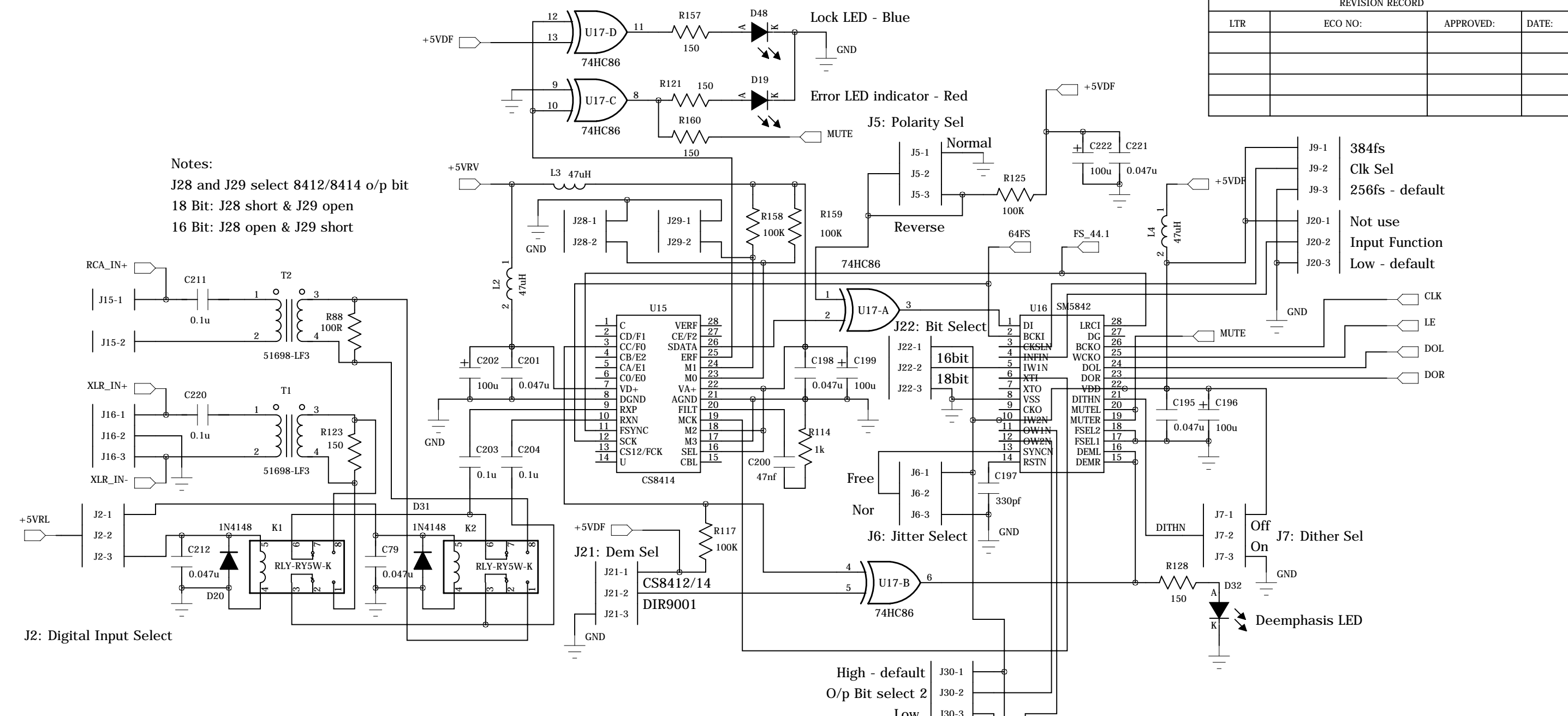
3

2

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Notes:
 J28 and J29 select 8412/8414 o/p bit
 18 Bit: J28 short & J29 open
 16 Bit: J28 open & J29 short



J2: Digital Input Select

J21: Dem Sel
 J21-1 CS8412/14
 J21-2 DIR9001
 J21-3

High - default
 O/p Bit select 2
 Low
 20bit
 High
 O/p bit select 1
 Low - default

J9-1 384fs
 J9-2 Clk Sel
 J9-3 256fs - default
 J20-1 Not use
 J20-2 Input Function
 J20-3 Low - default

J7: Dither Sel
 J7-1 Off
 J7-2 On
 J7-3

COMPANY:			
TITLE: RECEIVER & DIGITAL FILTER			
DRAWN:	DATED:	CODE:	SIZE:
CHECKED:	DATED:	DRAWING NO:	
QUALITY CONTROL:	DATED:	REV:	
RELEASED:	DATED:	SCALE:	SHEET: OF 7

6

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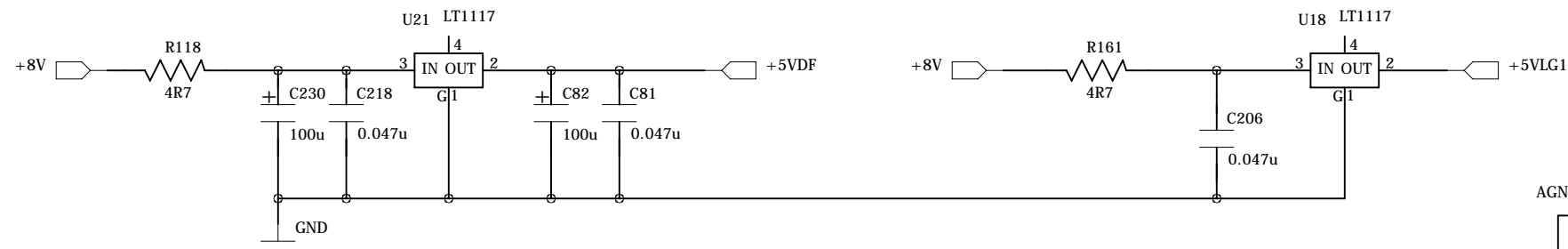
2

1

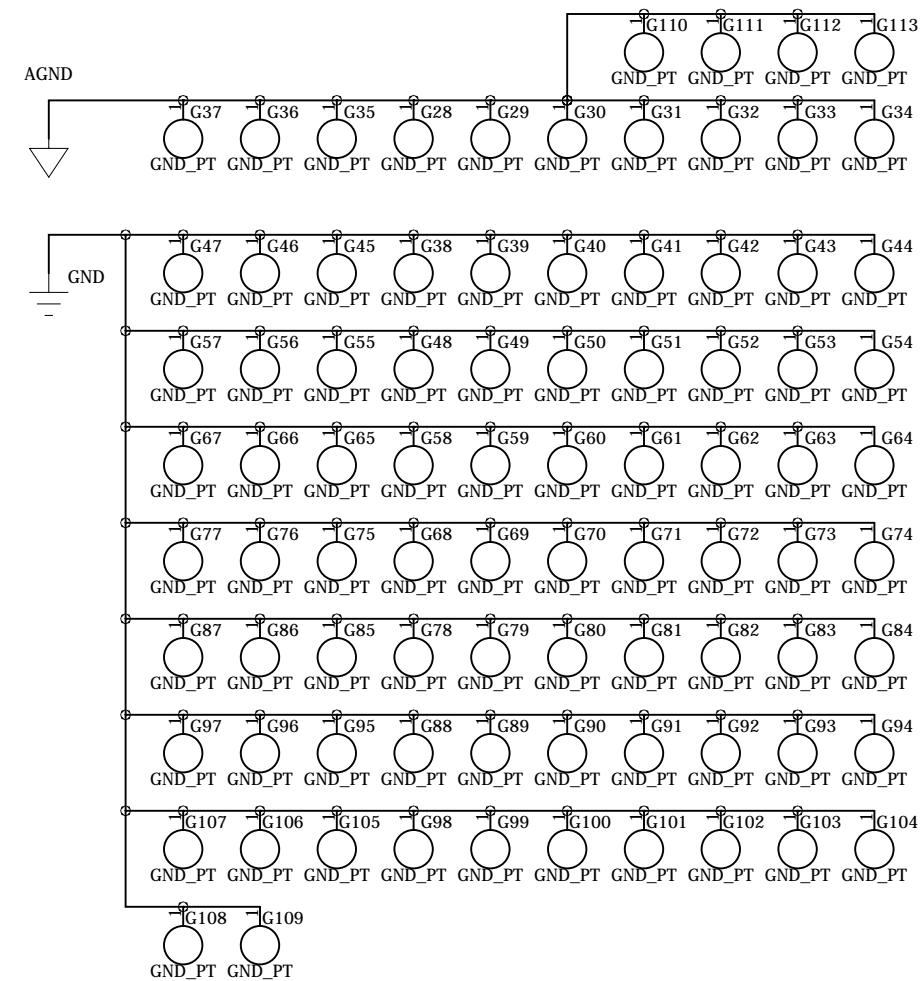
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

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D

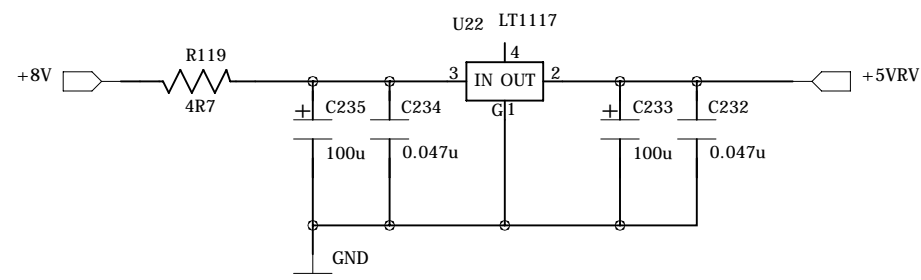


Analogy Ground and Digital Ground Via holes



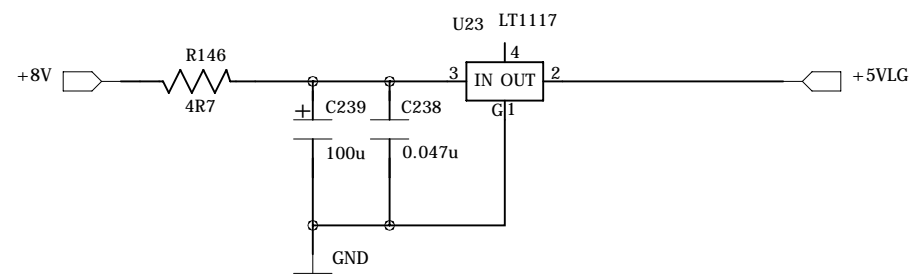
C

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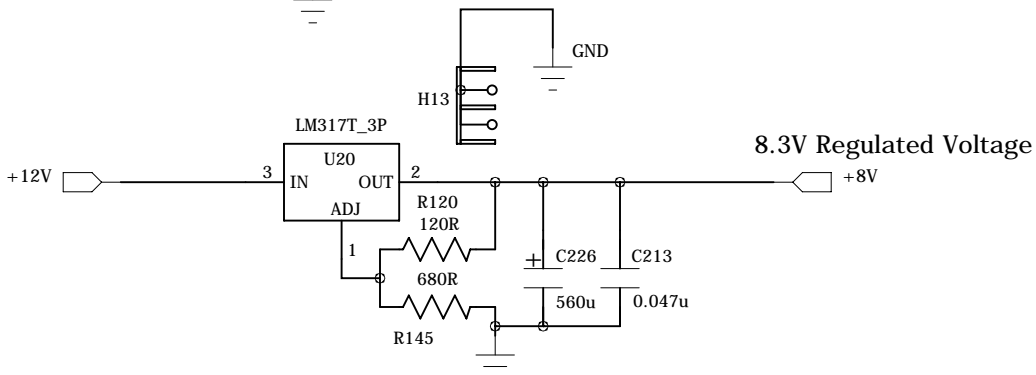
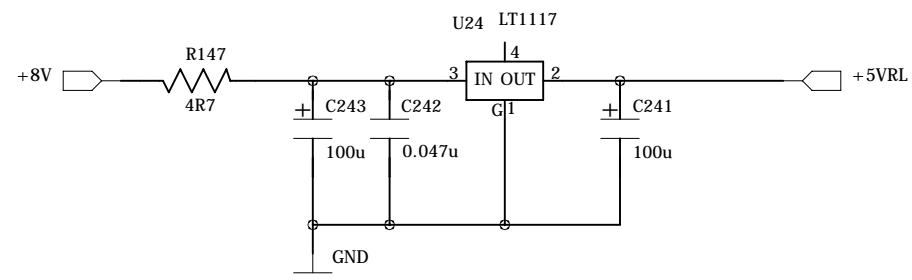
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COMPANY:			
TITLE: Digital Supply and pre-regulator			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:			SHEET: OF 9

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

6

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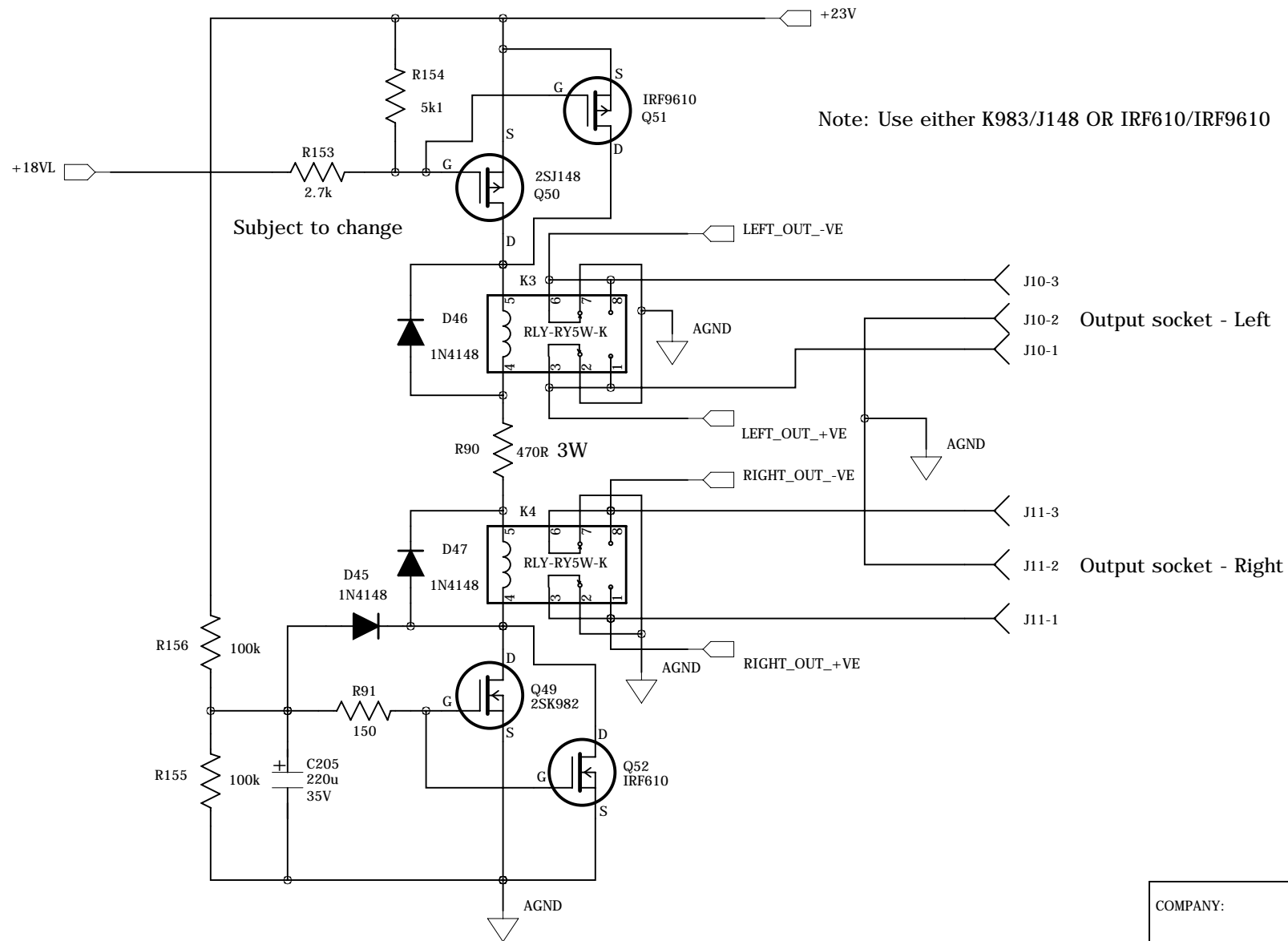
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1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:			
TITLE: Output Delay and Mute			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:			SHEET: OF 10

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

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