Buffer Amplifier Design
*by Dennis L Feucht*

The ×1 voltage amplifier, or "buffer," is a standard building block of analog design. This article presents the design of a discrete, low-parts-count, high-performance, matched-transistor buffer, and covers some of the finer points in optimizing its design.

In an era when a buffer is most easily implemented with an op amp, why use a discrete circuit? When high precision and minimal space are not worth the extra cost, a dual-JFET amplifier costing 50¢ in parts can deliver multiple hundreds of megahertz of bandwidth with an offset error of 10 mV, or less, and an offset drift of 10 μV/°C or less. By applying ingenuity good performance can be attained with discrete-component circuits, which will still be available when the op amp is obsolete. The buffer can become part of your design library.

Buffer Amplifier Circuit

The design goal of the ×1 voltage amplifier is that of the ideal voltage amplifier: infinite input impedance, zero output impedance, and linearity. To achieve high input impedance, a JFET instead of a BJT is used, as shown in the buffer circuit below.
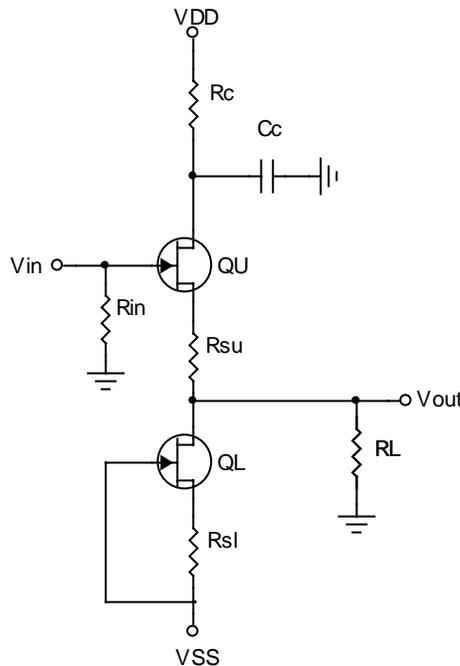
Discrete JFETs are available from over a half-dozen suppliers, including:
Fairchild http://parametric.fairchildsemi.com/ss.asp?FAM=JFET
ON Semi
www.onsemi.com/parametrics/selector/0,4093,10364,00.html?LevelName0=Product&LevelName1=Discrete&LevelName2=Small+Signal+Transistors&LevelName3=JFETs&AssociatedParametrics=JFETs+10364
Philips
www.semiconductors.philips.com/catalog/219/282/27046/30928/15490/15491/index.html#15491
Toshiba www.semicon.toshiba.co.jp/eng/prd/mpsig/ft_mpsig.html
Vishay Siliconix www.vishay.com/brands/siliconix/SSFsgnchjamp.html

For low cost, discrete JFETs are chosen, despite the advantages in thermal tracking of dual devices in a single package, such as the 2N3958, 2N5196 through 2N5199, and the 2N5564 through 2N5566. These dual parts tend to cost anywhere from $4.50 each to over $40 for the best ones. If you can absorb the additional cost, these are superior to discrete JFETs in their thermal tracking.

Some discrete n-channel JFET alternatives for the buffer are the 2N5484 through 2N5486. The 2N5485 costs about $0.20 each (in hundreds). It has a drain current selected for a nominal design value at midrange of $I_{DSS} = 7$ mA (I_{DSS} is I_D @ $V_{GS} = 0$ V) in a 4 to 10 mA specified range. Furthermore, the two JFETs are selected to match using a curve tracer. This takes less than one minute per pair, by sorting them into matching I_{DSS} bins, for an additional $0.10 of US labor.

Next, choose some standard supply voltages: $V_{DD} = +12$ V and $V_{SS} = -5$ V. These supply voltages are common in both desktop computers and instrumentation.

Offset Voltage

The first design feature of matched JFETs is the static (dc) tracking of the matched transistors. If the gate of the lower transistor, QL, is connected to its source, then $V_{GS} = 0$ V, and the drain current will be I_{DSS}. If this same current flows (with open load) through QU, then because it is matched, its V_{GS} is also zero and there is no voltage offset from input to output.

This nifty technique can be improved by setting the JFET operating point to the zero TC point instead, where thermal drift of V_{GS} with a given I_D is minimal over temperature. For JFETs the zero-drift V_{GS} is about 0.8 V above the pinch-off voltage. The value of this V_{GSZ} is where the I_D lines for various temperatures intersect. For the 2N5485 this is at about -1.2 V. And this is about 0.8 V higher in value than the pinch-off voltage of around -2 V. The curves for the 2N5485 (Siliconix) are shown below.

Transfer Characteristics
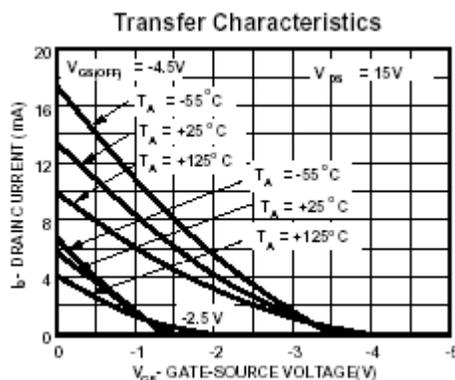
Using these values, Rsl = Rsu = R_z = 1.2 V/5 mA = 240 Ω, a 5% value. The voltage drop across Rsl is compensated in the signal path by a similar drop across the matched resistor, Rsu. For better matching, these resistors can be 1% tolerance instead.

Thermal Distortion

With a varying input voltage, the power dissipation of the two JFETs will also vary. A change in power causes a change in silicon temperature, which results in thermally-induced electrical noise, or "thermals," in the amplifier response. This "noise" is

waveform-related and can better be regarded as *thermal distortion*. It can be minimized by setting the dc operating conditions (or bias) for maximum power dissipation in the JFETs with no input (that is, at *quiescence*). The change in power (which we want to minimize) is least around the peak power value.

Let the quiescent dc bias current (or "standing current") of the JFETs be I_0. Then the power dissipated by upper and lower transistors is:

$$p_u = \left(V_{DD} - v_L - (R_c + R_z) \cdot \left(I_0 + \frac{v_L}{R_L} \right) \right) \cdot \left(I_0 + \frac{v_L}{R_L} \right) = V_{DD} \cdot I_0 + \left(\frac{V_{DD}}{R_L} - I_0 \right) \cdot v_L - \frac{v_L{}^2}{R_L}$$

and, $p_l = (v_L - V_{SS} - R_z \cdot I_0) \cdot I_0$

where, v_L is the load voltage (across R_L). The difference in power dissipation is:
   $\Delta p_D = p_u - p_l$

The power graphs are shown below, plotted using MathCAD.

At maximum Δp_D, the change in power with v_L is minimum, which is desired to minimize thermals. Differential power is maximum at:

$$v_L(\text{max}) = \frac{R_L}{(R_c + R_z) + R_L} \cdot \frac{V_{DD}}{2} - I_0 \cdot R_L$$

Another voltage of passing interest is where p_u and p_l are equal. Solving for v_L at $\Delta p_D = 0 \cdot \text{W}$:

$$v_{L0} = v_L(\text{max}) \pm \sqrt{v_L(\text{max})^2 + \left(\frac{R_L}{R_c + R_z + R_L} \right) \cdot I_0 \cdot R_L \cdot (V_{DD} + V_{SS} - R_c \cdot I_0)}$$

On the plot, $v_{L0} = 5.3$ V. Though the power dissipation is matched at this output voltage,
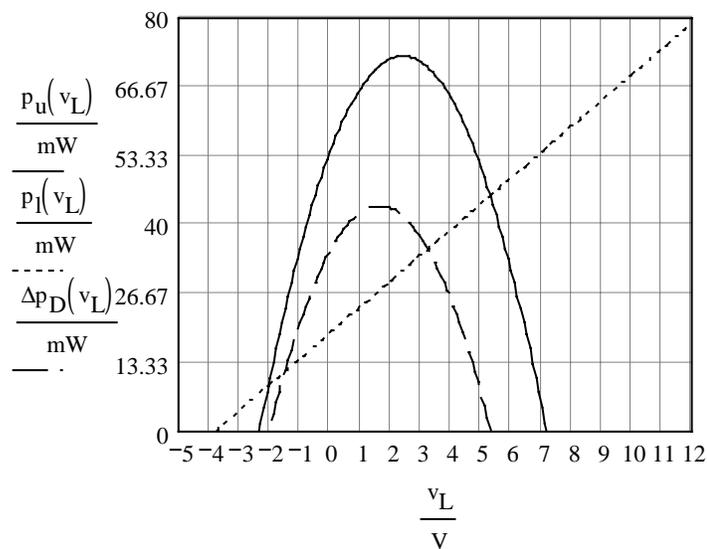
any change around this value causes a larger change in Δp_D than the same change in v_L around $v_L(\text{max})$. Consequently, the preferred bias point is at $v_L(\text{max})$.

On the plot, $v_L(\text{max}) = 1.62$ V. But the given circuit parameters have a quiescent v_L of 0 V instead. To adjust the quiescent voltages across the JFETs, an additional series resistor, R_c

is added. For the general case, let the quiescent output voltage be V_L. Then to set the vertex of the differential-power parabola at V_L:

$$v_L(\max) = \frac{V_{DD}}{2} - R_L \cdot I_0 = V_L$$

and solve for the value of V_{DD} that will satisfy the desired condition:

$$V_{DD}(\max) = 2 \cdot (V_L + R_L \cdot I_0)$$

Then substitute V_L and the available supply V_{DD} into:

$$R_c = \left(\frac{V_{DD}}{2 \cdot (V_L + R_L \cdot I_0)} - 1 \right) \cdot R_L - R_z$$

For this design, $R_C = 490\ \Omega$. C_C bypasses R_C so that no appreciable voltage change occurs at the drain.

Matched-BJT Buffer Amplifier

JFETs are superior to BJTs in that they have high input resistance and low input bias current. However, for the same TC, current matching must be an order of magnitude better for FETs than BJTs. This is why the input offset specification of FET-input op amps is generally worse than their BJT counterparts. Put simply, BJTs match better than JFETs.

If your buffer does not call for extremely high input resistance, use BJTs instead. The biasing will have to be done somewhat differently, using a fixed base voltage for QL. This makes QL a current source which drifts with temperature due to $V_{BE}(T)$. But a matched QU drifts similarly with the same bias current, and dynamic emitter resistance:

$$r_e = \frac{V_T}{|I_E|} = \frac{kT/q_e}{|I_E|} \cong \frac{26\text{mV}}{|I_E|}, 300\ \text{K}$$

is kept constant with temperature as I_{CL} ($= I_{EU}$) varies with temperature. As temperature increases, V_{BEL} decreases and I_{CL} increases. At the same time, r_{eU} increases with thermal voltage, but increased emitter current compensates by decreasing r_{eU}. The TC of current from QL compensates for changes in r_e, which affects the buffer voltage gain.

(The derivations of buffer design and thermal equations are found in *Analog Circuit Design* by the author. See http://www.innovatia.com)