Power amplifier design criteria

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This paper describes the criteria, objectives and solutions adopted for the configuration of the range of TAG McLaren Audio F3 series power amplifiers. The requirements for high quality domestic audio amplifiers are discussed in the introduction and the configuration adopted is described with reference to how it achieves the specified objectives.

Introduction

The criteria for the design of a high quality high fidelity audio power amplifier results in a number of conflicting requirements.

The initial requirement for audio power amplifier design to drive the typical high fidelity loudspeaker of 8 Ω nominal impedance would appear to be easily satisfied. However closer inspection of the demands placed upon the amplifier reveal that complex set of criteria have to be satisfied if a superior product is to be created. TAG McLaren engineers have investigated the real world requirements and then produced solutions which have contributed toward creating the highly lauded range of TAG McLaren F3 series power amplifiers.

Improvements in the quality of music reproduction are achieved through a carefully considered analysis followed by the creation of a design which addresses all of these demands

The following issues summarise the requirements set for the TAG McLaren F3 series of power amplifiers.

Power rating

To provide adequate power reserves to drive available loudspeakers to satisfactory levels without 'distorting' the music signal on crescendos the range of F3 products were designed to deliver 60 watts both channels driven into 8 ohms for the 60i, 60iRv and 60P amplifiers, 100 watts both channels for the 100P and 125 watts for the single channel or monobloc 125M.

Load tolerance

The F3 range of power amplifiers are specified and designed to allow the greatest possible freedom in the choice of partnering loudspeaker. Investigation of the load presented to the amplifier by the products of diverse loudspeaker manufacturers demonstrated that it would require the capability of supplying the current demanded by loads as low as 2 ohms in order that the F3 products could be freely specified for use with the vast majority of speakers which may become part of the customers system. The motional impedance of moving coil drive units coupled with complex impedance crossover filter networks also increased the current and power dissipation demands over

that of the simple resistive 8 ohm specification load. In addition the amplifier must be safe with loads from 2 ohms down to short circuit (0 ohms) and be unconditionally stable when the phase angle between voltage and current vectors varies between + / 90 degrees.

Distortion

While paying attention to the classical measure of THD as a necessary parameter of amplifier performance this not been to the exclusion of other, more relevant, measures. The time varying nature and complex array of frequencies which comprise music waveforms demands that more attention should be paid to the dynamic and transient performance of the amplifier in both design and analysis.

Bandwidth

The advent of digital audio storage mediums has resulted in the capability to capture and record the lowest pitched sounds without modification of either the magnitude or group delay of the waveform. Provided the ancillary equipment used in the complete recording and playback chain is capable of an extended low frequency response then an amplifier should have sufficient bandwidth to preserve the musical waveform fidelity.

Consistency

When presented with the challenge of designing and building a limited number of amplifiers it is perfectly satisfactory to use adjustment trims, selected and matched

components to achieve the design objectives. However when the design is to be manufactured in significant numbers it is desirable that every example is indistinguishable from any other example. Semiconductor device parameters usually exhibit variations of the order of +/- 25% between examples whereas it is comparatively easy to obtain passive components with tolerances of 1 or 2%. Using circuit topologies where the gain of each and every stage of the design is defined by passive components results in minimal variation between any two examples of the F3 amplifiers even when those examples were manufactured several years apart.

Components

In order that the F3 series power amplifiers deliver class leading sound quality it necessary but not sufficient to focus solely on the technical circuit design. In any chosen amplifier configuration, whether high or low feedback, Class A or Class B there are passive components which are crucial to the sound quality. Original and innovative circuit design are the key ingredients to removing and minimising any detrimental effects caused by imperfections in component parameters.

Reliability

To deliver effortless sound quality into presently available loudspeaker the F3 series has been designed with the capability of driving load impedances as low as 2 ohms with dynamic music signals. However there may be occasions when the amplifier output

is inadvertently shorted. Should this happen when there is signal present then the current demanded by this minuscule resistive load may be of the order of hundreds of amps. Under these conditions the amplifier must restrict the current delivery such that the power dissipation of the power output devices remains within the Safe Operating Area. This action of protecting the amplifier must be performed by a method which has negligible adverse effect on the sound quality delivered during normal use.

Modern solid state electronic products are impressively reliable but it is prudent design to ensure that any failure either to a power amplifier or to any ancillary piece of equipment should not damage the loudspeaker. With the appropriate circuit design in place for short circuit protection it is then comparatively easy to extend the monitoring function to include component failure without compromise.

Amplifier Configuration

Overall concept

During the early development of all solid state amplifiers designers focused on achieving numerically low values of THD at a measured frequency of 1kHz. The quest for perfection drove most designers down the conventional path of minimising harmonic distortion at mid (1kHz) frequencies by means of engineering circuit topologies which maximised the forward or open loop gain. The conventional design of a multistage power amplifier consists of 2 cascaded stages of basically common emitter configuration followed by an emitter

follower (unity voltage gain) current multiplier. Commonly the designers have striven for maximum voltage gain for each common emitter stage as this will maximise the forward open loop gain with the intention of reducing the closed loop distortion through the application of feedback.

During the early 1970s a faction led by Matti Otala [1] questioned this trend with papers which set about analysing the internal workings of an audio power amplifier when subjected to driving signals containing fast transients. His examination and analysis led to the proposal that the necessary circuit topology for ultimate fidelity required moderate open loop gain resulting in feedback factors of the order of 20 to 30dB and open loop bandwidths in excess of 20kHz and preferably greater than that of the preceding preamplifier. These criteria resulted in amplifier designs such as that contained in a paper presented by Jan Lohstroh [2]. Thus during the early 1970s the low open loop gain, wide open loop bandwidth design was the pinnacle of excellence. However by the second half of the 1970s a group of respected design engineers, which included Jung, Stevens & Todd - [3], Cordell [4] responded with a series of academic articles whose central theme was that if feedback was applied with a full understanding of the mathematics and innovative circuit designs were utilised then there were many benefits to be gained in reverting to the use of generous levels of feedback. Further works by Sundqvist [5], Leach [6] and Garde [7] laid the ground work for amplifiers with the benefits of classical feedback without the shortcomings highlighted by Otala. From this work the circuit topology of the F3 series was developed to provide a power amplifier
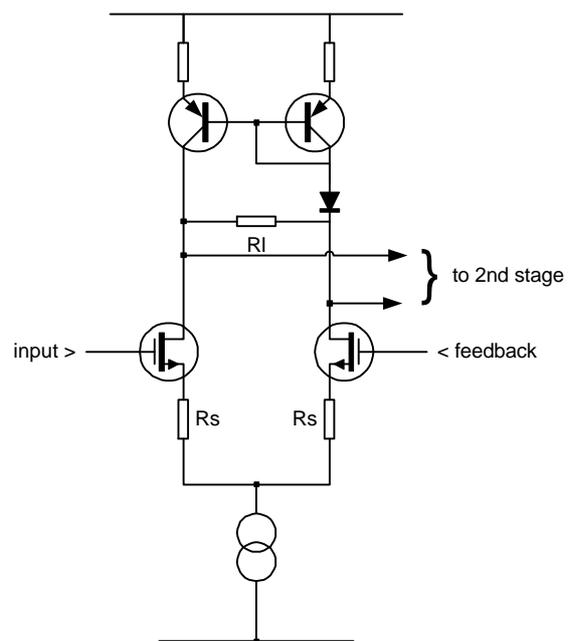
which excelled in all technical areas. To control and define the transfer function of the amplifier precisely an unconventional arrangement consisting of four stages, instead of the usual three, was designed. This design allowed total flexibility in optimising the total loop gain and the distribution of compensation poles and zeros.

Input stage

This is constructed around a dual J-FET pair. Heavy local feedback is applied by means of source resistors which reduces the transconductance of this stage. This does reduce the maximum available gain but it provides benefits in a number of areas. Use of source resistors linearises the transfer function and protects against driving the input stage into the nonlinear region where one or more devices have been 'cut off'.
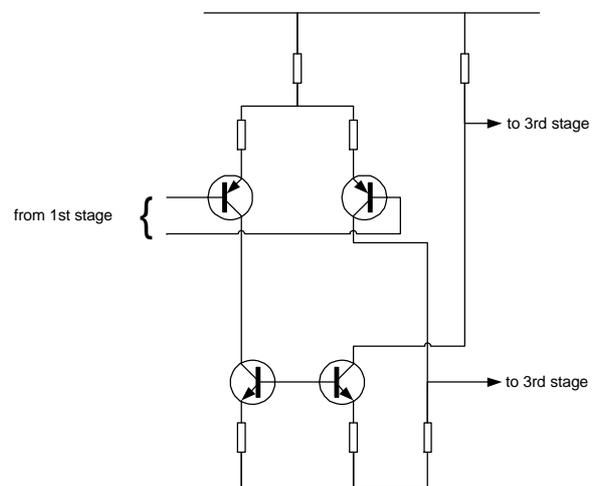
Current balance is achieved between the input FET devices by means of current mirror drain loading which further reduces non linearity of the transfer function.

With only current mirror loading the input stage would be configured solely as a transconductance stage with all the attendant problems of stage gain defined by semiconductor devices. Thus a resistively defined drain load is provided which results in a first stage voltage gain at low frequencies defined by 1% resistor values. The defined voltage gain of this stage is 20 x (26dB) The drains of the FETs are the nodes from which the signal is taken to drive the intermediate stage.
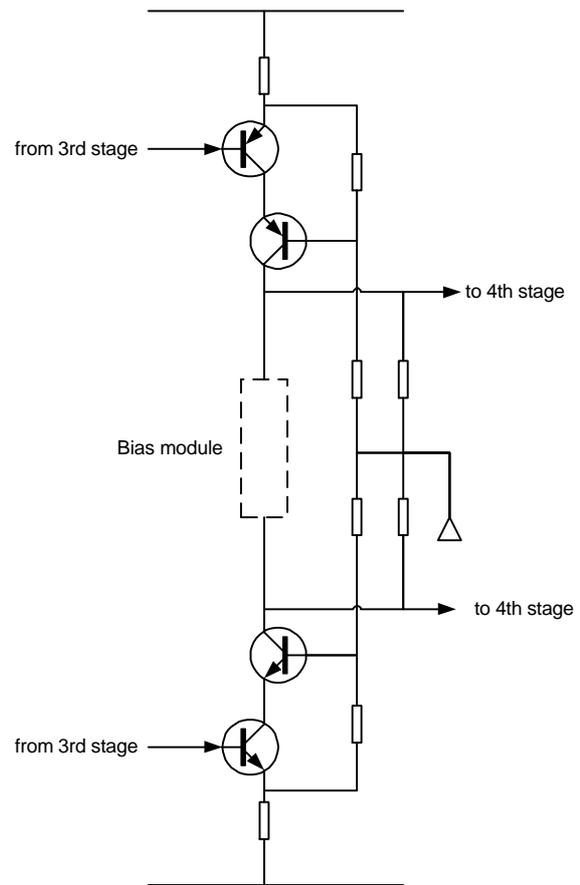

Intermediate stage

The drain pins of the dual J-FET are connected to a bipolar differential pair which are also configured in the consistent manner

with emitter degeneration resistors and passive collector loads which again provide a consistently and accurately defined voltage gain of 6 x (15.5dB). In addition to providing a stage of gain this amplifier carries out the functions of converting an unbalanced signal from the input differential amplifier into a level shifted differential drive for the voltage amplifier stage
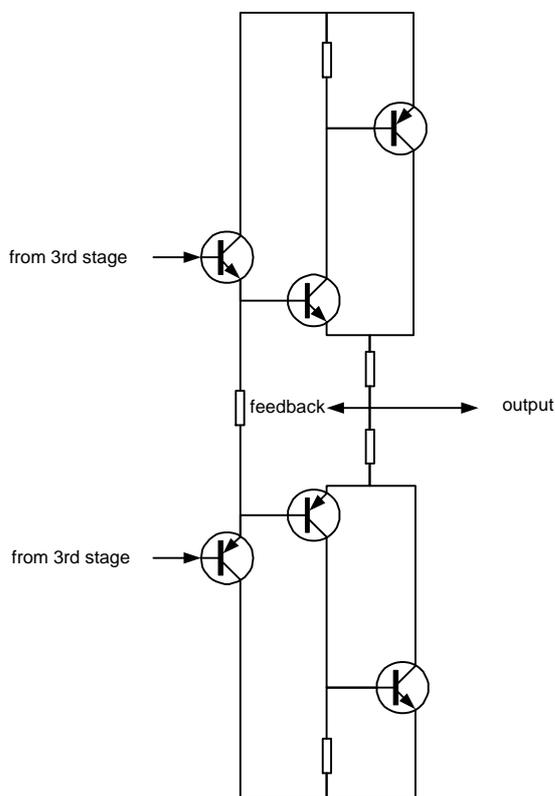
Voltage amplifier

This third stage is configured as a fully complementary bipolar push pull common emitter collector coupled amplifier. In the 100P and 125M incarnations the collectors have to swing through 120V while conducting sufficient current to drive the ß multiplying output stage without gross modulation. Care has been exercised to implement a highly linear configuration so as to minimise the demand for feedback as a distortion reduction mechanism.

To enhance the bandwidth and minimise the problems induced by Early effect the complimentary amplifiers are cascode designs. As previously the stage voltage gain is once more defined using resistors in the cascode emitters and to define the collector load impedance. To minimise the collector base voltage modulation of the common emitter amplifier the cascode biasing voltage is coupled to the emitter resistor. The benefits of this enhancement of the cascode amplifier is analysed in detail by Hawksford [8].

Output stage

Although the accepted nominal load impedance for audio loudspeakers is 8 ohms the true value of the minimum impedance presented to the amplifier is often as low as 2 ohms. To put this in context for an understanding of the implications as far as the power output stage is concerned then whereas the peak level of a 100 watt amplifier has to deliver 5 amps into the 8 ohm load this rises to 20 amps! should this load fall to 2 ohms. The preceding voltage amplifier has of the order of 15 mA of quiescent current. This falls far short of the 20+ amps required by the loudspeaker. Unless gross distortion is allowed only a small percentage modulation of this

quiescent current is allowable in a high fidelity amplifier. Therefore the output stage must buffer the voltage amplifier from the demands of the load impedance.
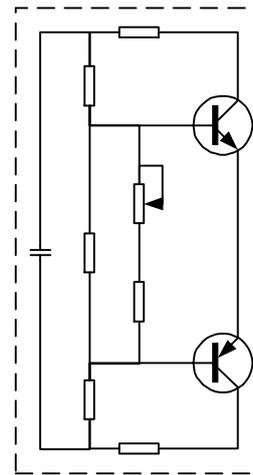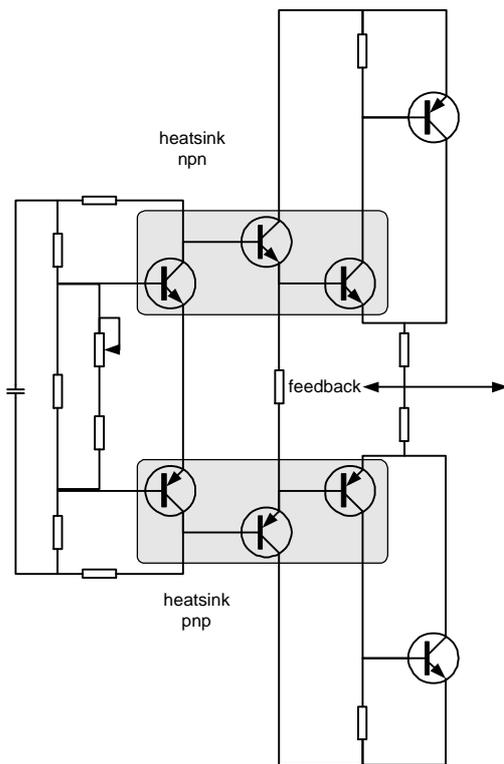
To carry out this task the output stage must deliver amps while drawing from the voltage amplifier mere microamps of current. The ability to produce music reproduction in a clean and effortless manner is in no small way linked to the capability of the power stage. Calculations quickly reveal that current multiplication of the order of between 10^4 and 10^5 are necessary. To achieve this all F3 amplifiers use a triple ß multiplying configuration. The second and third transistors are a complimentary Darlington pair connected to provide unity voltage gain. This transistor pair is driven from an emitter follower. DC current multiplication of the order of 400,000 can be achieved.

All F3 power amplifiers are provided with sufficient 200 watt 200V bipolar high f_t power transistors to drive 2 ohm loads at very low levels of distortion. Much discussion has been given over to the virtues and weaknesses of bipolar versus FET power devices but after close analysis of the technical performance parameters of the modern 20+ MHz f_t bipolar transistors it was clear that the optimum solution could be engineered from bipolar components.

Biasing module

Conventional triple emitter follower output stages result in six base - emitter junctions appearing in series in the temperature compensating chain. To track the variation in v_{be} with temperature of all six junctions it is necessary to mount all six devices along with

the compensation device on the power heatsink.

In the case of the F3 output topology this is no longer necessary because the power output devices are contained within a feedback loop of their own and only the preceding emitter follower pair have to be compensated. There is now no need for this function to take place on the heatsink.

In addition the optimum layout was achieved by separating the positive and negative halves of the output stage. As these sections are made up of pairs of NPN and PNP it was decided that the optimum thermal tracking would be achieved use a complementary NPN / PNP biasing module where NPN and PNP v_{be} / temperature variations were tracked by the same polarity transistor.

Compensation

The benefits of the circuit design described above are completed with the flexibility available in tailoring the compensation to achieve the optimum performance. The analysis of multiple pole zero amplifier topologies presented in the paper by Takahashi & Chikashige [9] showed clearly the benefits of multiple pole compensation. Combining this with the decision to locate the dominant pole on the output of the first stage coupled with sufficient emitter transconductance reduction that the input differential pair can withstand a full 2V step transient without either device reaching cutoff results in an amplifier which can never be driven into slew rate limiting. With the slew rate defined by the transient response of the first stage the voltage amplifier is no longer vulnerable to the classical slew rate limiting problem identified in the papers of Otala and others.
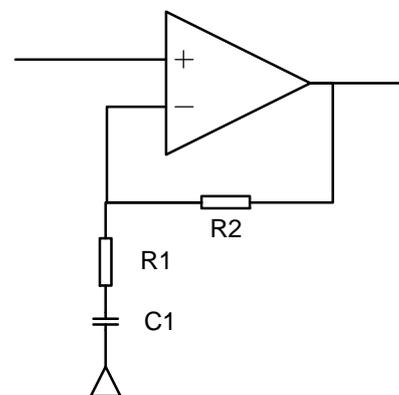
An ideal amplifier would be made up of a number of stages each of which had infinite bandwidth. If this was the case then the amplifier could be compensated for unconditional stability using just the two poles and a single zero. However in the real world transistors have a finite bandwidth which results in each gain stage introducing a pole which results in additional phase shift. The accumulation of these semiconductor poles would be such that it would be impossible to close the feedback loop. However it is possible to introduce passive zeros at the identical frequencies of the semiconductor poles and thereby 'cancel' their effect. In this way we can create an open loop Bode response which results in a unconditionally stable amplifier with the maximum possible bandwidth and lowest non linearity. TAG McLaren Audio has used sophisticated RF network analysers to measure the Bode and Nyquist responses of the uncompensated amplifier to identify these semiconductor poles. It is then possible to calculate precisely the cancelling zeros, apply them to the circuit and then measure the response a second time to ensure that the amplifier will be unconditionally stable when the loop is closed.

Servo

The simplest way of resolving the low frequency response would be to direct couple the amplifier input and feedback path. This would result in eliminating the signal passing through any coupling capacitors and there would be no modification to the phase or group delay in the transfer function at low frequencies. This approach has many dangers not least of

which is that the gain of the amplifier at dc is x 28 (29dB). Any offset voltage generated by imbalance at the input dual J-FET will be multiplied up by 28 times. In addition should the amplifier be used with any preamplifier that has a dc offset at its output this will also be multiplied by the power amplifier. Despite the rating of loudspeaker being in the area of 100+ watts for music this is not the case for dc signals. Without any motion of the base drive unit to provide forced cooling the voice coil can be burned out at comparatively low dc power levels.
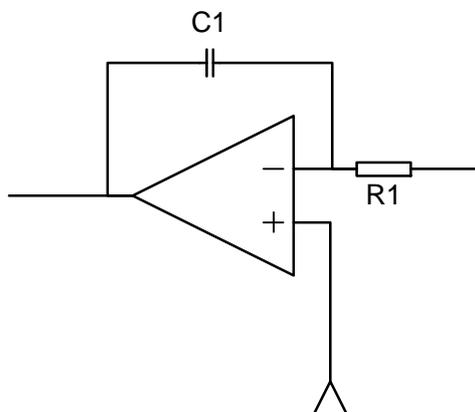
The conventional method of dealing with this issue was to reduce the gain to unity at dc with the use of a capacitor in the feedback path.

The shortcoming with this approach lies in the fact that the feedback potential divider which establishes the gain should use low valued components to minimise the noise generation. Unfortunately to achieve a low frequency -3 dB point it is necessary to use a large valued capacitor which is located where there is no dc signal to bias a conventional electrolytic capacitor.
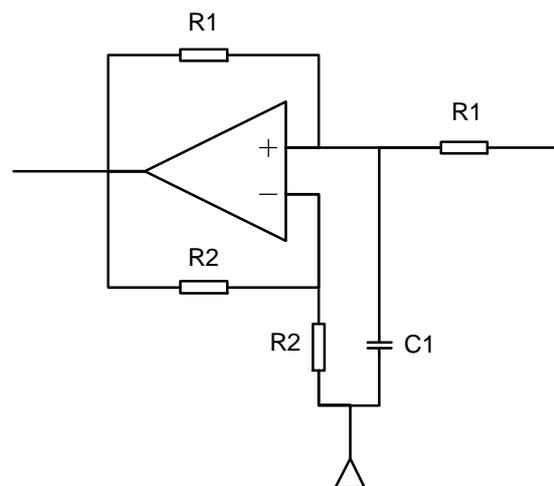
The more elegant solution to this problem is to use the properties of an integrator to reduce the gain to a negligible value at dc.

The dc offset of the power amplifier is then determined by the offset voltage properties of the operational amplifier used at the heart of the integrator.

C1

R1

However because the conventional integrator shown above is inverting the signal would have to be injected into the +ve terminal of the power amplifier in order that the integrating servo provides negative feedback and the amplifier remains stable. If this is carried out with an amplifier with a direct coupled input then the correcting servo signal will appear as a dc voltage on the input terminal which is undesirable.

To eliminate this problem a different topology of non inverting integrator has been designed so that stable servo feedback can be achieved with the correction signal returned to the -ve amplifier input

R1

R1

R2

R2   C1

SOA monitoring

Continuous monitoring of the instantaneous current through and the voltage across the power transistors allows the amplifier to deliver the maximum power to the load within the specification limits of the power devices. However should the demands exceed the devices capabilities, by example an accidental short circuit on the speaker terminals, then the monitoring circuit will disconnect the load from the amplifier until such time as the problem is removed. The crucial aspect of this design is that, unlike semiconductor clamping systems working within the forward gain of the amplifier, there is no degradation of the amplifiers transfer function or alteration of the stability margins right up to the maximum power delivery of the F3 power amplifier.

Conclusion

The above description has outlined the technical sophistication that is contained within the circuit topology of the F3 series power amplifiers. These products have for many years set the benchmark performance in their market sector. This has come about as a result of the painstaking attention to detail design covering all aspects of the requirements for the highest audio fidelity.

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