Input stage = JFet's

- 2SK389BL/2SJ109BL
  - bias crent adjustable (set to 7.7mA in LTspice)
  - Vds = 8.7V
- floating cascoded with IRF9610/610
- adjustable DC-offset control (will be built in with prototype and evaluated whether necessary)

Vas stage = MOSFet

- IRF9610/610 (fairchild) set to +-17.5mA bias current
- common base design is chosen because of simulated higher stability => gain margin increased compared to "standard VAS"
- Chosen because easy obtainable and high Vgs (compared to 2SK2013/2SJ313)
  - The higher Vgs will lead to a higher gain (higher value of loading resistor in LTP is necessary)
- see http://www.diyaudio.com/forums/solid-state/217528-low-power-mosfets-complementary-pairs.html
- Loading resistors towards ground are used to flatten the Open Loop Gain
  - More values will be used during prototyping and evaluated

Bias spreader

- Will be designed/tested during prototyping

Driver stage = Mosfet

- 2SK2013/2SJ313 (Toshiba) set to +-60mA bias current
- Chosen because of
  - their good complementary parameters (Ci and S/Rd)
  - having a bunch of them
  - low Vds (not that important because of seperate PSU for driver section)

Output stage = BJT

- Sanken 2SC2922/2SA1216
- Biased to +-158mA using 0R12 emitter resistors ==> Class A output power of 9Wrms/8R
- 10Ohm gate stoppers as proposed by John Curl
- During prototyping output can be connected to middle of Drivers (between two R10 resistors)

NFB

- Done with Dale RND55 resistors
- total of 29dB negative feedback (THX)
- To increase the second harmonic, a 1000k resitor is added between output and LTP output (See R45)

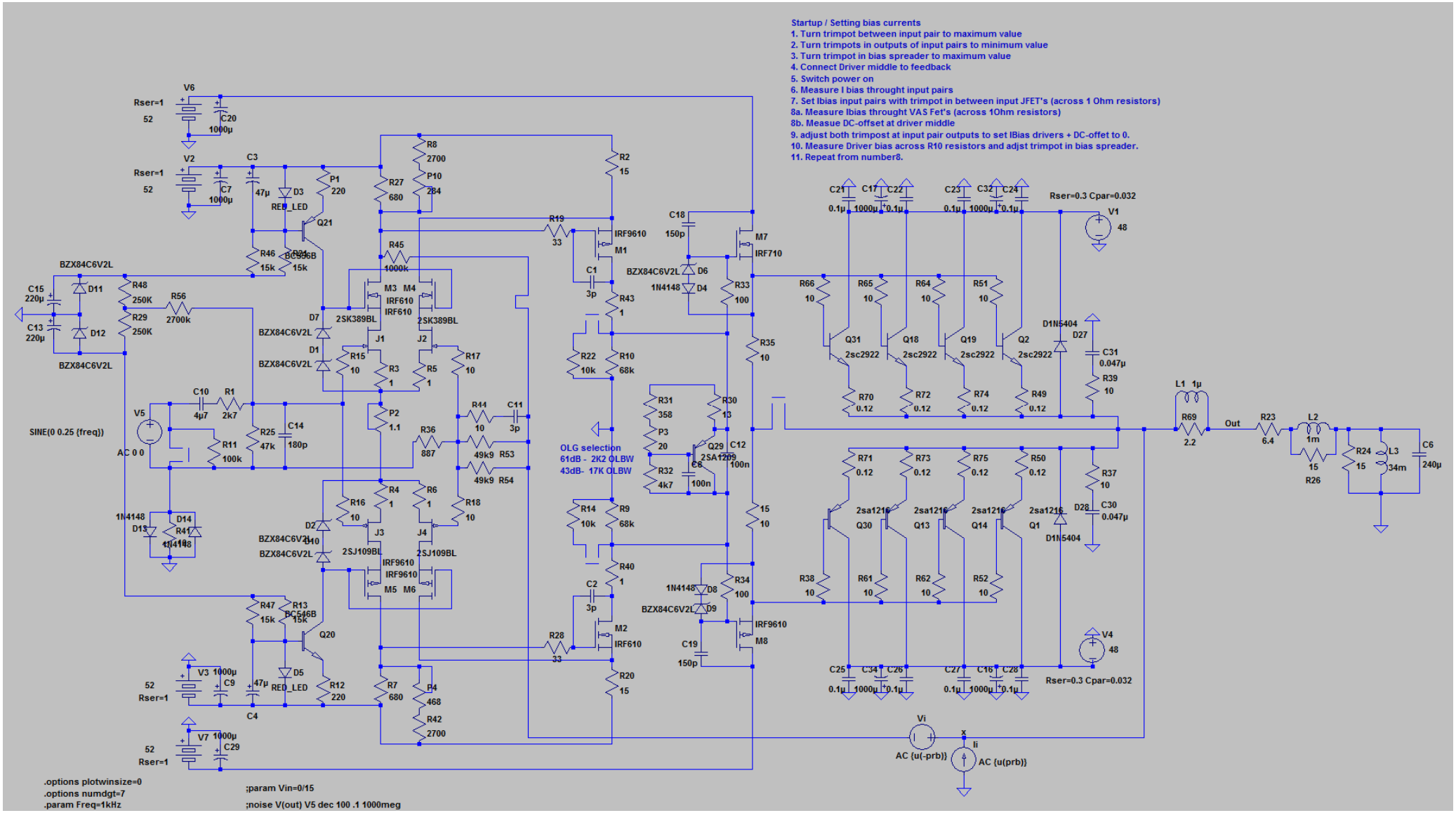
Power supply = mainly in seperate enclosure

- For output stage 2X50V
- For front end and drivers 2X59V (Cap multipliers will be used)
- See http://www.diyaudio.com/forums/power-supplies/247239-high-performance-dual-mono-psu.html
- In the amplifier enclosure a minimum of 20000µF/rail will be added close to the OPS PCB.

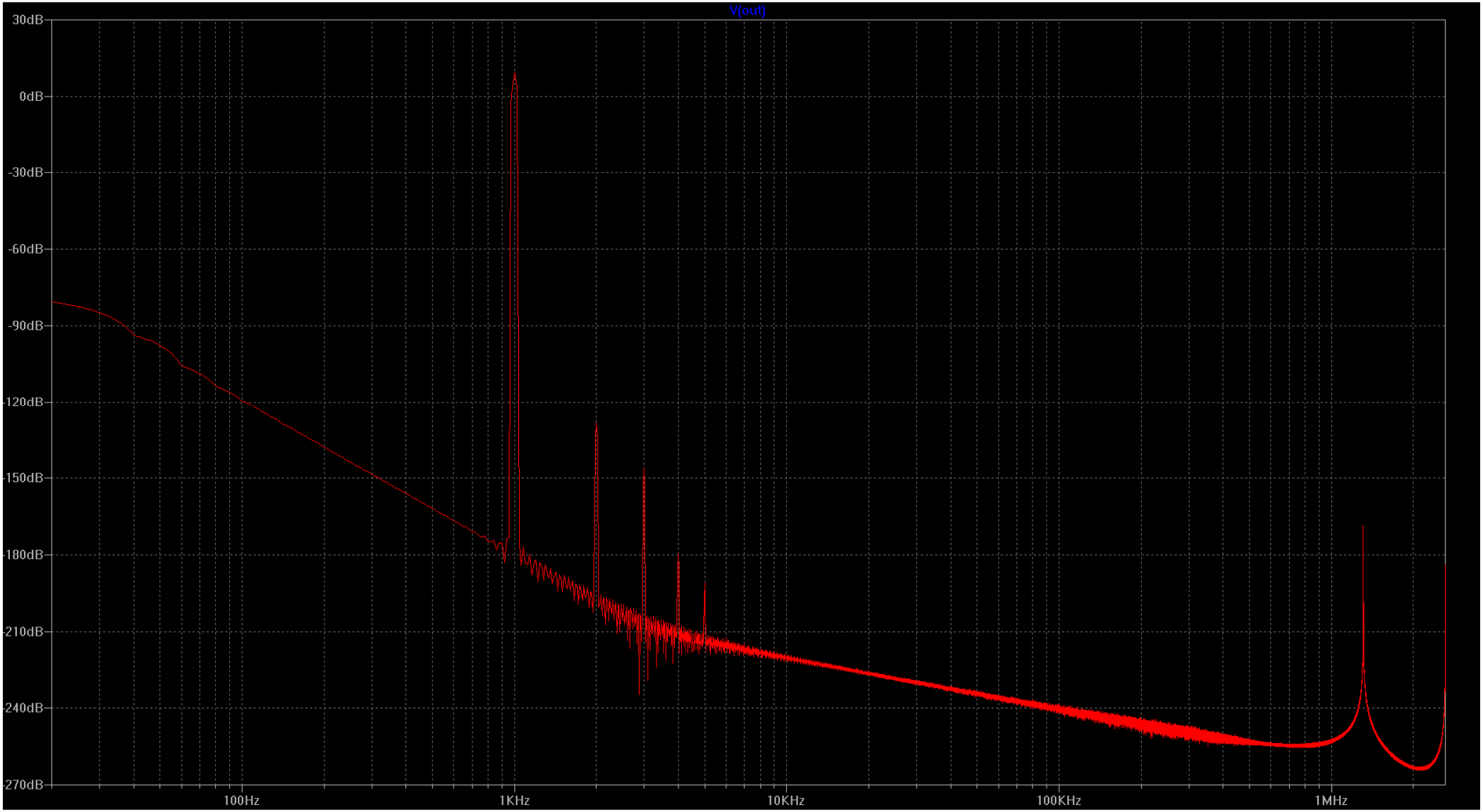
Enclosure

- Will be very hard looking to my previous amp
- see http://www.diyaudio.com/forums/solid-state/198209-amp-design-subwoofer-wideband-duty-13.html
- Or post 2837 http://www.diyaudio.com/forums/solid-state/96192-post-your-solid-state-pics-here-284.html

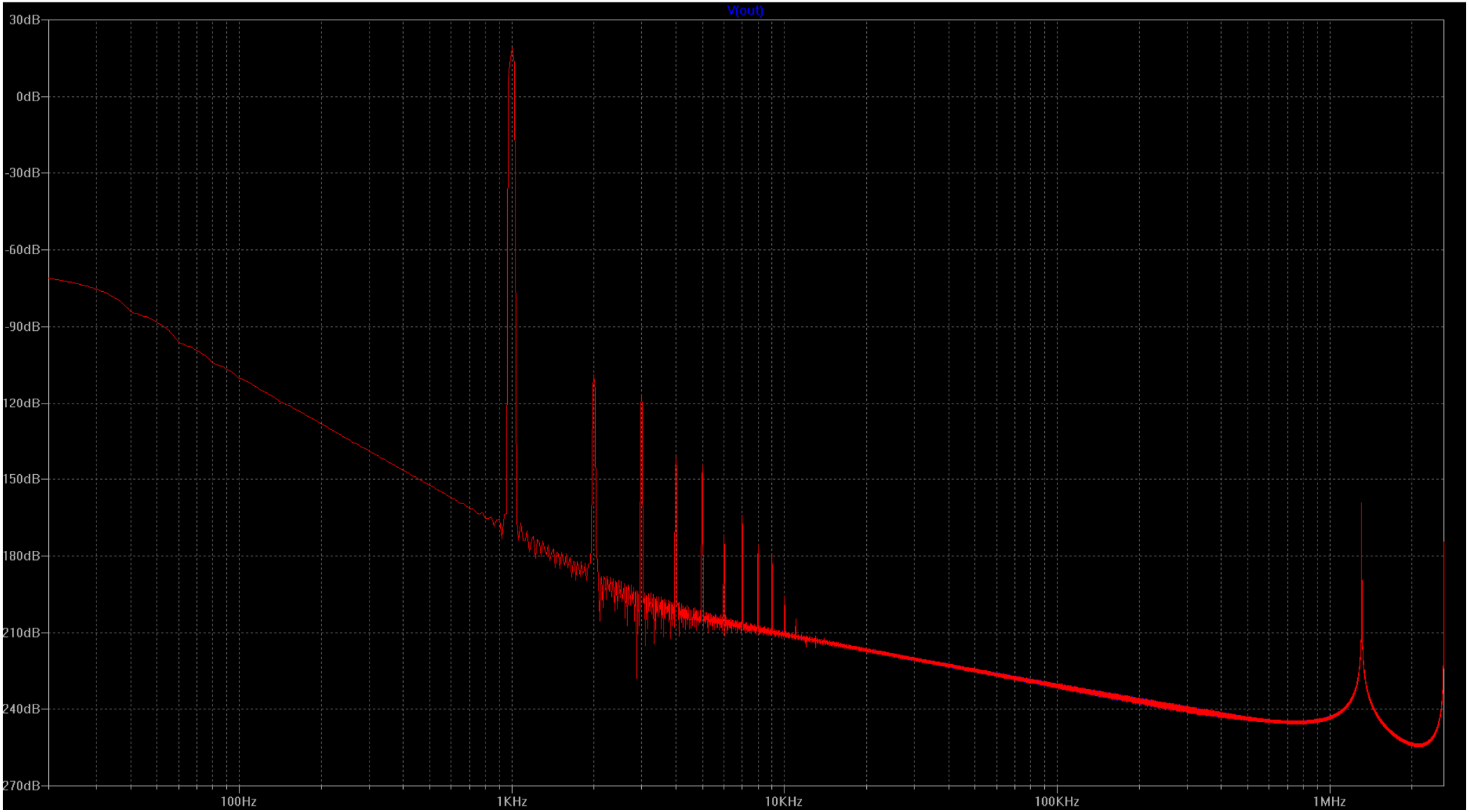
- Circuit 20131224



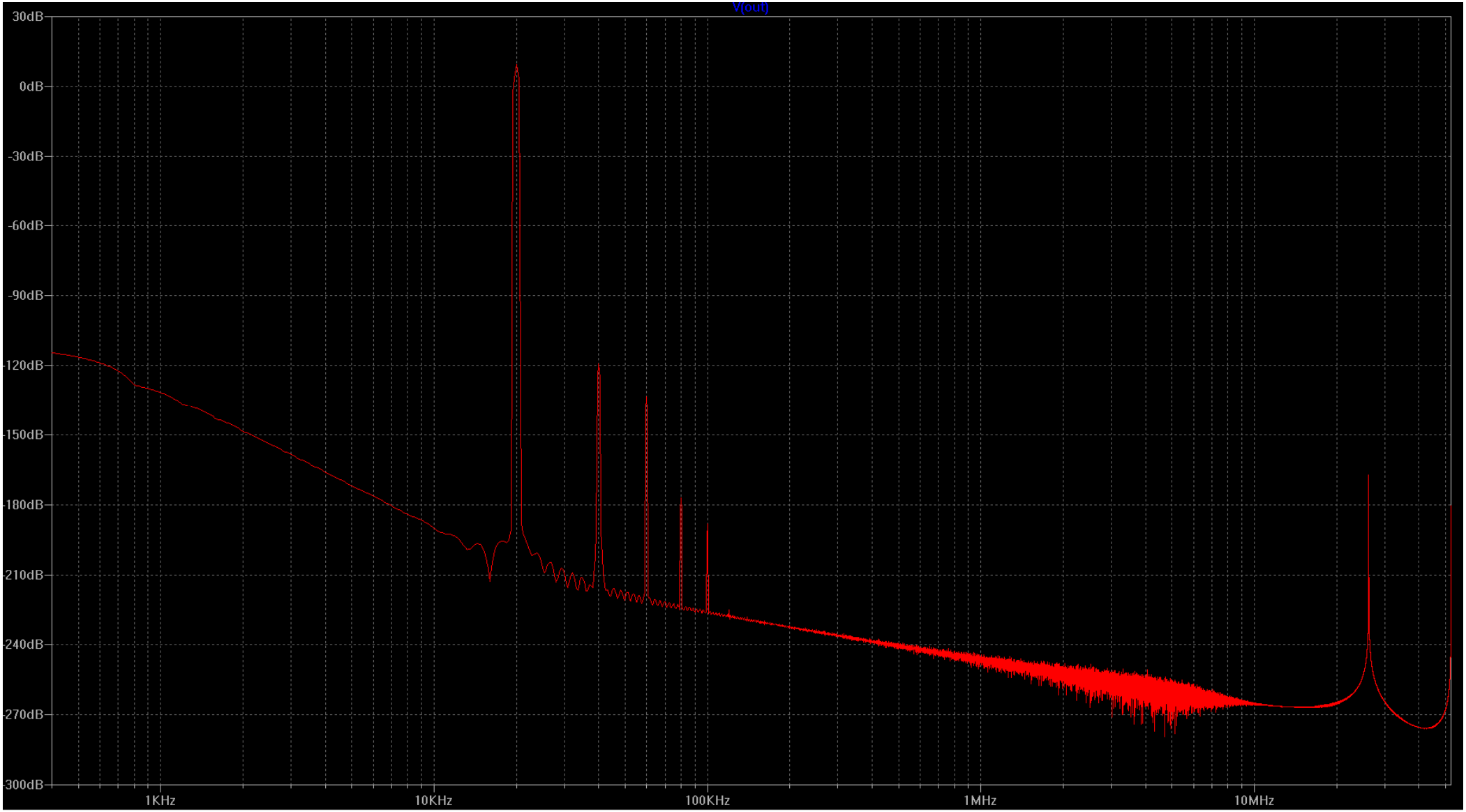
THD : 1KHz 1Wrms = 0.00005%



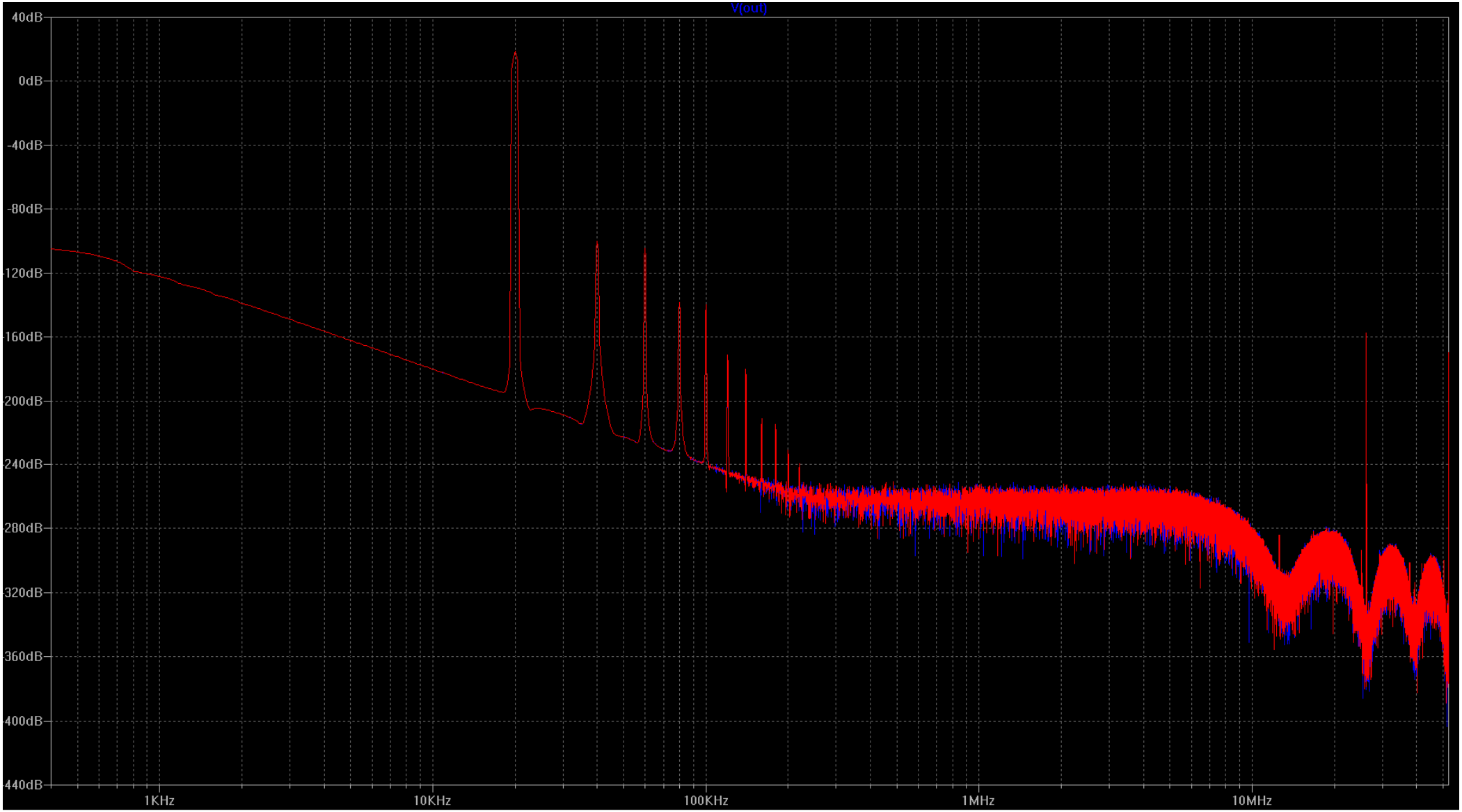
THD : 1KHz 10Wrms = 0.000064%



THD : 20KHz 1Wrms = 0.000038%

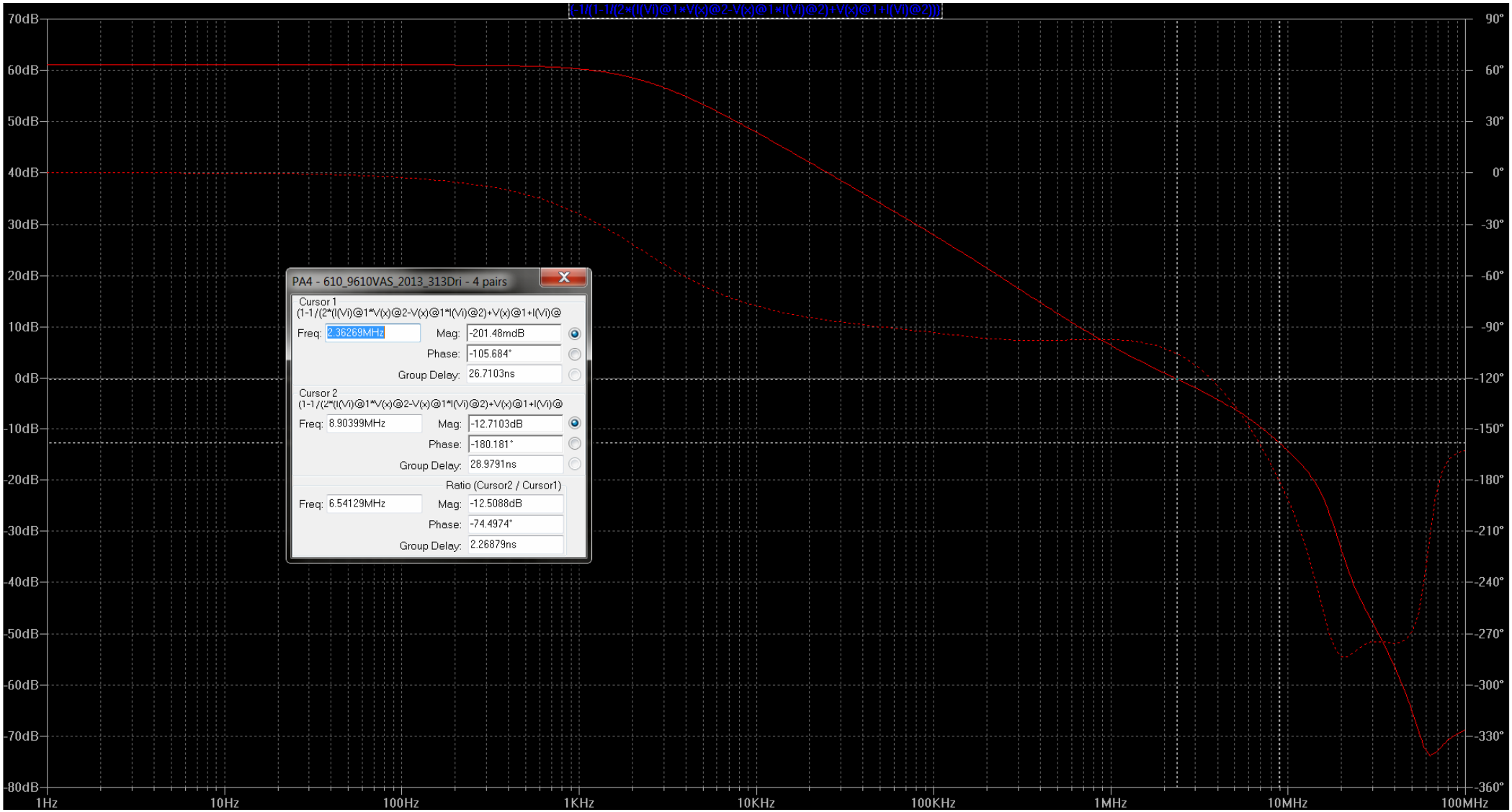


THD : 20KHz 10Wrms = 0.00013%



Phase and gain margin

- PM = 75°
- GM= 12.7dB
- UG = 2.36MHz



Prototype PCB for ouput stage (Front end and drivers will be on a second PCB close positioned inside the amp eclosure to the OPS PCB)