

University of California at Berkeley
Physics 111 Laboratory
Basic Semiconductor Circuits (BSC)

Lab 4

JFET Circuits I

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References:

Sedra & Smith	Chapter 5
Hayes & Horowitz	Chapter 3
Horowitz & Hill	Chapter 3

In this lab you will explore basic JFET characteristics, circuits and applications. You will build a JFET switch, memory cell, current source, and source follower. **Remember to keep your parts, do not lose them and do not return them to the parts cabinet.**

Before coming to class complete this list of tasks:

- Completely read the Lab Write-up
- Answer the pre-lab questions utilizing the references and the write-up
- Perform any circuit calculations or anything that can be done outside of lab.
- Plan out how to perform Lab tasks.

Pre-lab questions:

1. What is the maximum allowed gate current? What happens if this current is exceeded?
2. In a few sentences, explain how a self-biased current source works.
3. Explain how to use load line analysis as outlined in the background materials. Why does it give the equilibrium current for the self-biased current source?
4. Why does increasing a follower's source resistor decrease its JFET's transconductance? (Refer to the discussion just before 4.17.) Why does this degrade the performance of a source follower?

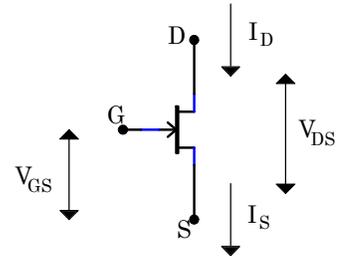
Do not forward bias the JFET gates.
Forward gate currents larger than
50mA will burn out the JFETs!

Background

JFET Transistors

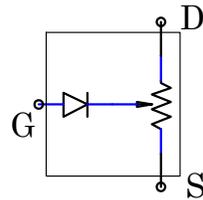
There are two principle types of transistors: bipolar transistors (BJTs), and field-effect transistors (FETs). The physical mechanisms underlying the operation of these two types of transistors are quite different. We will limit our study to FETs because their physical mechanism is simpler. FETs are subdivided into two major classes: junction field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs).¹ Since MOSFETs² burn out very easily, we will concentrate on JFETs. JFETs, particularly discrete JFETs, are less common than bipolar or MOSFET transistors, but will give us a good picture of how transistor circuits work.

Transistors are amplifiers; a small signal is used to control a larger signal. Typical transistors have three leads; in the case of a JFET, a *voltage* on one lead (called the gate) is used to control a *current* between two other leads (called the source and the drain). Of course, the gate voltage needs to be referenced to some other potential. By convention, it is referenced to the source. JFETs are drawn as shown to the right where the gate, drain and source (G, D, S, respectively) labels are normally omitted. Transistor voltages and currents are labeled by subscripts referring to the appropriate lead. Thus V_{GS} refers to the voltage between the gate and the source, I_D is the current into the drain, and I_S is the current out of the source. Under normal operating conditions, *no current flows into the gate*. Consequently $I_D = I_S$.



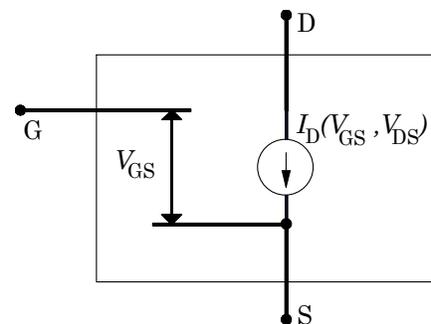
JFET Characteristics and the Transconductance Model

Under normal operating conditions, the JFET gate must be negatively biased relative to the source. **The JFET may burn out if the gate is positively biased.** The JFET gate and source–drain form a pn junction diode; a very simple model of the JFET is shown at right, in which the resistance depends on the gate bias. Since the gate is negatively biased relative to the source, the diode is reverse biased. Consequently the gate current will be negligible, thereby proving that $I_D = I_S$. Note that checking a JFET's internal diode with a DMM is a good way of determining if the JFET is working; the diode is usually blown out in broken JFETs.



A more useful JFET model replaces the variable resistor with a variable current source whose current depends on the gate voltage V_{GS} and the drain-source voltage, V_{DS} .

The drain-source current is largest when the gate-source voltage V_{GS} is zero, typically about 50mA. As V_{GS} is made negative, the current decreases. When the gate-source voltage V_{GS} reaches a critical value called the gate-source pinch off voltage V_S , the drain current I_D is cutoff entirely; no current flows. The value of V_S depends on the particular type of JFET (and even varies substantially between JFETs of the same type), but is typically around $-4V$. As V_{GS} is raised towards $0V$, current I_D starts to flow. A typical plot of the current vs. gate voltage is shown in Fig. 1 below. Simple models of JFET performance predict that the curve will be parabolic, but actual devices may differ substantially from this prediction.



¹ Actually, each type of FET is further subdivided into n and p-channel FETs, and, for MOSFETs, enhancement and depletion MOSFETs, but lets not get into all that!

² Static electricity easily destroys MOSFETs. They can be burnt out simply by walking across a room on a dry day while carrying them in your hand. Once soldered into a circuit, however, MOSFETs are quite robust.

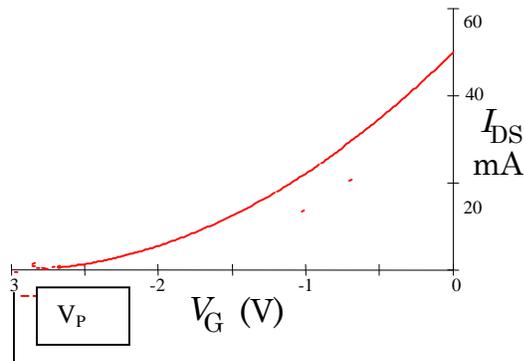
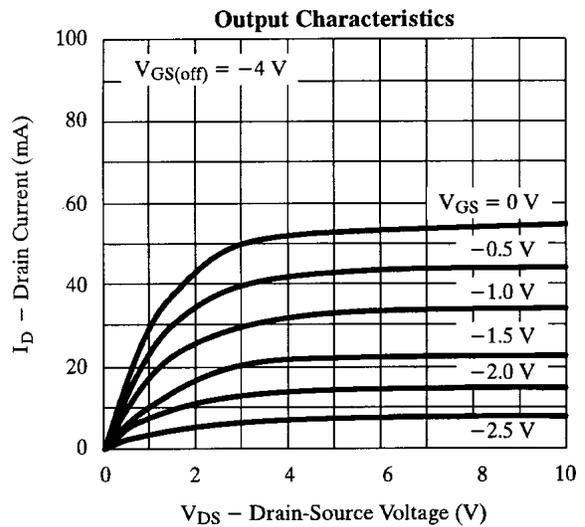


Figure 1: JFET Transfer Characteristic



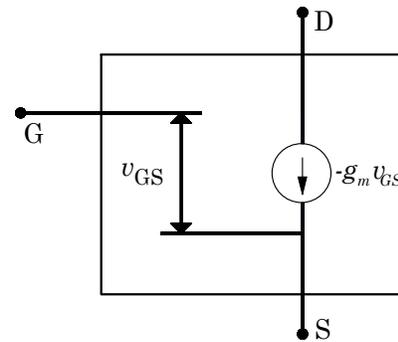
The source current also depends on the drain source voltage.

Two regimes are apparent in this graph: a low voltage “linear” regime where the output current is linearly related to V_{DS} , and a “saturation” region where the current is weakly dependent on V_{DS} .

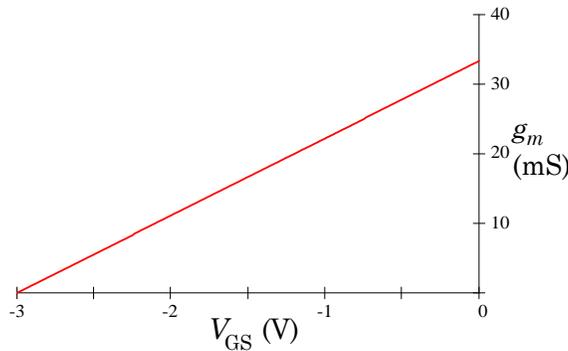
Small-Signal Transconductance Model

For small variations in V_{GS} , the JFET model can be linearized:

The input voltage³ v_{GS} and the output current i_D are related by the equation $i_D = -g_m v_{GS}$. The proportionality g_m is called the “transconductance”; “trans” because the gate voltage is transferred to the source current, and “conductance” because g_m has units of conductivity. As in any small-signal model, all constant voltage offsets and constant currents are ignored. In particular, the V_{GS} bias required to obtain the desired I_D is ignored; v_{GS} is centered around zero.

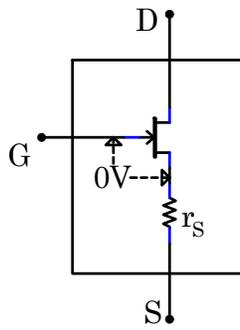


The transconductance is calculated by taking the derivative $g_m = dI_D/dV_{GS}$ (see graph below). Unfortunately, g_m depends on both V_{GS} and V_{DS} . For the JFET characteristic shown in Fig. 1, g_m is almost linearly dependent on V_{GS} .



³ We use capital letters for large signals quantities (like V_{GS}) and small letters for small signal quantities (like v_{GS}).

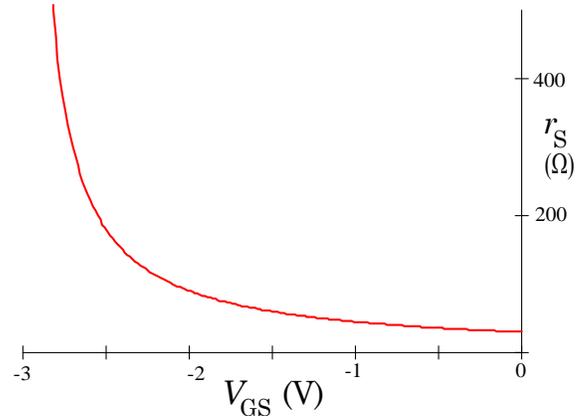
Small-Signal Source-Resistance Model



A useful variant of the transconductance model consists of an ideal JFET connected to a source resistor r_s .

The value of the source resistor is $r_s = 1/g_m$. For the JFET characteristics shown in Fig.1, the source resistance is shown to the right.

The ideal⁴ JFET passes whatever current is necessary to keep the gate and source at the same potential, hence the “0V” in the model’s drawing. Note that the ideal JFET and the source resistor r_s form an indivisible package. The ideal JFET’s source is internal to the package and is not accessible to the external circuit. As indicated by the label “S”, the “source” lead accessible to the external circuit is the lower end of the source resistor r_s .



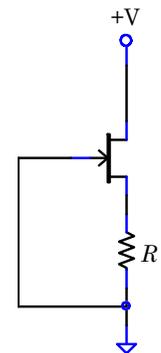
The equivalence of the two models is best established by an example. Consider a real JFET whose transconductance is $g_m = 0.01S$, driven by a voltage $v_{GS} = +0.1V$. How does the ideal JFET in the source resistor model keep its gate and source at the same potential? Drive enough current through the source resistor to raise the ideal source voltage to $+0.1V$. Since the source resistance is $r_s = 1/0.01 = 100\Omega$, this requires a current of $0.001mA$. But the transconductance model predicts a drain current of $i_D = g_m v_{GS} = 0.01 \times 0.1 = 0.001mA$. Thus, both models predict the same current.

Self-Biased Current Sources

Current sources are very important in modern circuit design. A typical Op Amp, for instance, might contain a dozen current sources. While a JFET operated in the saturated regime functions as a current source, it is not stiff enough for most applications. Moreover, its output current will vary substantially with temperature.

The self-biased current source depicted to the right is a much stiffer source.

As in any current source, the current through the JFET in this circuit is relatively independent of the voltage $+V$ across the circuit. Changing the value of the resistor R programs the size of the current.



The behavior of this circuit is not obvious. The circuit depends on feedback: the output of the circuit controls its input. Feedback is an extraordinarily useful and general circuit design technique that has almost magical power. The self-biased current source is the first of many feedback circuits that we will study in this course.

Let’s consider how the above current source might startup when power is first applied. Imagine that the $+V$ source is turned on abruptly, and no current is yet flowing through the JFET. Then the voltage drop across the resistor will be zero, and the gate source voltage V_{GS} will also be zero. But zero V_{GS} allows large currents to flow through the JFET, so the current will increase. As the current increases, a voltage drop will develop across the resistor, and the upper end of the resistor will become positively biased. *This means that the gate will become **negatively** biased with regards to the source.* Negative values of V_{GS} will start to shut the JFET off. Eventually, a stable equilibrium will be attained where V_{GS} is just right for the current flowing through the JFET. Once in equilibrium, if the

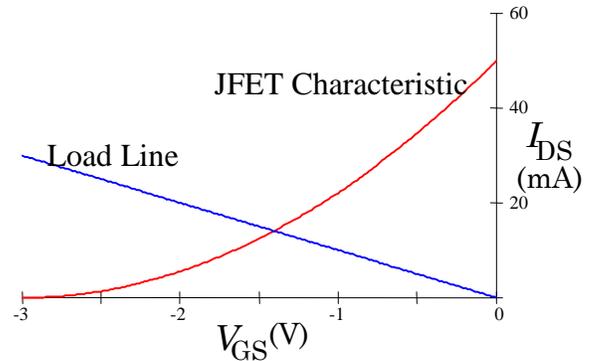
⁴ The JFET is ideal in the sense that its transconductance is infinite. Any desired current can be obtained with an infinitesimal v_{GS} , consequently $v_{GS} \approx 0$.

current were to increase, the drop across the resistor would increase, the JFET source would become more positive, V_{GS} would become more negative, and the JFET would shut off slightly. If the current were to decrease, the drop across the resistor would decrease, the JFET source would become less positive, V_{GS} would become less negative, and the JFET would turn on slightly.

In sum, the circuit regulates its output by feeding back a signal proportional to its output (in this case, the voltage across the resistor) into its input.

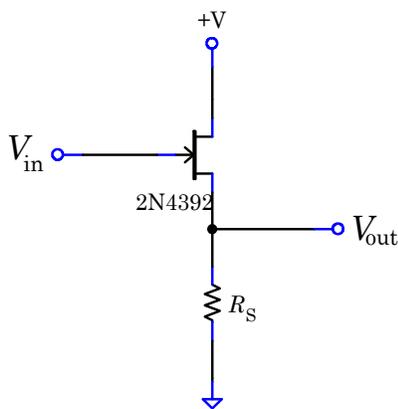
The current through the source can be predicted by load line analysis. On a graph of the gate voltage-drain current characteristic, draw the resistor load line $I = -V/R$.

The intersection of the two curves gives the equilibrium current.



Source Followers

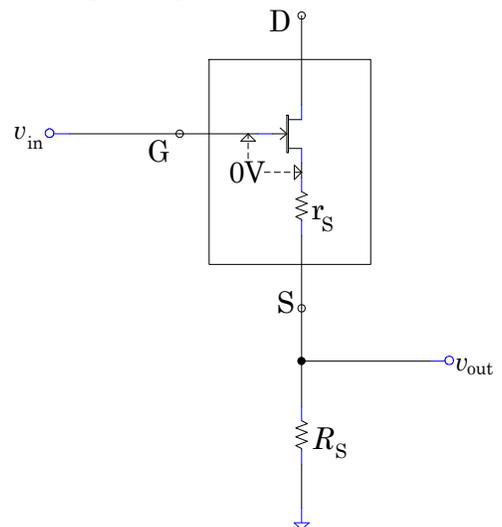
A description of a self biasing follower is in Sedra & Smith 2nd Ed. Pages 282 through 287.



A follower is a circuit whose output voltage equals its input voltage. Since followers have no voltage gain, it might appear that they are useless. However, followers can have large *current* gains, which may be more important than voltage gain for high input impedance sources. For example, photomultiplier⁵ tubes are commonly used light detectors. Although such tubes put out reasonably sized voltage signals, their large output impedance limits their output current, and hence their output power, to relatively small values. Typical tubes might have an output impedance of $1M\Omega$, and put out a signal of $10mV$, leading to an output current of only $10nA$, and an output power of $100pW$. Such a tiny output power makes the photomultiplier signal difficult to use. But if the signal were fed into a 100Ω output impedance follower, the maximum output current would increase to $100\mu A$, and the power to $1\mu W$, for a power gain of 10^4 .

A particular type of follower, a source follower, can be constructed from a self-biased current source. Instead of grounding the gate, the gate is driven by the input signal source.

The circuit's behavior changes little from that of the current source; the JFET adjusts its current to keep V_{GS} at the appropriate value for this current. Note how feedback manages to keep the gate reverse biased; if a large positive voltage attempts to forward bias V_{GS} , the resulting increase in the current through R_S immediately increases the source voltage and forces V_{GS} negative. The follower's small signal behavior can be described more accurately by replacing the JFET by its source-resistance model.



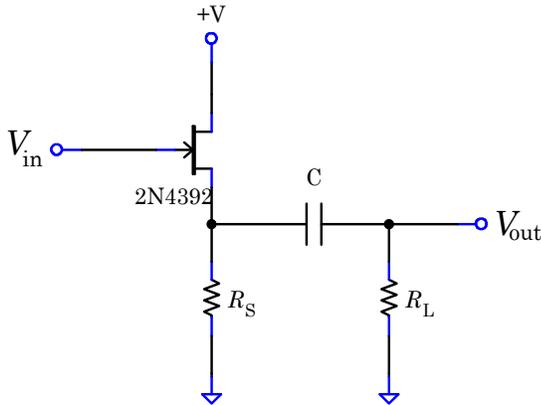
⁵ Some photomultiplier tubes can detect single photons. Note that not all photomultiplier tubes have high output impedances.

Remember that the ideal JFET keeps the internal source at the same potential as the gate. The model reduces to a voltage divider driven by a voltage-controlled voltage source.

Thus the output of the circuit is

$$v_{out} = \frac{R_S}{r_s + R_S} v_{in} \quad (1)$$

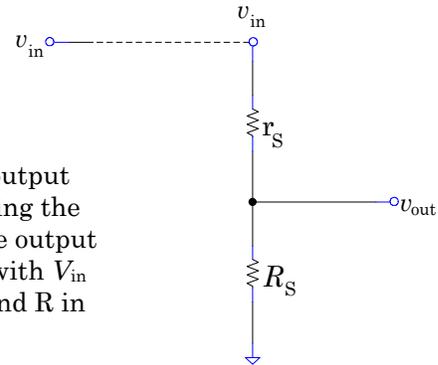
So long as r_s is much less than R_S the output voltage will closely follow the input voltage.



We can calculate the output impedance by measuring the resistance between the output terminal and ground with V_{in} shorted. It is just r_s and R in parallel, so

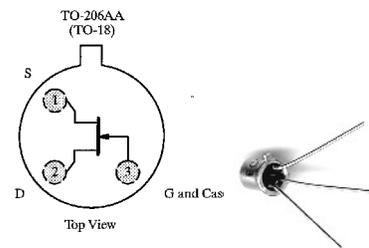
$$Z_{out} = \frac{r_s R_S}{r_s + R_S} \quad (2)$$

As R_S is normally chosen to be much bigger than r_s , the output impedance is approximately $Z_{out} \approx r_s$.



Packaging and Leads

Transistors are manufactured in many different packages and sizes. Ours come in a metal can. The leads are arranged in a triangle; the gate lead is the first lead clockwise from the tab when looking down (onto the can end, not the lead end) on the JFET.



When inserting the JFET into the breadboard, there is no need to squash the leads out horizontally. In fact, doing so risks accidentally shoring the leads to the case.

Instead, just bend them out gently so that they form a triangular pattern, which will insert into the transistor sockets on the breadboard.

Many JFETs, including the 2N4392, are symmetrically constructed. The source and drain can be exchanged without changing the device behavior. But for simplicity, use the correct source and drain leads. Asymmetric JFETs, in which the source and drain cannot be exchanged, are normally drawn with an offset gate lead.

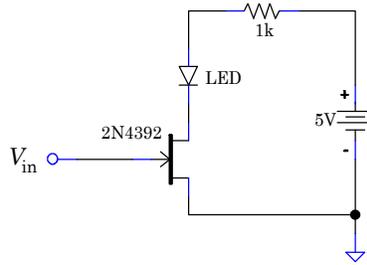
In the lab

The properties of JFETs vary substantially from sample to sample. Unless otherwise noted, use the same JFET for all subsequent measurements in this lab and in some of next week's lab. Make sure you keep your JFET separate. Also build neat circuits with short wire length to keep noise problems to a minimum.

4.0 Test that your JFET is working by measuring the resistance between the various pins. Explain how you did this.

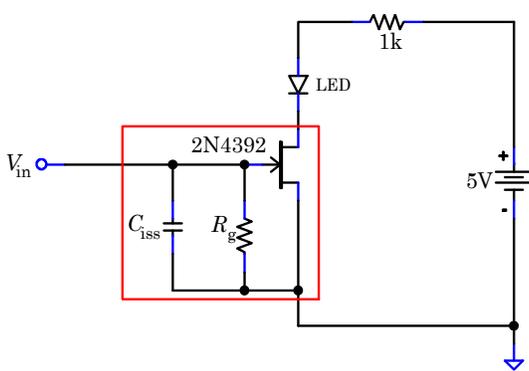
(A) JFET Switch

4.1 JFETs can be used as electronic switches. The circuit below switches an LED on and off.



Touch the gate lead to ground to turn the LED on, and touch it to -12V to turn the LED off. So far, this switch is not very impressive; we could just as well have switched the LED on and off by moving its own lead rather than the JFET gate lead.

Place a 2.2M resistor in series with the gate lead. Can you still switch the LED? From 4.15, you know that the LED will not light when driven by a 2.2M resistor. The JFET allows us to control the substantial LED current with the very small signal available through the 2.2M resistor.



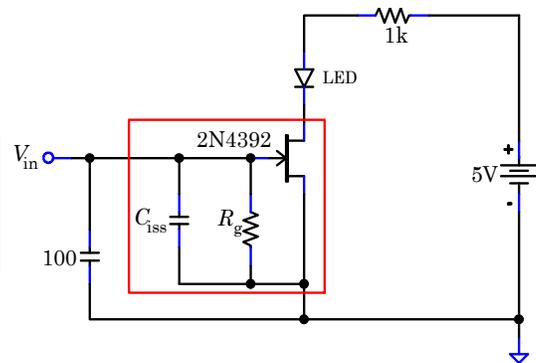
(B) Memory

You may have noticed that the JFET switch remembers its last setting. Touch the gate to -12V for an instant and the LED stays off for a while; touch the gate to ground and the LED stays on. This effect is the basis for the dynamic RAM (Random Access Memory) found in computers⁶, and results from the JFET's intrinsic gate capacitance C_{iss} and very high gate resistance R_g . When the gate capacitor is discharged, V_{GS} is zero and the JFET switch will be on. But when the capacitor is negatively charged, the JFET switch will stay off until the capacitor discharges, i.e. for a time on the order of $R_g C_{iss}$. The circuit

can be redrawn with a JFET model (shown above) that includes these effects.

The memory time can be extended by adding an external capacitor.

4.2 Measure the “forgetting” time with and without an external 100pf capacitor. From these two times, determine the approximate values of C_{iss} and R_g . Note that the resistance R_g is very high.⁷



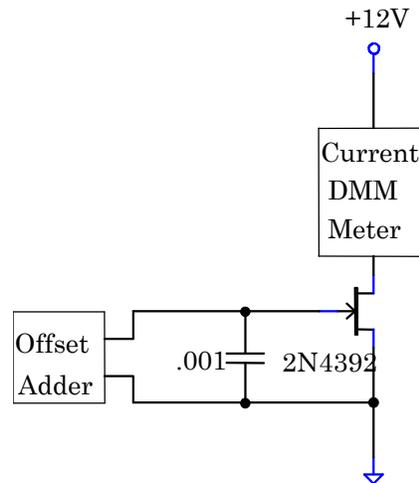
⁶ Computers use two types of memory. Static RAM remembers forever, but is relatively expensive and cannot be packed tightly on a chip. Dynamic RAM is cheaper and smaller, and functions very much like the memory cell here. However, the gate capacitance is very small for the FETs used in Dynamic RAMs. The computer must remind, or refresh, the memory of its state every few milliseconds; first it has to read each memory bit to find out what state it is in, and then refresh the memory bit by the equivalent of touching its gate to the appropriate potential.

⁷ The capacitance and leakage resistance of the breadboard itself will influence your measured values by lowering the input resistance and increasing the capacitance.

(C) JFET Gate Transfer Characteristics

In many of the following exercises, you will use the DMM to measure current. Remember that the voltage drop across the DMM is not zero!

4.3  Build the circuit below. **Check your circuit before turning the power on; it is easy to burn out the JFET and the DMM!** Make sure the offset adder is turned all the way negative to avoid JFET burnout.



Use the scope or another DMM to measure the gate voltage. The $0.001\mu\text{F}$ capacitor is in the circuit to suppress parasitic oscillations.⁸ First find the most negative voltage for which drain current flows through the FET.⁹ Then roughly determine the relationship between current and gate voltage by increasing the gate voltage to zero, recording the current at approximately five points.



Obtain the detailed JFET transfer characteristic with the computerized JFET Transfer Tracer. (See Appendix III for how to use the JFET Curve Tracer and how to connect the JFET leads.) Use the Tracer's analysis option to fit the transfer characteristic to a parabola, and to find the transconductance and source resistance r_s . How close is the characteristic to a parabola? Is it at least a parabola over some limited range? Plot all your data, and add the points that you took by hand to the transfer characteristic curve. For a gate voltage of -1V , find the transconductance directly by differentiating the transfer characteristic curve, and check that your value agrees with the value automatically calculated by the Curve Tracer.

The 2N4392 JFET is designed to be operated as a switch, and its transfer characteristic is far from ideal.

4.4 Get a new JFET for this exercise only. You may have noticed that at fixed gate voltages, the higher currents drift downwards with time. Investigate this effect: Set the gate voltage for a current of 1mA , and watch the current for a minute. Does it drift? Next set the current to approximately

⁸ Parasitic oscillations are high frequency, spontaneous oscillations. In this case, they would be visible by using the scope to look at the JFET drain. They are caused by unintended parasitic capacitances between the JFET leads, typically from having two wires too close together. Next week's write-up will discuss parasitic oscillations further.

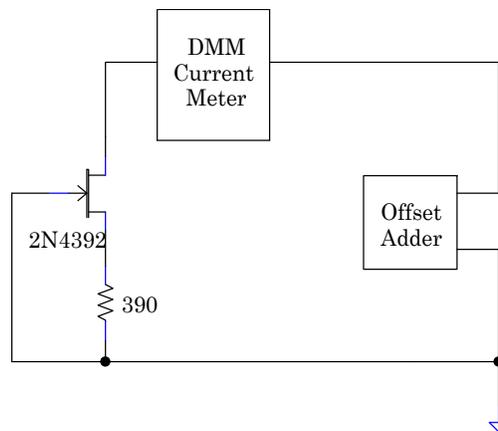
⁹ Don't be fooled by currents on the order of the lowest resolution measurable by the DMM. If the current doesn't depend on the gate voltage, these base-level readings are from the noise floor of the DMM. Find the gate voltage that just starts to increase the current.

15mA. Now does it drift? How much power is being dissipated by the JFET? Is the JFET hot? (Be careful, touch the JFET gingerly!) Obtain a can of circuit cooler.¹⁰ Spray the JFET for two seconds, and watch the current. How does it change?

Overheated components are a frequent cause of circuit failure. A common diagnostic technique is to spray a suspect component or circuit with circuit cooler, and see if the circuit begins to work again.

(D) JFET Source-Drain Output Characteristics

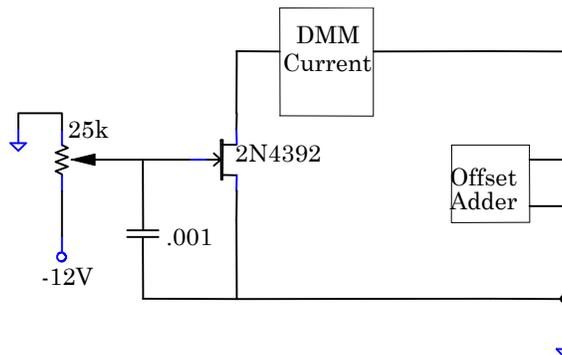
4.5 Build the circuit below.



Set the Offset Adder to +8V (at the drain, not directly at the Offset Adder). Measure and record the current going through the JFET. If the current is not between 4 and 8mA, adjust the value of the resistor until it is.

Do section 4.8 now also before you take apart the circuit.

4.6 Investigate the effect of the source drain voltage with the circuit below. Set the Offset Adder to +10V, and adjust the potentiometer to give approximately the same current as you measured in 5.5. Measure and record the potentiometer voltage. **Do not touch the potentiometer for the remainder of this exercise.**



Measure and graph the output current as a function of the Offset Adder potential. Use only positive potentials.

¹⁰ Circuit cooler works by spraying pressurized freon onto the FET, thereby cooling it by evaporative cooling and giving us all UV-induced skin cancer twenty years hence. **Moreover, circuit cooler is expensive. Spray for only a second or two. Not much is required.**

Now set the Offset Adder back to +10V. Briefly spritz the JFET with circuit cooler. By how much does the current change?



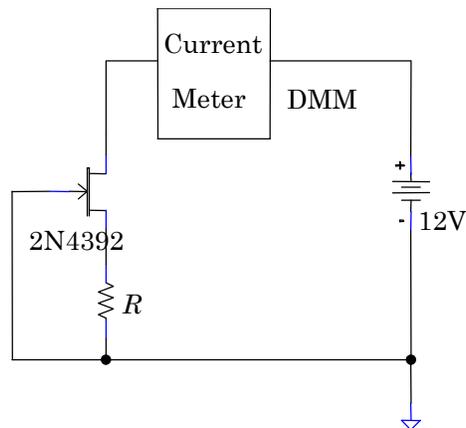
4.7 Find the complete output characteristic for your JFET with the JFET Output Tracer. Take scans in both the linear and saturated regimes.

(E) Self-Biased Current Sources

4.8  Rebuild the circuit used in 5.5. Measure the output current as a function of the Offset Adder potential. Graph your new data on the graph for 5.6. Does this circuit make a stiffer current source? Calculate the approximate stiffness of the source at a source potential drop of +10V. (The stiffness is essentially the output impedance at the quiescent point, the DC operating point). Spray the JFET with circuit cooler. Does the output current change less than in 5.6?

4.9 **Substitute** a 10k resistor for the 390Ω resistor in your circuit. What is the new current? Quickly scan the Offset Adder potential. Does the circuit still behave like a current source? (You need not record anything.)

4.10 Replace the Offset Adder with the +12V supply.



Measure and record the output current for resistor values R_s of 100Ω, 390Ω, 2.2k and 10k. Do the measured values agree with the values predicted by a load line analysis based on the data from 5.3?

As you saw in 5.6 and 5.8, the externally biased JFET current is approximately constant in the saturation regime. Why not use that circuit instead of the self-biased source?

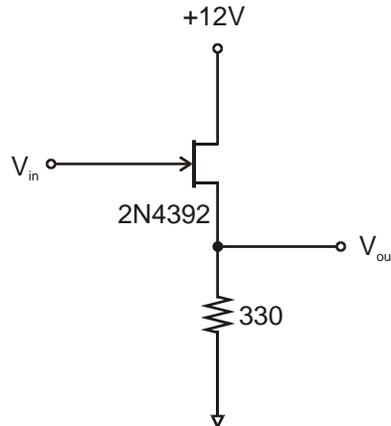
1. *The self-biased source is stiffer.* For fixed V_{GS} , the JFET current in 5.7 and 5.8 increases weakly with V_{DS} . Hence the source is not perfectly stiff. But in the self-biased circuit, ΔV_{DS} induced increases in the current will increase the voltage drop in the resistor, making the gate more negative with regard to the source, thus diminishing the current increase. While not perfect, the self-biased source will be much stiffer.
2. *The self-biased source is much less temperature dependent.* JFETs, like diodes, are strongly temperature dependent, but feedback acts to stabilize the current through the same mechanism described in the previous paragraph.
3. *The self-biased source has no external biasing network.* The self-biased circuit is simpler than the external bias circuit because it requires one fewer resistor.¹¹ More importantly, the self-biased supply does not need a negative bias power supply, and is thus completely independent of varia-

¹¹ Counting the potentiometer as two resistors in a voltage divider configuration.

tions in such bias supply voltages. Consequently, the circuit can be powered by a wide range of supply voltages. Most Op Amps, for example, rely heavily on self-biased current sources, and will run on power supplies ranging from $\pm 5\text{V}$ to $\pm 18\text{V}$.

(F) Source Followers

4.11  Build the simple follower below.



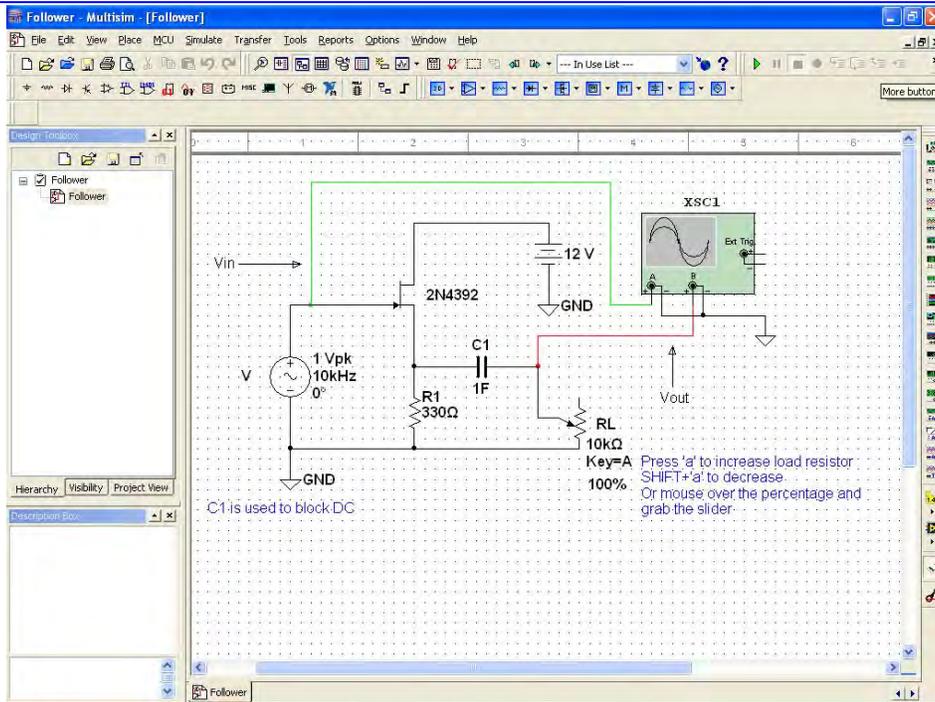
Drive the circuit with the waveform generator and Offset Adder. Play with different values of the offset, waveform amplitude, and waveform frequency, and compare V_{out} to V_{in} . Notice that the output amplitude is slightly smaller than the input amplitude. Explain the offset of V_{out} from V_{in} .

4.12 Remove the Offset Adder and drive the circuit by the signal generator directly. Carefully measure the gain $G = v_{out}/v_{in}$ of the follower. Because the two signals are almost the same size, the gain can be determined most accurately by measuring the difference $\Delta v = v_{out} - v_{in}$ directly on the scope and calculating the gain from $G = 1 + \Delta v/v_{in}$ (See Appendix I.)

With the input signal set to zero, measure the gate source voltage, and determine the source resistance from the data of 5.3. Does the gain agree with the predicted gain from Eq. (1)?



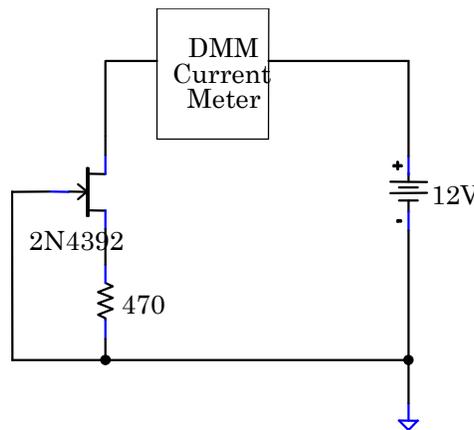
4.13 Study the effect of a load resistor with the MultiSim schematic Follower.ms11 Below:



Double click on the oscilloscope and run the simulation (by clicking on run button or going to simulation and pressing run) vary the load resistor by dragging the slide near the potentiometer or by pressing “a” and “Shift+a”. (make sure the schematic is responsive to keys by clicking on it before trying the hot keys. How does the output change? Approximately what is the output impedance of the follower? Determine the transconductance-source resistance r_s from your data and Eq. (2). Why is it necessary to use a blocking capacitor?

JFET transistors of the same type vary considerably due to manufacturing variations. JFET data sheets only list average characteristics. For example, the saturation drain current I_{DSS} is the current between the drain and the source when the gate source voltage is zero. For the 2N4392, this current is specified to be between 25 and 75mA, no average value is even given.

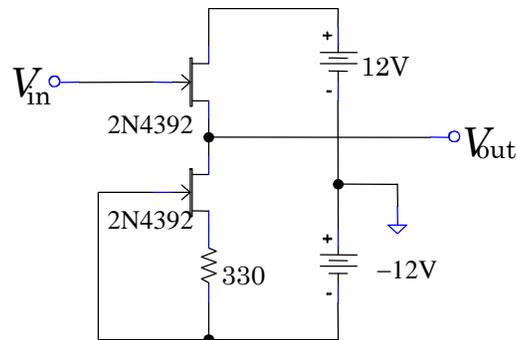
4.14 Measuring I_{DSS} is difficult because of the large power dissipated in the FET when $V_{GS} = 0$. Instead of measuring I_{DSS} , measure the current through your JFET at a lower current with the circuit below.



Obtain at least five additional 2N4392 JFETs and measure the current through each. Keep the JFET whose I_D is as close as possible to the I_D of your calibrated JFET, about within 10%, and return the rest. A set of nearly equal transistors is called a matched pair.¹² **Keep your matched pair for next week's lab.**

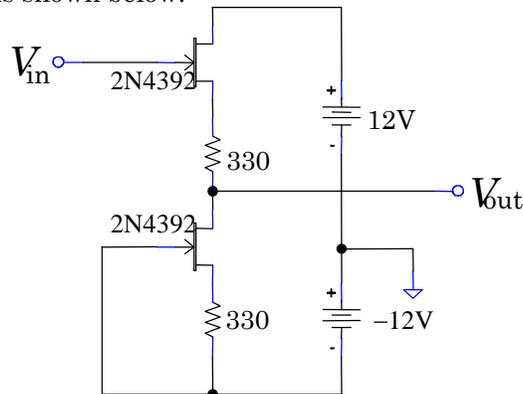
The gain of the simple follower studied in 5.11-5.13 is less than unity. According to Eq. (1), the gain can be improved by simply increasing the source resistor R_S . Unfortunately this technique also decreases the transconductance, thereby increasing the output impedance. But by replacing the source resistor with a current source, we can increase the effective source resistance without changing the transconductance.

4.15 Using your matched pair, construct the current-source driven follower diagrammed below.



Compare the input and output for a variety of input signals. Is there any discernible difference between the input and output amplitudes? What about DC offsets? DC offsets come from the difference between the JFETs. Using the stiffness of the current source calculated in 5.8, calculate the gain; does it agree with your observations?

4.16 The output of 5.15's follower is offset from the input. Show that the offset will largely disappear if you insert a resistor as shown below.



Explain why.

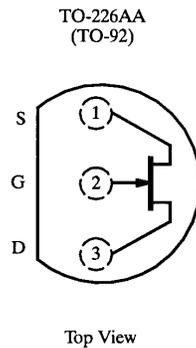
¹² Hand selection of matched pairs is not practical for commercial equipment. Fortunately it is rarely necessary because JFETs constructed on the same piece of silicon, such as in an integrated circuit, are very well matched. For the rare occasions when a discrete matched pair is required, very simple integrated circuits containing only a JFET pair are available.

Analysis

4.17 JFET followers stay linear over a wide range of input voltages V_{in} , yet the gain depends on g_m , which in turn depends on V_{GS} . Explain how feedback keeps the amplifier linear.

Supplementary Problems


4.18 Use the Curve Tracer to find the transfer characteristics of a 2N3819 JFET. The 2N3819 is more typical than the 2N4392; is its transfer characteristic closer to a parabola? Note that the 2N3819 uses the pin out shown at left. Specifications for the 2N3819 JFET are available at the course website.



4.19 Using the JFET Transfer Tracer compare some of the JFETs. (Use the **Keep Previous Data** button to overlay the curves for each device.)

Physics 111 ~ BSC**Student Evaluation of Lab Write-Up**

Now that you have completed this lab, we would appreciate your comments. Please take a few moments to answer the questions below, and feel free to add any other comments. Since you have just finished the lab it is *your* critique that will be the most helpful. Your thoughts and suggestions will help to change the lab and improve the experiments.

Please be specific, use references, include corrections when possible, using both sides of the paper as needed, and *turn this in with your lab report*. Thank you!

Lab Number: _____ Lab Title: _____ Date: _____

Which text(s) did you use?

How was the write-up for this lab? How could it be improved?

How easily did you get started with the lab? What sources of information were most/least helpful in getting started? Did the pre-lab questions help? Did you need to go outside the course materials for assistance? What additional materials could you have used?

What did you like and/or dislike about this lab?

What advice would you give to a friend just starting this lab?

The course materials are available over the Internet. Do you (a) have access to them and (b) prefer to use them this way? What additional materials would you like to see on the web?

Appendix I: Comparing Two Nearly Equal Signals

Comparing the amplitude of two nearly equal scope traces is difficult because of calibration errors in the scope. Since scope probes introduce additional amplitude and phase errors, do not use them with low impedance sources like follower outputs.

The calibration errors can be removed by calibrating the scope channels against each other. Feed the same signal into both channels and set both channels' gain to the same value. Then turn the CAL vernier in the center of the CH1 volts/div knob until the signal overlap. If you cannot get the two traces to overlap with the CH1 vernier, return the CH1 vernier to its pre-calibrated position,¹³ and adjust the CH2 vernier knob. If you change the volts/div scale, you will need to recalibrate.

The blurriness of the traces may still prevent you from making an accurate comparison of the two signals. A better measurement can be made by subtracting the signals. Temporarily attach both channels to one of the signals that you wish to compare. Set the channel couplings to AC, and set both volts/div knobs so that the traces are as large as possible without running off the scope screen. Check to make sure that both channels look correct, and then change Ch2 to INVert, and set the mode to ADD. On these settings the scope subtracts the two channels. Ideally you should see a flat line, but small differences in the channel gains will probably cause the scope to show a small amplitude signal. This error signal can be eliminated by calibrating the scope channels; turn the CAL verniers as described above. Perfect cancellation of the two signals may not be possible. Then take one of the channels and attach it to your other signal. The trace that you see on the screen will be the difference between your two signals.

You can increase the sensitivity of the scope by turning both volts/div knobs one position. Any more will cause the scope amplifiers to saturate. If you change the volts/div knobs, you will have to recalibrate the scope.

Note that this subtraction technique only works if the signals that are being compared are in phase; any significant phase shift between the input and output will yield a false reading.

Remember to return all the calibration knobs to their pre-calibrated positions when you are finished. Leaving them in the uncalibrated positions is an excellent way to confuse both yourself and subsequent scope users.

¹³ To return the vernier to its pre-calibrated position, turn it until it clicks into place.

Appendix II: 2N4392 Specifications

Siliconix

2N/PN/SST4391 Series

N-Channel JFETs

2N4391	PN4391	SST4391
2N4392	PN4392	SST4392
2N4393	PN4393	SST4393

Product Summary

Part Number	V _{GS(off)} (V)	r _{DS(on)} Max (Ω)	I _{D(off)} Typ (pA)	t _{ON} Typ (ns)
2N/PN/SST4391	-4 to -10	30	5	4
2N/PN/SST4392	-2 to -5	60	5	4
2N/PN/SST4393	-0.5 to -3	100	5	4

2N4391, For applications information see AN104, page 21.
 PN/SST4393, For applications information see AN106, page 28.

Features

- Low On-Resistance: 4391 < 30 Ω
- Fast Switching—t_{ON}: 4 ns
- High Off-Isolation: I_{D(off)} with Low Leakage
- Low Capacitance: < 3.5 pF
- Low Insertion Loss

Benefits

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response, Low Glitches
- Eliminates Additional Buffering

Applications

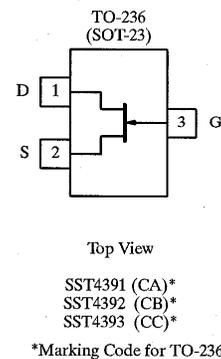
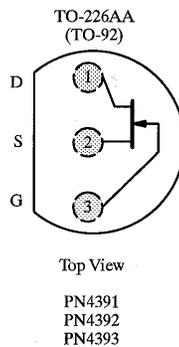
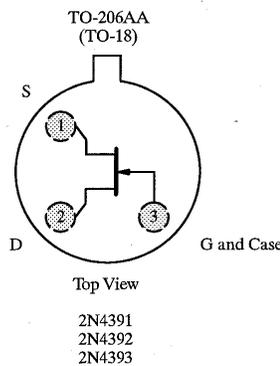
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters
- Commutators

Description

The 2N/PN/SST4391 series features many of the superior characteristics of JFETs which make it a good choice for demanding analog switching applications and for specialized amplifier circuits.

can be available with processing per MIL-S-19500 (see Military Information). Both the PN, TO-226AA (TO-92), and SST, TO-236 (SOT-23), series are available in tape-and-reel for automated assembly (see Packaging Information). For similar dual products, see the 2N5564/5565/5566 data sheet.

The 2N series hermetically-sealed TO-206AA (TO-18)



2N/PN/SST4391 Series

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Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage: (2N/PN Prefixes) -40 V (SST Prefix) -35 V	Operating Junction Temperature: (2N Prefix) -55 to 200 °C (PN/SST Prefixes) -55 to 150 °C
Gate Current 50 mA	Power Dissipation: (2N Prefix) ^a (T _C = 25 °C) 1800 mW (PN/SST Prefixes) ^b 350 mW
Lead Temperature 300 °C	
Storage Temperature: (2N Prefix) -65 to 200 °C (PN/SST Prefixes) -55 to 150 °C	Notes a. Derate 10 mW/°C above 25 °C b. Derate 2.8 mW/°C above 25 °C

Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit	
				4391		4392		4393			
				Min	Max	Min	Max	Min	Max		
Static											
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA V _{DS} = 0 V	2N/PN	-55	-40		-40		-40		V
			SST	-55	-35		-35		-35		
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 20 V	2N/PN: I _D = 1 nA		-4	-10	-2	-5	-0.5	-3	mV
		V _{DS} = 15 V	SST: I _D = 10 nA								
Saturation Drain Current ^c	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	2N		50	150	25	75	5	30	mA
			PN		50	150	25	100	5	60	
			SST		50		25		5		
Gate Reverse Current	I _{GSS}	V _{GS} = -20 V, V _{DS} = 0 V	2N/SST	-5		-100		-100		-100	pA
			PN	-5		-1000		-1000		-1000	
			2N: T _A = 150 °C	-13		-200		-200		-200	nA
			PN: T _A = 100 °C	-1		-200		-200		-200	
SST: T _A = 125 °C	-3										
Gate Operating Current	I _G	V _{DG} = 15 V, I _D = 10 mA		-5						pA	
Drain Cutoff Current	I _{D(off)}	V _{DS} = 20 V	2N: V _{GS} = -5 V	5						100	pA
			2N: V _{GS} = -7 V	5				100			
			2N: V _{GS} = -12 V	5		100					
			PN: V _{GS} = -5 V	0.005						1	nA
			PN: V _{GS} = -7 V	0.005				1			
			PN: V _{GS} = -12 V	0.005		1					
		SST V _{DS} = 10 V, V _{GS} = -10 V	5		100		100		100	pA	
		V _{DS} = 20 V T _A = 150 °C	2N: V _{GS} = -5 V	13						200	nA
			2N: V _{GS} = -7 V	13				200			
			2N: V _{GS} = -12 V	13		200					
V _{DS} = 20 V T _A = 100 °C	PN: V _{GS} = -5 V	1						200	nA		
	PN: V _{GS} = -7 V	1				200					
	PN: V _{GS} = -12 V	1		200							
V _{DS} = 10 V T _A = 125 °C	SST: V _{GS} = -10 V	3									
Drain-Source On-Voltage	V _{DS(on)}	V _{GS} = 0 V	I _D = 3 mA	0.25						0.4	V
			I _D = 6 mA	0.3			0.4				
			I _D = 12 mA	0.35		0.4					

Siliconix

2N/PN/SST4391 Series

Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit	
				4391		4392		4393			
				Min	Max	Min	Max	Min	Max		
Static (Cont'd)											
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$			30		60		100	Ω	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1\text{ mA}$ $V_{DS} = 0\text{ V}$	2N	0.7		1		1		1	V
			PN/SST	0.7							
Dynamic											
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20\text{ V}, I_D = 1\text{ mA}, f = 1\text{ kHz}$		6						mS	
Common-Source Output Conductance	g_{os}			2.5							μS
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0\text{ V}, I_D = 0\text{ mA}, f = 1\text{ kHz}$			30		60		100	Ω	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	2N	12		14		14		14	pF
			PN	12		16		16		16	
			SST	13							
Common-Source Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 0\text{ V}$ $f = 1\text{ MHz}$	2N: $V_{GS} = -5\text{ V}$	3.3						3.5	
			2N: $V_{GS} = -7\text{ V}$	3.2				3.5			
			2N: $V_{GS} = -12\text{ V}$	2.8		3.5					
			PN: $V_{GS} = -5\text{ V}$	3.5						5	
			PN: $V_{GS} = -7\text{ V}$	3.4				5			
			PN: $V_{GS} = -12\text{ V}$	3.0		5					
			SST: $V_{GS} = -5\text{ V}$	3.6							
			SST: $V_{GS} = -7\text{ V}$	3.5							
			SST: $V_{GS} = -12\text{ V}$	3.1							
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 10\text{ V}, I_D = 10\text{ mA}$ $f = 1\text{ kHz}$		3						nV/ $\sqrt{\text{Hz}}$	
Switching											
Turn-On Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}$ $V_{GS(H)} = 0\text{ V}$ See Switching Circuit	2N/PN	2		15		15		15	ns
			SST	2							
	t_r		2N/PN	2		5		5		5	
			SST	2							
Turn-Off Time	$t_{d(off)}$		2N/PN	6		20		35		50	
			SST	6							
	t_f	2N/PN	13		15		20		30		
		SST	13								

Notes

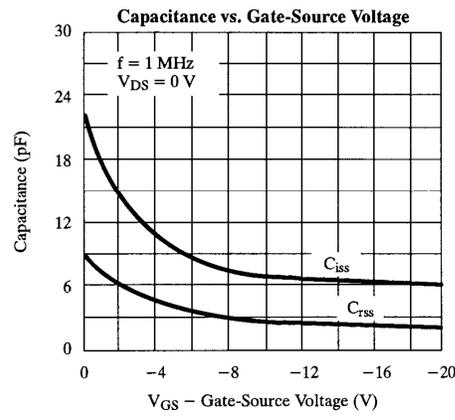
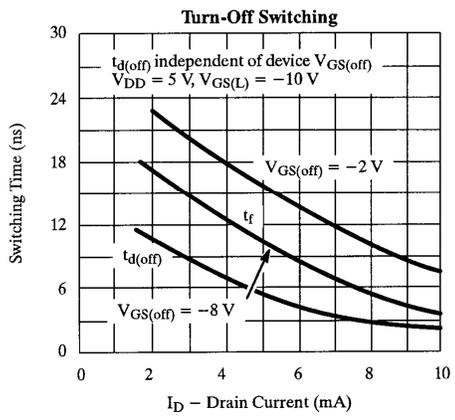
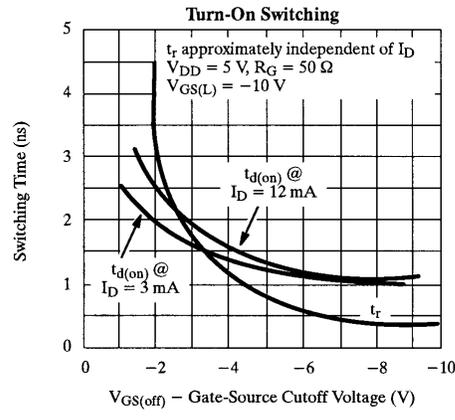
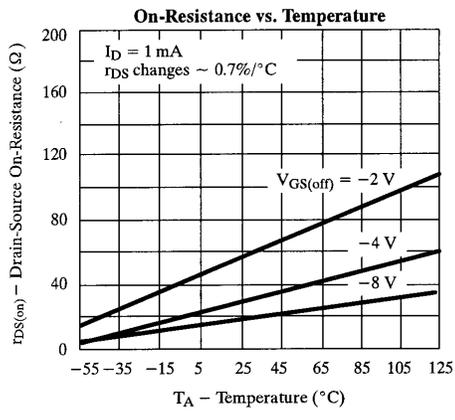
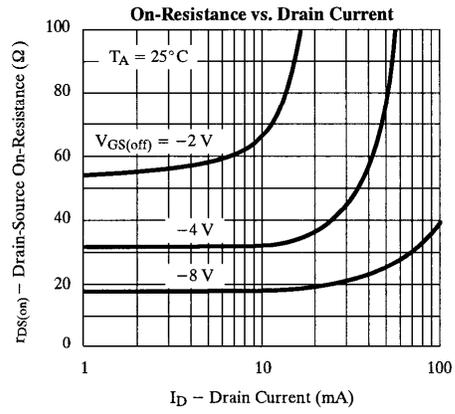
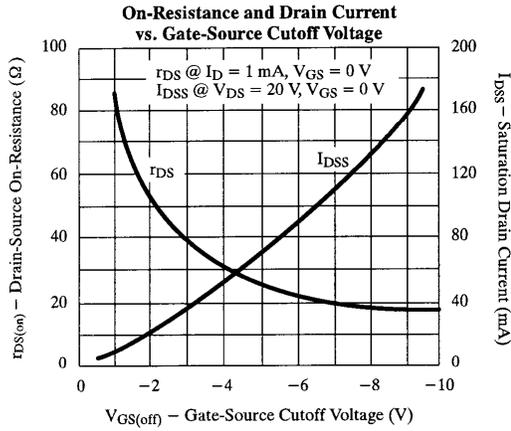
- a. $T_A = 25^\circ\text{C}$ unless otherwise noted.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 3\%$.

NCB

2N/PN/SST4391 Series

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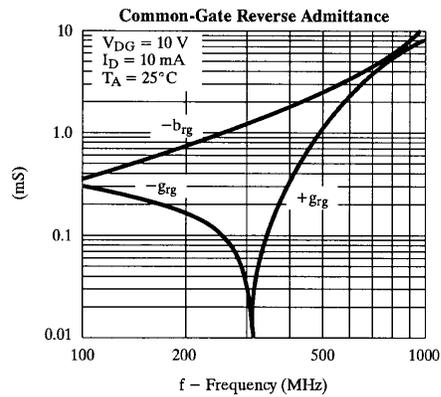
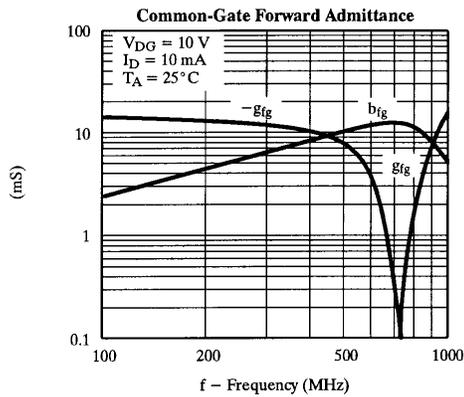
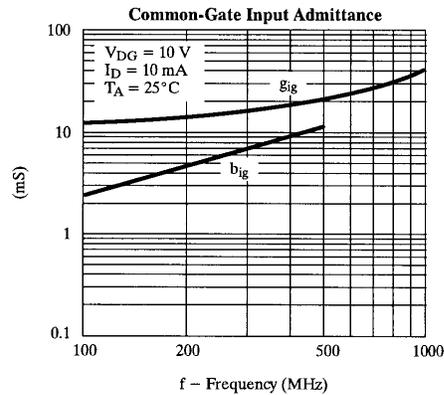
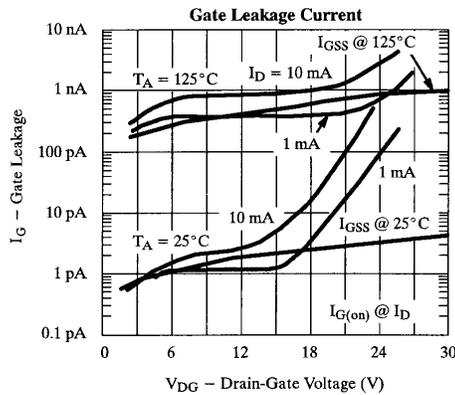
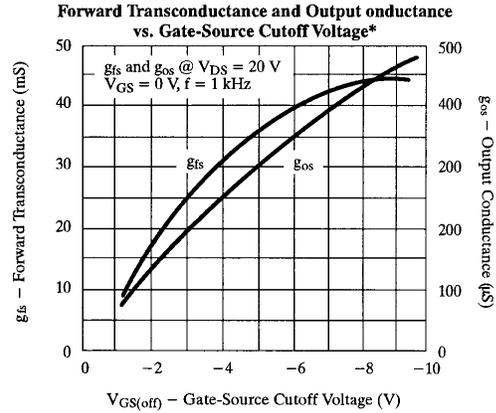
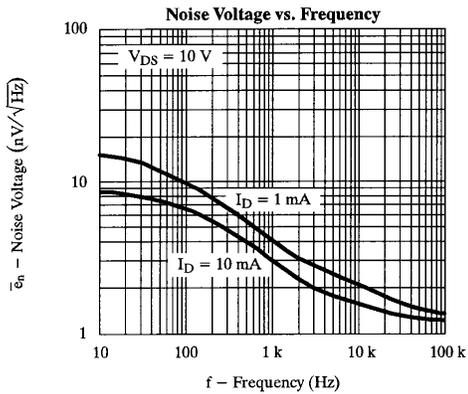
Typical Characteristics



2N/PN/SST4391 Series

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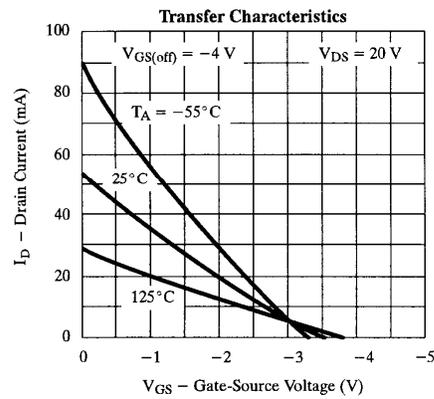
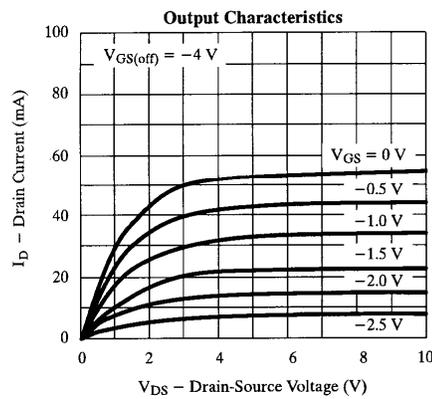
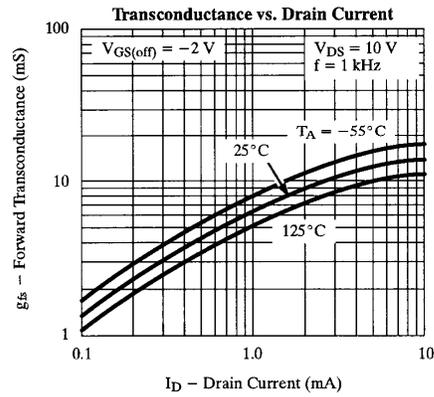
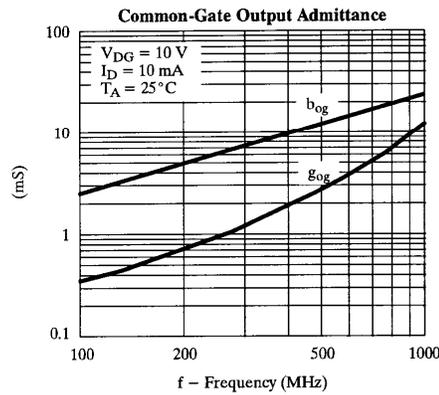
Typical Characteristics (Cont'd)



2N/PN/SST4391 Series

Siliconix

Typical Characteristics (Cont'd)



Switching Time Test Circuit

	4391	4392	4393
$V_{GS(L)}$	-12 V	-7 V	-5 V
R_L^*	800 Ω	1600 Ω	3000 Ω
$I_{D(on)}$	12 mA	6 mA	3 mA

*Non-inductive

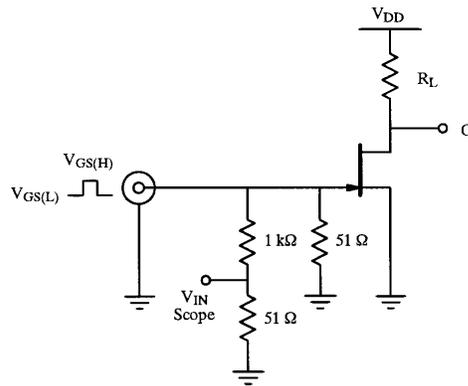
Input Pulse

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

Sampling Scope

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF

See Typical Characteristics curves for changes.

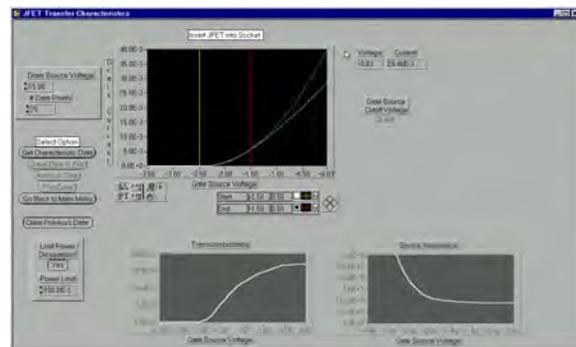


Appendix III: JFET Curve Tracer

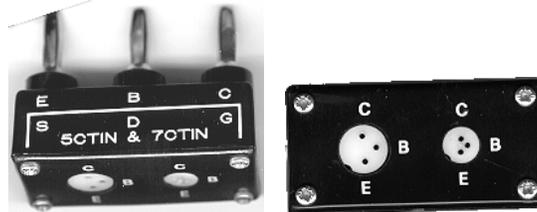
Refer to Curve Tracer information in Lab 4 for basic curve tracer operation.

JFET Transfer Tracer

The JFET Transfer Tracer determines a JFET's transfer characteristic by locating the Gate Source Pinch-off Voltage V_P , and scanning the gate voltage from V_{GS} to ground, while keeping the drain source voltage fixed at the value set by the **Drain Source Voltage** control. The **Analyze Data** option will find the best-fit parabola to the data and will also determine the transconductance and the source resistance. The power limiting options allow the average power to be limited to the specified values. The remaining controls are similar to those used by the Diode Tracer.

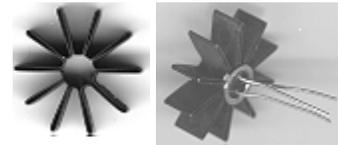


Most JFET leads are too short to be directly connected to the Tracer banana inputs. The transistor input block provides a convenient way to insert the JFETs. The bottom of the block has three banana plugs, which plug into the Tracer, and the top has two different size sockets.



Use either socket, inserting the JFET source into the E (emitter) input, the gate into the B (base) input, and the drain into the C (collector) input.

The JFETs may dissipate a significant amount of power on certain scans, and heat up enough to change the characteristic curves. Use a heat sink to limit the JFETs' temperature rise. The fins on the heat sink increase the surface area in contact with the air, increasing the thermal conductivity between the JFET and the air, thereby increasing the cooling. Mount the heat sink onto the JFET by pushing the case of the JFET into the hole in the center of the heat sink.



JFET Output Tracer

The JFET Output Tracer scans the drain voltage, while measuring the drain current, for a series of fixed gate voltages. The lowest gate voltage equals V_{GS} plus the **Gate Start Offset**. The Tracer can be configured for linear and saturated scans with the preset buttons. The remaining controls are similar to the JFET Transfer Tracer controls, but there is no analysis function.

