Simple 3-Point FET Matching for F5X

EUVL
10 March 2012

Motivation

I have been asked about a simple procedure for matching JFETs and Mosfets for the F5X power amplifier that does not required complicated equipment other than digital multimeters and laboratory power supplies. I am glad to oblige.

As already described in my earlier posts in various F5 threads, or on the xen-audio website, the cancellation of even harmonics in a balanced circuit relies on the left and right halves of the circuit behaving in an identical manner. This requires the active devices to be as identical to each other as possible over the operating range. As described on the xen-audio website, single-point matching method does not always result in proper matching over the entire operating range. This can only be achieved by testing the devices under actual working conditions, e.g. by curve tracing with actual circuit voltage and bias current.

Many of you do not own a curve tracer with sufficient accuracy and thermal stability, or do not want to go into such trouble. So the method described here is a compromise between curve tracing and one point measurement. At the very least, it allows you to match the devices at three points which will cover the actual operating range in circuit. Note that the procedure described here in detail applies to the F5X circuit conditions only. You will to adapt certain values to suit the application in other circuits. The basic principle is, however, universal.

Equipment Required for Matching

The basic equipment required are laboratory power supply (min. 16V 3A, preferably with adjustable current limit), and two 3½ digit or better digital multimeters, ideally powered by low-noise voltage regulators.
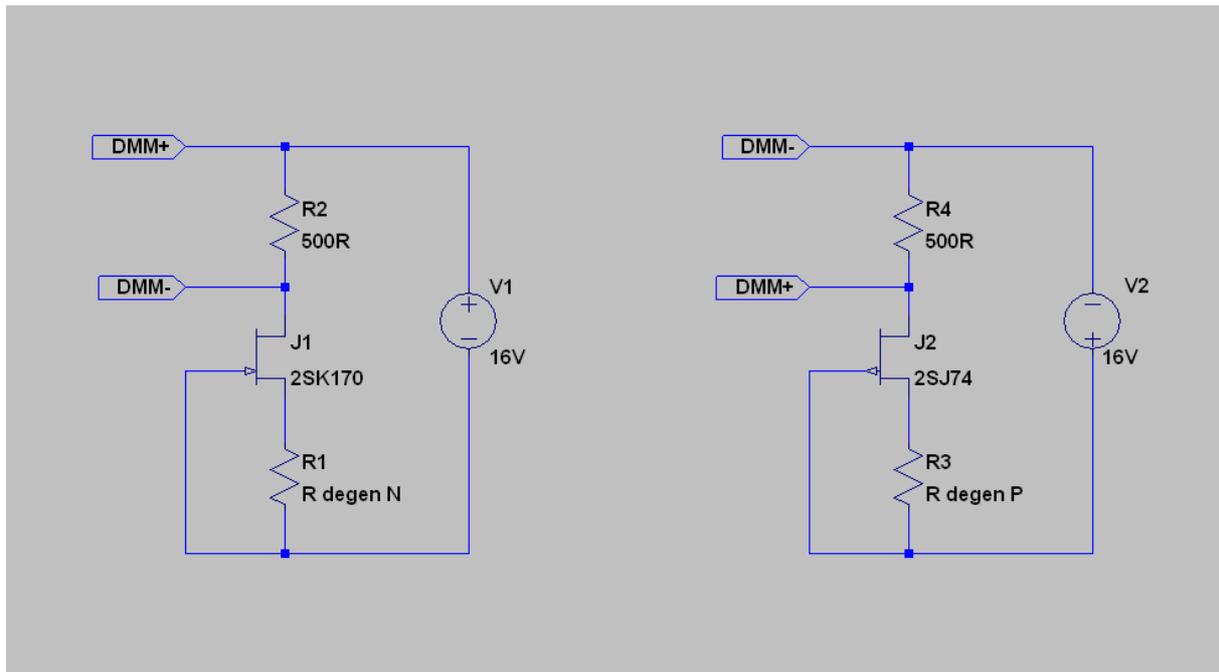
JFET Matching

In earlier post at the DIY Audio forum, I described a 3-point measurement method for JFETs using different degeneration resistors. I shall repeat that here, but with a bit more detail.

The input JFETs of the F5X do not operate at Idss, as they are degenerated by the shunt resistor of the feedback network. Thus to measure the actual bias current, the JFET should also be degenerated. On top of that, I have described the need for an additional 5R source resistor for the 2SJ74 in order to reduce its transconductance to that of the 2SK170. Thus, the JFETs should be tested with the following circuits, which are identical to the input stage of the F5X.

For 2SK170, the 3 resistor values used for degeneration should be 0R, 11R and 22R. For 2SJ74, they should be 5R, 16R and 27R instead. As you measure the voltage drop across the 500R resistor for each degeneration resistor, record the value for each in an excel sheet. Once all JFETs are characterized, put them in an excel sheet and sort them by the current of the middle measurement (i.e. 11R for N-JFET and 16R for P-JFET). This is the actual bias current later in the F5X. Then also compare all three reading of each JFET and pair them accordingly. This not only applies to P-P or N-N match, but also P-N match. Since the current for all devices are measured with the same 500R low-tempco resistor, the actual value of the resistor is less important than its thermal stability. If you have lots of JFETs to match, then it might be worth using a rotary switch to switch between degeneration resistors. If you only intend to build 2 channels, then I would just use normal 0.1" DIL socket.

JFETs are thermally sensitive devices, so at least you want to give it a few minutes to reach steady state before taking the ready. Also environmental conditions are important, so measure them within half an hour under constant ambient temperature, and shield the entire measurement circuit from air movement by putting it inside a suitable transparent container (e.g. a bell jar cloche).
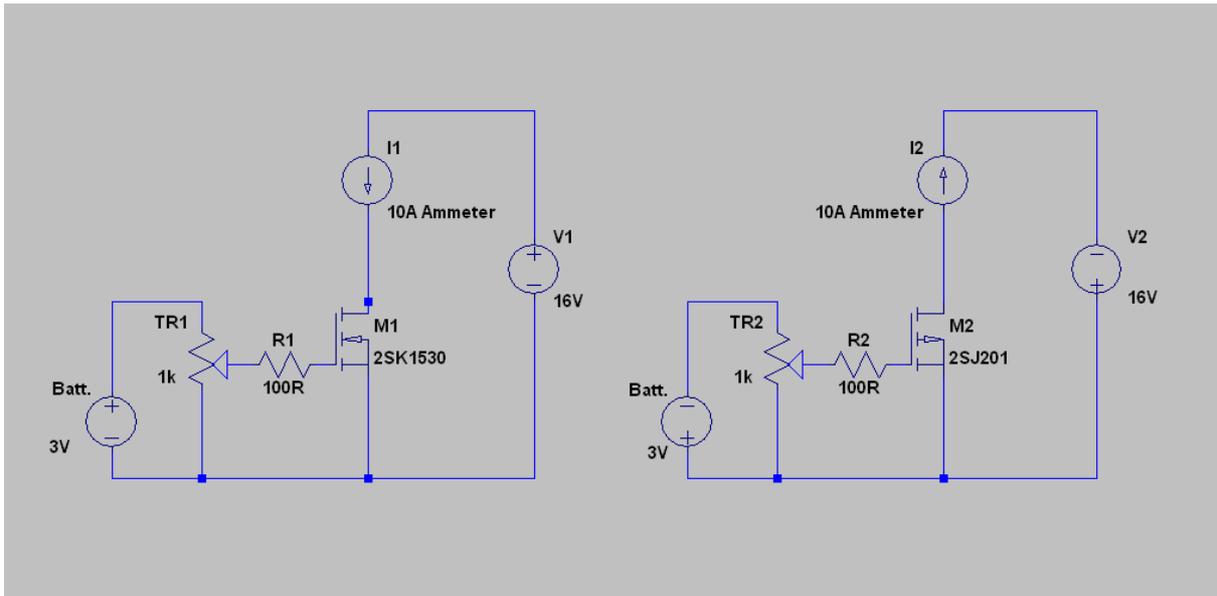
JFET Match Schematics

Mosfet Matching

Matching Mosfets under operating conditions is a bit more involved, as they run at high temperature in Class A circuits. Ideally one can mount them all the original heat sink in the actual position, bias them at the right voltage (16V Vds) and current (2A Id), wait for the whole thing to reach steady state while checking and trimming the current constantly, before taking the final value. But this will take quite a bit of time.

A more practical method that I use is to mount the Mosfets (4Ns or 4Ps for 2 channels) next to each other on a large aluminium block (say 5kg) with a flat, machined mounting surface. Kerafol or a good thermal grease should be used as an interface to ensure proper thermal contact. Electrical isolation between Mosfet and aluminium block is not important as long as you make sure the drain is the only electrical connection that will come into contact with the block. Put the whole thing in an oven and allow it to warm up and stabilise to heat sink temperature (e.g. 60°C). Allow enough time for this. You can use long, heat-resistant wires and a 3-way terminal block to connect one Mosfet at a time to the test circuit, keeping the block and the Mosfets inside the oven while measurement takes place. It sounds complicated, but it isn't really. Just time consuming.

Now you can apply 16V to the Mosfet drain to source (with the respective correct polarity for N- and P-Mosfets), and use a separate 3V battery and a 1k trimmer to apply a variable Vgs. The drain current should be measured using the 10A measurement range of one DMM, while the other DMM is used to measure Vgs applied. An additional thermocouple clamped to the block would also be very useful in monitoring temperature.

Start off with Vgs =1.5V (positive polarity for N-Mosfets, negative for P-Mosfets), and slowly increase this until Id reaches 2A. Give it a few minutes to settle and readjust Vgs if necessary. Once at steady state, you can now record the Vgs value at the DMM. Reduce Vgs to lower Id to 1.5A, and record Vgs again. Finally, increase Vgs to raise Id to 2.5A, and again record Vgs. Repeat this for all Mosfets of the same type.

Mosfet Match Schematics

Tabulate all the measured values in an Excel sheet, and sort them by Vgs at 2A. Compare all Vgs values and pair the FETs accordingly. In a balanced F5 circuit, the N-N and P-P match is more important than N-P match. The latter is important only for even harmonic cancellation between the top and bottom halves in a single ended F5. This cancellation is, however, being taken care of by the left and right halves, so that less-than-perfect cancellation between top and bottom halves can still be tolerated.

Patrick