

# JFETS: THE NEW FRONTIERS, PART 2

*This noted design expert from Germany continues his series by showing how you can best take advantage of JFET performance.*

In Part 1 of this article, I discussed the single-stage (or single-ended) amplifier operating in common-source mode. As these stages are usually limited in audio to AC signals, the inherent DC drift is of relatively little importance. You can even use them for DC signals if you select the working point carefully at zero temperature coefficient. However, if you remember the formula for zero tempco ( $V_{GS} = V_p + 0.63V$ ), you realize that the condition is different from unit to unit, since  $V_p$  is different.

A better solution is to use a differential amplifier, where the drifts of two matched JFETs tend to cancel each other. The configuration is shown in Fig. 12a. If  $R_0$  is large enough, then:

$$I_{D1} + I_{D2} = I_0$$

Further, if  $I_{D1}$  changes  $\Delta I_{D1}$ , then  $I_{D2}$  also changes by the same amount, but in the opposite direction, i.e.,

$$\Delta I_{D1} = -\Delta I_{D2}$$

The differential gain of the stage is:

$$A_{V(DD)} = \frac{(V_{D1} - V_{D2}) / (V_{GS1} - V_{GS2})}{= R_D \times g_m}$$

which is the same as the gain of a single common-source stage. For  $R_0$  to be very large,  $-V_S$  must also be very large. This is usually inconvenient, so instead of a resistor, you use a so-called constant-current source, which delivers  $I_0$  independent of  $-V_S$  (Fig. 12b).

Due to its symmetrical nature, you can also consider the differential amplifier as two symmetrically arranged "half-circuits," each with a JFET, a load resistor, and half of a current source, providing  $I_0/2$ .<sup>1</sup> This is shown in Fig. 13. If the two JFETs are "identical," then you can join the two half-circuits together at the sources without upsetting the DC operation. However, you now have balanced single-ended amplifiers.<sup>2</sup>

Seen from gate 1, JFET 1 operates as a common-source amplifier, except that the source is connected to the source of

JFET 2, operating it with source input. Seen from gate 2, the same thing happens—JFET 2 is in common-source mode, driving JFET 1 in the source. There are a number of advantages to operating two JFETs in this way, and I will start here with the common-mode rejection.

### Common-Mode Signals

A very important feature of the differential amplifier is its ability to reject common-mode signals. Common mode means that both gates are driven with the same polarity and equal amplitude signals. It is easy to see that if only gate 1 is driven positive, then  $I_{D1}$  increases and  $I_{D2}$  decreases. But if both gates are driven positive, then both  $I_{D1}$  and  $I_{D2}$  must increase, which is impossible because  $I_{D1} + I_{D2} = I_0$ ; i.e.,  $I_0$  is constant. Consequently, the differential amplifier cannot amplify same-polarity or common-mode signals.

Just how good it is in rejecting common-mode signals is expressed with the common-mode gain:

$$A_{V(CM)} = -R_D / 2r_o$$

where  $r_o$  is the output impedance of the constant-current source. In order to have low common-mode gain (i.e., good rejection), the output impedance of the current source must be very large.

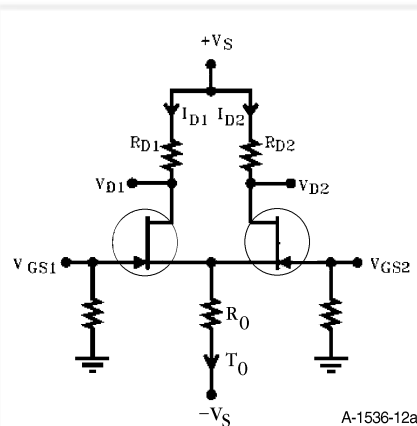


FIGURE 12A: Basic differential amplifier with JFETs.

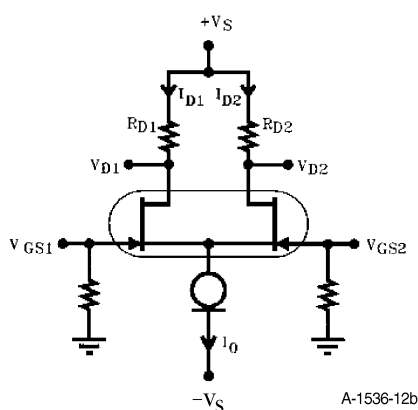


FIGURE 12B: Improved differential amplifier with constant-current source.

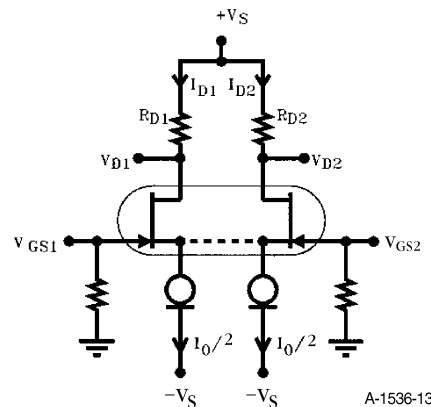


FIGURE 13: The differential amplifier represented with two symmetrically arranged "half-circuits."

The importance of low common-mode gain is closely related to the temperature drift, because changes in  $I_D$ ,  $V_{GS}$ , and  $g_m$  can be considered common-mode signals if they are the same for both JFETs. Normally, a common-mode rejection ratio (CMRR) is specified for the differential amplifier. It is the ratio between the differential gain and the common-mode gain:

$$CMRR = A_v(DD)/A_v(CM) \approx 2g_m \times r_o.$$

Obviously the two JFETs must be closely matched to achieve good common-mode rejection. In fact, these two formulas are valid only if the two JFETs are perfectly matched. Although it is possible to select well-matched JFETs, the easier way is to use dual JFETs matched by the manufacturer, or even better, dual JFETs manufactured on the same silicon chip, i.e., monolithic duals.

I have been using the NPD 5566 dual N-channel and the AH 5020CJ dual P-channel JFETs.<sup>3</sup> However, these are not truly complementary types, as I pointed out in my article.<sup>3</sup> The first complementary types on the market were the 2SK240/2SJ74 medium  $g_m$  and the 2SK146/2SJ73 high  $g_m$ /low-noise types. These are closely matched single devices, mounted in a common aluminum case for good thermal tracking. Unfortunately, these devices are no longer in production.

### Dual Monolithic JFETs

Although there are plenty of N-channel dual JFETs on the market, complementary dual monolithic JFETs are rare. In fact, I know of only one family, the 2SK389/2SJ109, made by Toshiba. These are still manufactured and available, so I use them in all my amps with differential input. Now I'll describe some practical differential circuits.

Figure 14a shows a simple differential amplifier with the 2SK389 dual monolithic JFET from  $I_{DSS}$  group V. I hooked it up with  $\pm 36V$  to operate the JFETs under conditions similar to those of the SE ones. The constant-current source is a J511 JFET delivering 4.7mA. In order to run the drains at roughly one-half the supply voltage (about 18V), I chose  $R_{D1} = R_{D2} = 10k$ .

First I tested the amplifier in single-ended mode, i.e., gate 2 connected to ground, with the measurements taken at  $V_{D2}$ . ( $V_{D2}$  has the same phase as  $V_{GS1}$ .) Although from the operational point of view it is single-ended, I think this mode is more appropriately called the unbal-

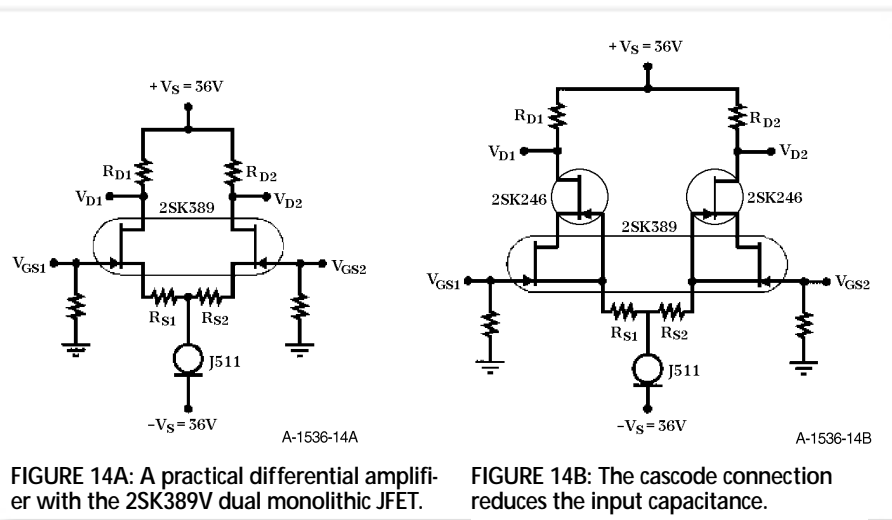


FIGURE 14A: A practical differential amplifier with the 2SK389V dual monolithic JFET.

FIGURE 14B: The cascode connection reduces the input capacitance.

anced mode. Gain without local feedback ( $R_{S1} = R_{S2} = 0$ ) is about 64 times, which is 36dB. Frequency response is 175kHz, and the input capacitance is 330pF. THD, measured at 1kHz, is shown in column 1 of Table 2.

Next I inserted source resistors  $R_{S1} = R_{S2} = 100R$ , and reran the measurements. Due to the local feedback, the gain dropped to approximately 28 times, and the input capacitance to 160pF. The THD also decreased by about 6dB.

In order to reduce the input capacitance further, I put 2SK246 cascodes in the circuit (Fig. 14b). The gain did not

anced signal from the two drains.

I have made some rudimentary THD measurements in balanced mode, shown in column 3 of Table 2. Unfortunately, my oscillator and THD analyzer (HP339A) are unbalanced, so I needed to improvise the balanced operation with op amps, limiting the measurements to the levels shown in the table (lower levels were masked by noise). Nevertheless, it clearly indicates that the circuit thrives in balanced mode, having 10–20dB less THD compared to unbalanced mode. It also indicates the advantages of this circuit relative to the SE cir-

TABLE 2

Output in VRMS	Column 1 SE mode, $R_{S1} = R_{S2} = 0$	Column 2 SE/cascode mode, $R_{S1} = R_{S2} = 100R$	Column 3 Balanced mode, $R_{S1} = R_{S2} = 100R$
0.3	0.013%	0.006% (noise)	
1	0.035%	0.012%	
3	0.27%	0.1%	0.023%
5	0.85%	0.33%	0.06%
8	2.6%	1%	0.12%
10	4.7%	2.3%	0.17%

change significantly, but the input capacitance dropped to 50pF! THD also decreased, as shown in column 2, Table 2.

### Balanced Mode

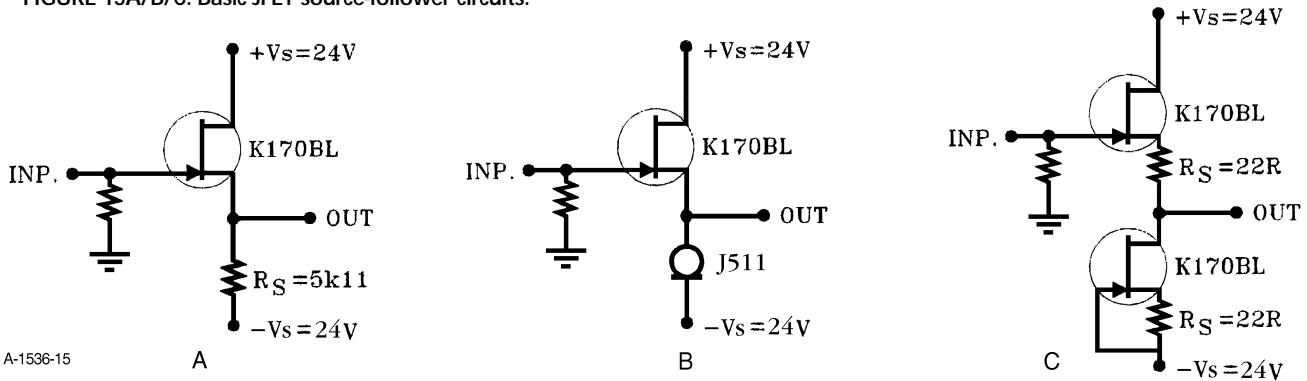
A couple of comments are in order concerning this circuit. According to the measurements, it is a very decent design, considering that it uses only a very small amount of local feedback. The gain is still fairly high, and you can reduce it further by increasing the source resistors, which in turn further reduces the THD. However, to fully take advantage of the symmetrical nature of this circuit, you should use it in balanced mode, which requires applying a balanced signal at the two gates and taking the bal-

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As mentioned in Part 1, the input capacitance is voltage-dependent, which can cause THD when the amplifier is driven from high source impedances. I have tested the circuit described in column 2 of Table 2 with 50k, 100k, and 500k sources. There was no measurable change in distortion up to 100k, but at

FIGURE 15A/B/C: Basic JFET source-follower circuits.



500k, I could see a slight increase.

Again, for noise reasons, you should probably keep the source impedance below 50k, so there is no problem with the capacitance modulation anyway. I also checked the CMRR by connecting the two gates together and driving them with a 3V RMS signal. The output, again in balanced mode, was down 87dB at 1kHz. The CMRR dropped to 70dB at 10kHz and 63.5dB at 20kHz, but even at 100kHz, it was 50dB!

**The Output**

I have now described two types of amplifier stages using JFETs, the common-source or single-ended stage, and the differential or balanced amplifier. You can use either of these to build audio amplifiers, depending on your preference for balanced or unbalanced operation. Personally, I prefer the differential circuit, because you can use it with balanced or unbalanced sources, and it can also feed balanced or unbalanced power amplifiers. Balanced operation gives a subjective impression of increased dynamics. It can also be an extremely useful interfacing consideration in breaking up ground loops.<sup>4</sup>

There are two issues to consider when talking about the SE and balanced amplifiers. First of all, the output does not sit at 0V DC, but at some 10–20V above ground. If you wish to connect it to, say, a DC-coupled power amplifier, you must block this DC voltage from reaching the power-amp input. This is easily done using a capacitor, and this problem is well known to all SE fans, whether of tube or semiconductor variety. I will therefore not spend much time on the subject.

A much more important question is whether these circuits can drive the input impedance of a power amplifier. The output impedance of the amps ex-

Output V RMS	Column 1 $R_S = 5.11k$	Column 2 $R_S = \text{constant-current source}$	Column 3 $R_S = \text{JFET current source}$	Column 4 The "Borbely" source follower
0.3V	0.0025	0.0023	0.002	0.0025
1V	0.0033	0.0024	0.0018	0.0035
3V	0.011	0.0025	0.0016	0.0045
5V	0.02	0.003	0.0016	0.0074

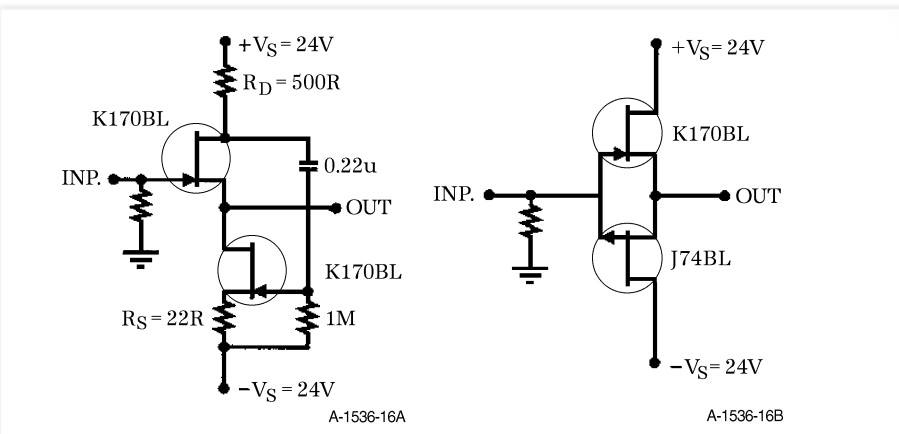


FIGURE 16A/B: These source-follower circuits can drive low-impedance loads with very low THD.

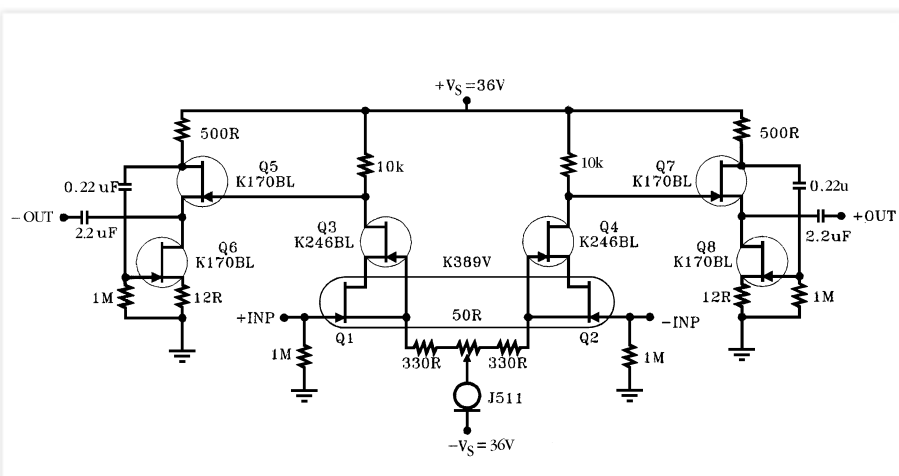


FIGURE 17: The all-JFET balanced SE line amp.

amined is basically equal to the drain resistor of the amplifier. If  $R_D = 10k$ , then the output impedance is also close to 10k. But if the input impedance of the power amp is also 10k, then you are certainly in trouble. First, you lose 6dB of gain by the voltage division between the 10k resistors; second, the 10k input will most likely load the output and cause a lot of THD. Even with 20k or 50k input impedance, you might run into problems. It is advisable to put an impedance transformer at the output to avoid this. Source followers to the rescue!

### JFETs as Followers

Just like tubes and bipolar transistors, JFETs can also be operated as followers, more specifically source followers. The basic circuit is shown in *Fig. 15a*. The drain is AC-grounded, and the output signal is taken out across the source resistor, which means it operates with 100% local feedback. The gain of the source follower is:

$$A_V = g_m \times R_S / (1 + g_m \times R_S)$$

Two things become obvious from the formula: first, the source follower does not reverse the phase of the signal, and second, if  $g_m \times R_S \gg 1$ , then the gain becomes approximately unity. In order to make  $R_S$  large, you can use a constant-current source with high output impedance (*Fig. 15b*). The linearity is also dependent on  $R_S$  (see the 1kHz THD measurements in columns 1 and 2 of *Table 3*).

The input capacitance is low because it is not augmented by the Miller effect. I measured approximately 5pF for the circuits in *Fig. 15a* and *b*. The output impedance equals approximately  $1/g_m$ . With high- $g_m$  devices, this will be fairly low. I measured 38Ω for the basic circuits in *Fig. 15a* and *b*.

The circuits in *15a* and *b* have a DC offset voltage at the output—the gate-source voltage at the given drain current. For the JFETs I used in the test setup, I measured a 0.2V offset. If you need zero DC output, you can use the circuit in *Fig. 15c*. Here the constant-current source is made with the same type of JFET as the follower.

If the two JFETs are matched and the two source resistors are equal, then the DC offset will be very small. With two matched K170BLs, I measured less than 1mV offset. (It would probably be even lower if you used here a dual monolithic JFET like the K389BL/V.) DC drifts tend to cancel out as well, because of the matched devices. The circuit also has

very low THD (see column 3 of *Table 3*).

### Follower Feature

One of the most important features of a follower is its ability to drive low-impedance loads. I checked all three circuits with 1k and 10k loads at 3V RMS output. With 1k they measured 1%, 1.7%, and 0.23%, respectively. Although its output impedance is actually higher than the circuits in *Figs. 15a* and *b*, that in *15c* is better in driving low-impedance loads. With a 10k load, the circuits in *15b* and *15c* didn't have many problems. THD was 0.004 and 0.0022%.

My choices of source followers are shown in *Fig. 16*. The circuit in *16a* is a JFET version of the tube White cathode follower.<sup>5</sup> Basically, the circuit is an extension of *Fig. 15c*, in that the follower is fed with a constant-current source, but in addition the drain current of the current source is modulated by the AC signal. When the output signal goes positive, the tail current decreases, and when it goes negative, the current increases. The result is a significant reduction of the output impedance and an apparent increase in drive capability.

The output impedance with the devices shown measured 2.3Ω. The input capacitance is about 5pF, the same as the previous source-follower circuits. The penalty for the drive capability is a slight increase of distortion (see column 4 in *Table 3*). The THD with a 1k load and 3V RMS is 0.0095%. The necessary gate drive voltage is derived from a small resistor in the source follower's drain circuit, and it is AC-coupled to the current source.

### Power Dissipation

John Curl used the complementary JFET source follower shown in *Fig. 16b* in the JC-2 phono-preamp module.<sup>6</sup> The JFETs work in Class A as long as the peak load current is less than twice the bias current. After that, the circuit works in Class AB. I usually let the two matched devices work at  $I_{DSS}$ , to maintain as much Class A headroom as possible. However, you must watch the power dissipation. If  $I_{DSS}$  is such that the power dissipation is more than the maximum allowed, then you need to insert a source resistor to reduce the drain current or select a device with lower  $I_{DSS}$ .

I tested the circuit with K170/J74, both the BL and V types, and got excellent results. The THD is shown in column 4 of *Table 3*. Depending on the matching, the offset can be as low as 1mV. The output impedance is about

18Ω, and the input capacitance is 28pF. Most important, the circuit can drive low-impedance loads without distress—the 1k/3V RMS THD was 0.0078%. With a 10k load, there is no difference from the no-load results.

I also tested the source followers for THD caused by the voltage-dependence of the input capacitance. Since the voltage excursion is much larger at the input because of the unity gain, the circuits are also more susceptible to the distortion. There is no significant increase up to a 10k source; however, at 50k the THD is increasing by an order of magnitude. Normally this is no problem, because the source impedance is usually very low. However, in certain applications such as filters, this can cause distortion.

Of course, using any of these source-follower buffer circuits with the SE and differential amplifiers discussed previously solves only one of the problems stated at the start of this section—the drive-capability problem. The DC voltage is still there. Given the topology of these circuits, you must use a capacitor at the output to block the DC voltage. Naturally, you can also solve this problem by using level-shifting circuits, but it requires a bit more circuit design. For now, I'll look at an all-JFET balanced/SE all-FET line amp, using the circuits already developed.

### The Balanced/SE All-JFET Line Amp

The schematic shown in *Fig. 17* consists of the differential amplifier Q1/Q2, cascoded with Q3/Q4, and the output buffers Q5/Q6 and Q7/Q8. The differential amplifier uses a dual monolithic K389V JFET. Each JFET operates at just over 2mA, this current supplied by the J511 constant-current source. The 330R source resistors provide local feedback and control the gain of the differential amplifier. The trimpot P1 cancels out small imbalances between the two JFETs, but it is normally unnecessary with monolithic duals, and you can leave it out.

The Cascode FETs are K246BLs. The output buffers are those I developed from the tube White Cathode Follower, shown in *Fig. 16a* ("modestly" called the "Borbely" source followers here). The supply voltage is ±36V. Of course, you can make the negative supply much less than 36V; the constant-current source requires only a couple of volts for proper operation. I made them both 36V to be able to try other configurations.

The output caps must be of highest quality in order to preserve the outstand-

ing sound quality of this simple circuit. If you are likely to drive loads down to 1k, then the caps must be a minimum of 10 $\mu$ F. If you are driving normal 10k or higher loads, you can get away with a 1 $\mu$ F or 2.2 $\mu$ F cap. I tried the Hovland Musicaps, which are rather neutral, but there are plenty of good caps on the market you can try.

Normal oil caps are *not* for this circuit; they destroy the excellent resolution to a “nice” blurred mish-mash. (Don’t get the idea that I don’t like oil caps; I use them in some of my amps.) I would have liked to try some silver-foil caps, but, alas, the prices are more ridiculous than the cable prices, and I refuse to play that game. (If anyone knows of a reasonably priced silver-foil cap, please let me know.)

You can use the line amp with unbalanced or balanced sources, and you can feed power amps with balanced or unbalanced inputs. However, you should really take advantage of its superior performance in balanced operation, as I mentioned before. Should you use it with unbalanced sources, then you must short the –INP to ground. And in the unlikely event that you don’t wish to take advantage of the balanced outputs, you can leave out the circuit around Q5/Q6, i.e., the negative output. I recommend a 10k or 20k ladder attenuator as a volume control. Good luck with the JFETs, the “New Frontiers” in audio amplification. ■

### References

1. Erno Borbely, “New Devices for Audio from National Semiconductor,” *Audio Amateur* 5/83, p. 7.
2. Nelson Pass, <http://www.passlabs.com>.
3. Erno Borbely, “Third Generation MOSFETs: The DC-100,” *The Audio Amateur* 2/84, p. 13.
4. Walt Jung, private communication.
5. Erno Borbely, “Differential Line Amp with Tubes,” *GA* 1/97, p. 24.
6. John Curl, “Classic Circuitry,” *The Audio Amateur* 1977, Issue 3, p. 48.

### Acknowledgments

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