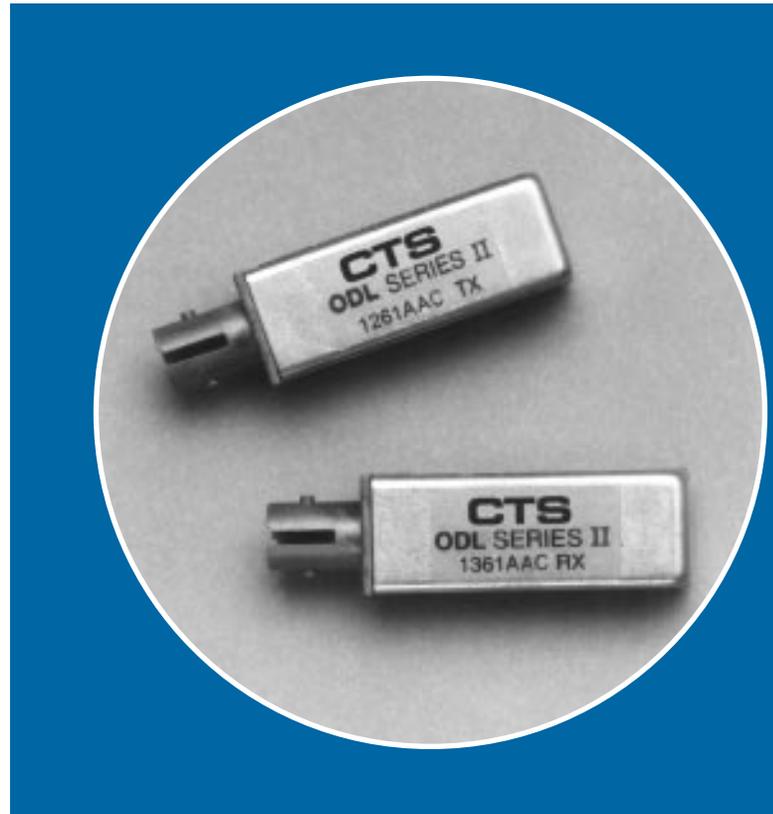


ODL[®] 50 Series II Lightwave Data Link

Features

- Economical package utilizes low-cost, conductive plastic housing
- TTL compatible
- Standard 16-pin DIP footprint
- ST[®] Receptacles
- Typical link margin: 17 dB
- Wide dynamic range
- Link status flag and mute (output disable)
- Compact, light, EMI-shielded package
- No additional circuitry required
- Selectable scrambler circuitry provides 50% duty cycle
- Single 5 V power supply
- High-reliability modules incorporate single IC design
- Compatible with various fiber sizes



The optical data link provides electrical isolation and intrusion-resistant data transmission between systems at speeds up to 50 Mbits/s.

Applications

- Telecommunications
 - Network control and timing
 - Link between PBX modules
 - Local loops
- Data communications
 - Locals area networks (LANs)
 - Point-to-point
 - Channel extenders
- Secure communications
 - Banking
 - Military
 - Channel extenders

Description

The ODL 50 Series II Lightwave Data Link is a high-performance link designed for data rates from 1 Mbit/s to 50 Mbits/s (NRZ) at distances up to 3 km using 62.5/125 μm optical fiber. In addition to the typical transmit and receive functions found in lightwave data links, capabilities also include data encoding/decoding and clock recovery and retiming. Encoding is included in the transmitter; decoding is available with the addition of an optional companion clock recovery IC.

The 1261AAC Transmitter and 1361AAC Receiver each contain a CMOS IC that performs the data-handling functions. Both devices use a 5 V power supply. The data link is designed to operate with 62.5/125 μm optical fiber, but is also compatible with other fibers (see Table 1).

The transmitter and the receiver are housed in advanced, yet low-cost packages. The device is made of a conductive plastic that reduces the data link's susceptibility to radiated EMI and RFI fields (Non-conductive plastic version is available). The plastic offers corrosion resistance while maintaining high heat resistance (>200 °C) and UL V-O flame retardancy; the oxygen index, as determined by ASTM Standard D2863-77, is 37. Metal covers are used to provide receiver shielding and LED heat sinking for high-reliability applications. If extra attachment strength is desired, mounting holes provided in the package bottoms may be used to secure the devices.

In addition to the 850 nm LED, the transmitter contains a temperature-compensated LED driver IC, which includes an optional-use seven-stage data scrambler circuit. The pin selectable scrambler enriches the data stream over the link with transitions and provides a 50% duty cycle, allowing full use of the 50 Mbits/s maximum data rate.

The receiver consists of a silicon PIN photodiode and an IC. The IC contains pre- and postamplifiers, and a decision circuit. A carrier-detection flag indicates loss of optical power by providing a TTL-logic high at the link-status monitor output pin. The mute input provides the user with the capability of disabling the output. The mute input signal can originate from either the link status flag output pin or a user-supplied TTL level input.

The link status flag monitors the integrity of the optical fiber communication channel. During normal operation, the output of this pin will be a TTL low. The output will switch to a TTL high if any of the following events occur:

- The optical fiber is broken.
- The optical transmitter stops transmitting.
- The link budget of the system is exceeded.

The output of the link status flag is capable of driving a minimum of two standard TTL loads.

Description (continued)

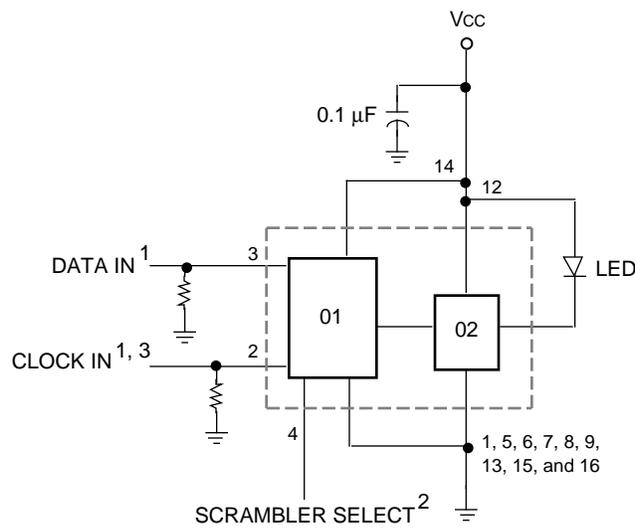
Table 1. ODL Series II Lightwave Data Link Fiber Compatibility

All values are typical and are referenced to standard Multimode Fiber (62.5/126 μm).

Fiber Size (μm)*	Transmitter Launch Power Change (dB)	Receiver Sensitivity Change (dB)†
50/125	-2.5	0
62.5/125	0	0
85/125	+1.8	0
100/140	+3.0	0

* Inner-core/outer-core diameters.

† Does not include the additional dispersion due to differences in fiber-core sizes.

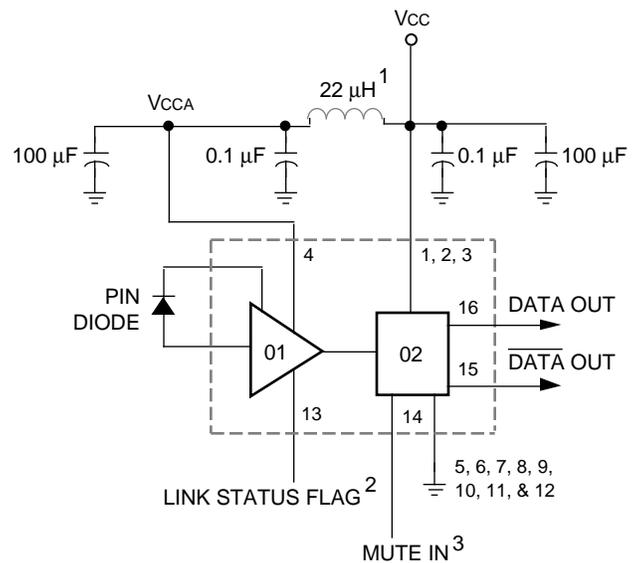


01 DATA SCRAMBLER
02 LED DRIVER

1. To preserve pulse shape, the source driving the transmitter may need to be terminated for impedance matching.
2. To enable scrambler, tie to ground; to disable scrambler, tie to Vcc.
3. A clock input is required only when the scrambler is in use. For normal use (scrambler disabled), no clock input is required and this pin should be left open.

Note: Pins 10 and 11 are internally connected. Do **not** connect externally. Dashed lines indicate circuitry integrated on a single silicon IC. The decoupling circuit shown in the block diagram should be used to ensure adequate power supply filtering and noise rejection. Capacitors should be placed as close as possible to the appropriate pins.

Figure 1. Transmitter Block Diagram with Recommended Decoupling Circuit



01 RECEIVER (PREAMPLIFIER/POSTAMP)
02 DECISION CIRCUIT

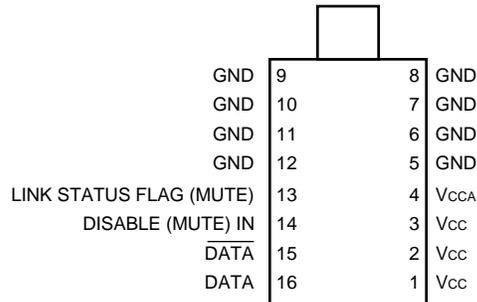
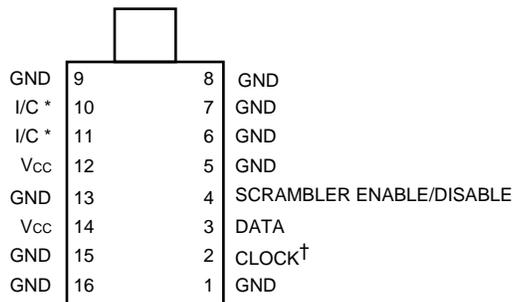
1. The dc resistance of the 22 μH inductor must be ≤1 Ω .
2. TTL high at link status flag output indicates loss of optical signal.
3. Ground to enable DATA and DATA outputs; tying to TTL high will disable outputs upon loss of optical signal.

Note: Pins 5 through 12 should be grounded in all use conditions. Dashed lines indicate circuitry integrated on a single IC chip.

Figure 2. Receiver Block Diagram with Recommended Decoupling Circuit

Pin Information

Top view



* Internal connection; must be left as an open circuit.

† Use only with scrambler.

Figure 3. Transmitter Pin Diagram

Figure 4. Receiver Pin Diagram

Application Considerations

A fiber-optic receiver employs a very high gain transimpedance amplifier. It is designed to detect and amplify signal levels that are only nanoamperes in amplitude. Any unwanted signals which couple into the receiver circuitry will cause a decrease in the receiver's sensitivity and may also degrade the performance of the receiver's signal detect indicators.

As with any sensitive or high-speed component, to obtain optimum performance from fiber-optic data links, careful attention must be given to the printed-wiring board design. The routing of sensitive input traces relative to other components and signal lines must be considered in great detail.

To minimize the coupling of unwanted noise into the receiver, transmitter input traces and other traces carrying high-level or high-frequency signals should be routed as far away as possible from the receiver pins. If physical separation is not possible, then the interleaving of signal and ground traces should be considered.

The choice of board construction is also important. As a minimum, a double-sided printed-wiring board having a large ground plane directly beneath the optical components should be utilized. In applications where a large number of other devices or devices operating

at high clock frequencies are included on the circuit card, a multilayer circuit board is preferred. This allows for the separation of power and ground connections and provides a means to isolate sensitive traces from high-level signals which might couple to the sensitive inputs.

When laying out the printed-wiring board for the 1261/1361 AAC, note that the plastic housing is conductive. Avoid placing topside metal or vias that are not at ground potential in the areas beneath the housing standoffs or beneath the areas where the metal shield is soldered to the package (see Outline Drawing). The preferred PWB layout for these devices is to employ a ground plane on the component side of the board, directly under the transmitter and receiver.

Special attention must be paid to the power supply pins to ensure that they are well filtered. Noise that couples into the receiver through the power supply pins can degrade performance. To minimize coupled power supply noise, the power supply filter circuit shown in Figure 2 is recommended. The capacitors should be high-quality ceramic devices rated for RF applications. Place these capacitors as close as physically possible to the receiver power pins. Surface-mount capacitors mounted adjacent to the pins are ideal.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T _{stg}	-40	100	°C
Lead Soldering Temperature/Time	—	—	240/10	°C/s
Supply Voltage	V _{cc}	0	6.0	V
Transmitter Input Voltage	V _{IH}	0	V _{cc}	V
Receiver Short-circuit Output Current	I _{os}	—	20	mA

Loading and Layout Requirements

The performance indicated in this data sheet is achieved by following these recommendations:

- The decoupling circuit shown in the Block Diagrams should be used. Capacitors should be placed as close as possible to the appropriate pins.
- A multilayer board should be used so that a ground plane occupies the area around and beneath the receiver. This permits spreading of currents that may otherwise induce noise on leads connected to sensitive circuitry within the receiver. All pins listed as ground pins (pins 5 through 12) should be directly attached to the ground plane with no additional lead length.
- The DATA and $\overline{\text{DATA}}$ outputs should be terminated identically. The load should not exceed 15 pF or, for optimum performance, require more than I_{oL} = 2 mA.
- For optimum performance, the load on the link status flag should not exceed 15 pF or require more than I_{oL} = 2 mA.

Electrical/Optical Characteristics

Table 3. Transmitter Characteristics

All values include temperature and supply voltage variations. Values are determined at 50 Mbits/s with $2^7 - 1$ pseudorandom word length and NRZ coding.

$V_{CC} = 5.0 \text{ V} \pm 5\%$; $T_C = 0 \text{ }^\circ\text{C}$ to $70 \text{ }^\circ\text{C}$; typical values are at $V_{CC} = 5.0 \text{ V}$ and $T_C = 25 \text{ }^\circ\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Input Data Voltage:*					
Low	V_{IL}	0.2	—	0.8	V
High	V_{IH}	2.0	—	V_{CC}	V
Input Current:					
Low	I_{IL}	—	—	1	nA
High	I_{IH}	—	—	1	nA
Power Supply Current Drain	I_{CC}	—	110	150	mA
Peak Optical Power†	P_{OH}	25.1 (–16)	60.6 (–12.2)	—	μW (dBm)
Static Extinction Ratio (P_{OH}/P_{OL})‡	ER	100 (20)	>200 (>23)	—	(dB)
Output Rise Time§	t_R	—	5	7	ns
Output Fall Time§	t_F	—	5	8	ns
Propagation Delay					
Low to High	t_{PLH}	—	11	16	ns
High to Low	t_{PHL}	—	11	16	ns
Pulse Width Distortion	PWD	—	1.2	4	ns
Optical Wavelength	λ	850	875	900	nm
Spectral Width	$\Delta \lambda$		50	70	nm
Data Rate	BR	dc	—	50	Mbits/s
Power Dissipation	P_{DISS}	—	0.55	0.79	W

* As with all CMOS devices, V_{CC} must be applied before the data and clock inputs (pins 3 and 2 respectively). In addition, any input must **not** exceed V_{CC} and must **not** be less than ground. This recommendation is intended to minimize the potential of ESD and latch-up problems for all CMOS devices. These modules have ESD protection circuitry.

† Peak optical power is defined as average optical power plus 3 dB. Steady-state beginning-of-life power coupled into 0.275 NA (determined by the Far-Field Radiation Pattern Measurement described in EIA test procedure RS-455-47.62.5), 62.5/125 μm connectorized fiber. The data-stream input is 2 Vdc.

‡ P_{OL} is defined as the peak optical power at logic low.

§ Rise and fall times are for 10% and 90% transition times. Square wave (1010 . . .) is used as data-stream input.

Electrical/Optical Characteristics (continued)

Table 4. Receiver Characteristics ^{1,2}

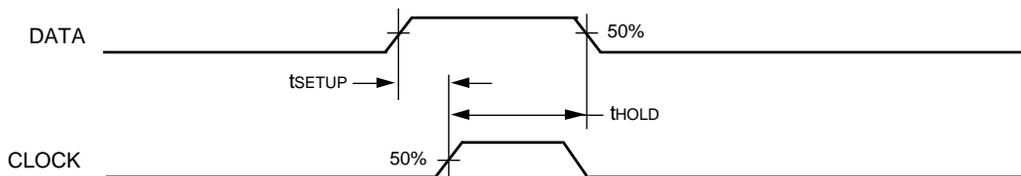
All values include temperature and supply voltage variations. Values are determined at 50 Mbits/s with a $2^7 - 1$ pseudorandom word length and NRZ coding. A TTL load with 5 pF capacitance was used.

$V_{CC} = 5.0 \text{ V} \pm 5\%$; $T_C = 0 \text{ }^\circ\text{C}$ to $70 \text{ }^\circ\text{C}$; typical values are at $V_{CC} = 5.0 \text{ V}$ and $T_C = 25 \text{ }^\circ\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage:					
Low	V_{OL}	—	<0.2	0.5	V
High	V_{OH}	2.4	>4.0	—	V
Output Current:					
Low	I_{OL}	—	—	2	mA
High	I_{OH}	—	—	-150	μA
Power Supply Current Drain	I_{CC}	—	86	110	mA
Peak Optical Sensitivity ³ @ 10^{-9} BER	SEN	2.00 (-27)	1.00 (-30)	—	μW (dBm)
Maximum Optical Input Power (peak) ⁴ @ 10^{-9} BER	$P_{IN \text{ MAX}}$	—	—	100 (-10)	μW (dBm)
Output Rise Time ⁵	t_R	—	1.8	5	ns
Output Fall Time ⁵	t_F	—	2.0	5	ns
Propagation Delay					
Low to High	t_{PLH}	—	33.5	50	ns
High to Low	t_{PHL}	—	33.5	50	ns
Eyewidth @ 50 Mbits/s, 10^{-6} BER, and -28 dBm Average Power Input (P_I)	EW	12	15	—	ns
Optical Wavelength for Rated Sensitivity	λ	825	—	900	nm
Data Rate	BR	1	—	50	Mbits/s
Power Dissipation	P_{DISS}	—	0.43	0.58	W

1. Since the receiver is ac-coupled, a 6 ms preamble is recommended before valid data is present at outputs. In addition, we recommend the use of scrambling or Manchester encoding for use above 40 Mbits/s.
2. Use of scrambler is recommended when data stream provides either less than 30% or more than 70% duty cycle. Also, if the scrambler is not being used, the input data stream must contain a transition at least every 7 μs .
3. Peak optical input power is defined as average power plus 3 dB.
4. The device has been operated satisfactorily with peak optical input levels up to -8 dBm.
5. Rise and fall times are for 10% and 90% transition times and are determined with an average optical power input of -23 dBm. A square wave (1010 . . .) is used as data-stream input.

Timing Characteristics



Notes:

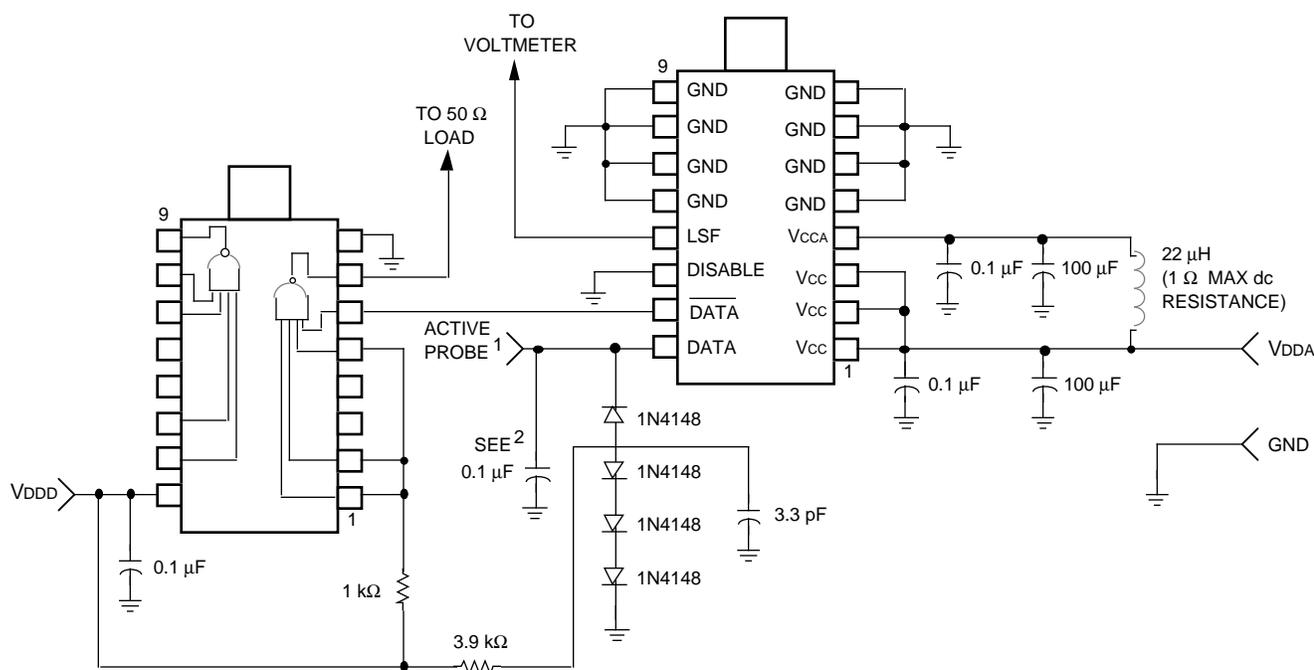
The setup and hold times must both exceed 3.0 ns.

t_{SETUP} is the minimum time information must be present at the DATA input before the transition of the CLOCK.

t_{HOLD} is the minimum time information must remain unchanged at the DATA input after the transition of the CLOCK.

Figure 5. Scrambler-Mode Timing Diagram

Test Circuit



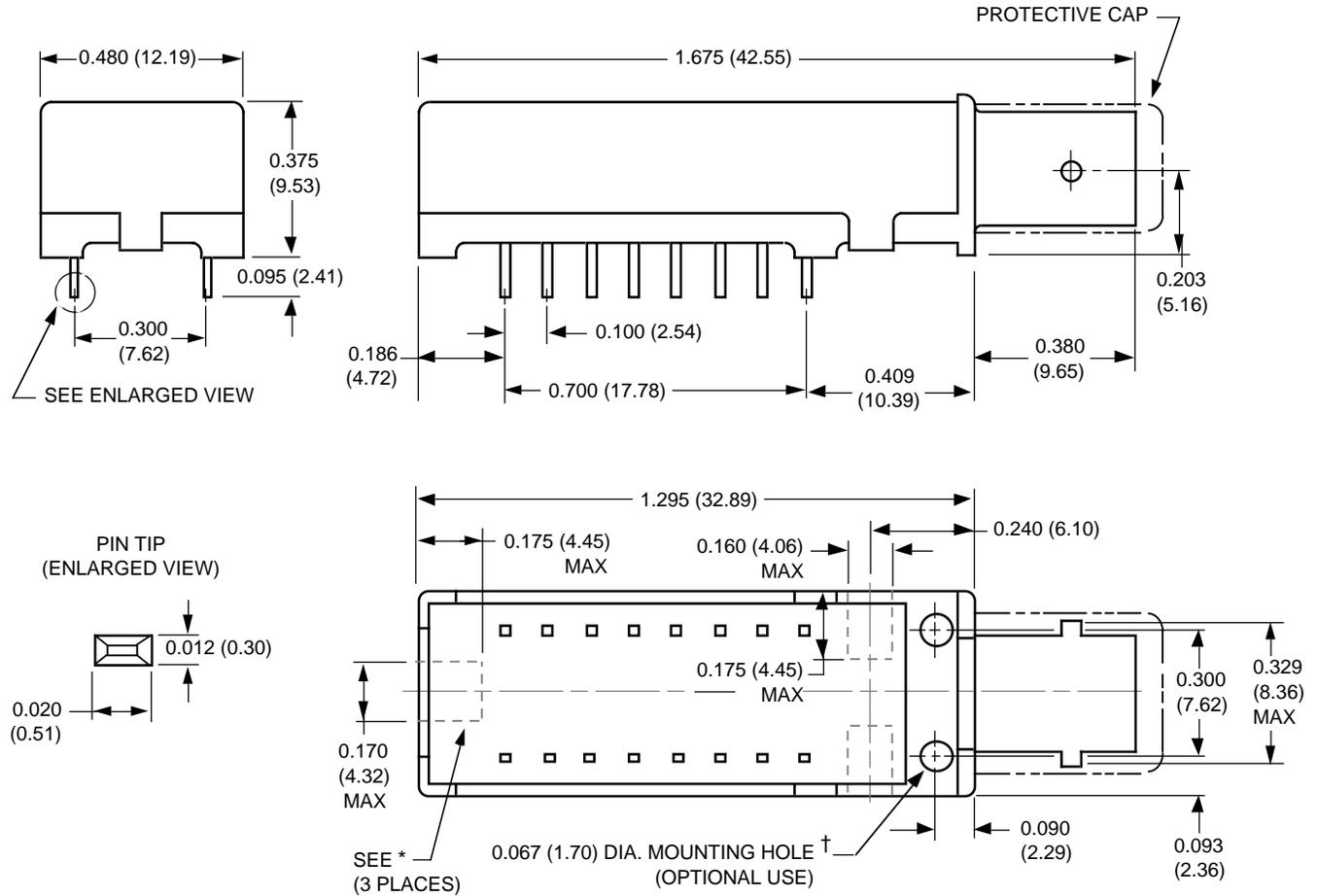
1. Tektronix³ P6202A or Tektronix P6201 or HP⁴54001A. Active probes are recommended.
2. This includes the capacitance from the probe.
3. Tektronix is a registered trademark of Tektronix, Inc.
4. HP is a registered trademark of Hewlett-Packard Company.

Figure 6. Test Circuit for Receiver

Outline Diagrams

Dimensions are in inches and (millimeters). Transmitter weight: 5.5 g. Receiver weight: 5.5 g.

CAUTION: These components are not hermetically sealed. Do not totally immerse in solvents.



* Do not place signal or power supply metal within **outlined areas around solder tabs**. Metal shield and plastic housing are at ground potential.

† Use a #1 self-tapping screw. Insert screw before soldering module on PWB. Maximum length = 0.3 in. + circuit board thickness.

Ordering Information

Table 6. Ordering Information

Device	Part Number
<i>ODL 50 Series II Transmitter</i>	1261AAC
<i>ODL 50 Series II Receiver</i>	1361AAC
<i>ODL 50 Series II Transmitter (Non-Conductive)</i>	1261AAC1
<i>ODL 50 Series II Receiver (Non-Conductive)</i>	1361AAC1

Notes

Order From

Or for additional information, contact your local CTS Distributor, Agent, Sales Representative or in:

U.S.A., EUROPE, ASIA PACIFIC:

CTS Microelectronics, 1201 Cumberland Avenue, W. Lafayette, Indiana 47906
Phone 317-463-2565, FAX 317-497-5399

JAPAN:

CTS Corporation, Japan Sales Office, Mori Building No. 32, 4F, 4-30, 3 Chome Shibakoen, Minato-ku Tokyo 105, Japan
Tel. 81-3-5472-6201, Fax 81-3-5472-6234

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