Discrete Opamp in DIP- 8 Package -- Design Considerations

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Circuit Description & Component Choice

The design described here is an attempt to produce an all-FET discrete opamp that is pin and size compatible to a standard single opamp in DIP package, such as the NE5534. The circuit is based on the discrete opamp design (Fig. 14, JFET input, 3-stage) published by Nelson Pass. A similar circuit was also published by Erno Borbely in his recent preamp article. The only change is the use of dual N-JFET's biased at Idss for the 3rd stage. The reason not to use complementary matched JFET's for the output stage, as in Borbely's design, is only due to the unavailability of P-JFET's in SMD packages. This is also why JFET's are not used for the second stage, as Borbely did with a folded cascode. The entire circuit runs in pure Class A. Thermal dissipation is approximately 1.2W, with ±15V supply rails. The circuit will take higher voltages, only limited by thermal dissipation.

Versions 1 & 2

In the first version of this design, the natural choice of device for the first stage was a LSK389B in SOT23-6 package for the input differential pair, to be biased at 2.8mA each. LSK389A could also be used for that purpose. The LSK389 (or 2Sk389) requires a minimum of about 3mA bias to ensure low noise. Bias of the differential pair was provided by a single current regulating diode (F562). The drain resistor of the positive input JFET was set at 1.1k, to give a voltage of about 3V. This was applied to drive the MOSFET of the 2nd stage, a ZVP3306F, biased at 10mA by a current regulating diode (F103). The output at the drain was further buffered by a simple JFET follower a la John Curl, using a single LSK389B (also in SOT23-6) biased at Idss (no source degeneration) for best Idss match and thermal tracking.

The first stage would have a voltage gain of 22 (= 1100/50). The second stage would have a voltage gain of 7700 (=170000/22). This is because the transconductance of the ZVP3306 is about 45mS at 10mA, giving an effective source resistance of 22ohm, whereas the F103 has a dynamic resistance of 170kohm. With the follower effectively at unity gain (assuming loads > 3k), the total open loop gain would be 170000, giving about 85dB negative feedback when configured with a closed loop gain of 10. The circuit is not unity gain stable without compensation (C_{dom}). As the use of non-linear SMD ceramic capacitors was thought undesirable, pin 8 of the package is so wired that it could be used to provide access to the MOSFET gate, so that an external compensation capacitor could be connected between Pin 8 and the output pin. Should this be unnecessarily for certain applications, it would be best to remove the connection to pin 8 either on the package or the PCB, or both. Solder-pads were also provided in the PCB layout for a 100p NPO ceramic capacitor in 0603 package between gate and drain of the MOSFET if internal compensation was desired.

A PCB layout was successfully designed within a footprint of 10x10mm, double sided with one pin-through. However, the biggest issue was the non-availability of the LSK389 in SOT-23-6. The more readily available SOIC-8 package is simply too large for the desired footprint. Therefore a Version 2 layout was done based on single LSK170s which would then have to be matched manually for both the differential pair and the output buffer. The only disadvantage is the somewhat inferior thermal coupling of the JFET pairs.

Version 3

Version 2 would have been the circuit for implementation but for the fact that the LSK170 is at least 2x more expensive than a standard 2SK170, even in quantities of 100+. In addition, there are reports of problems of the manufacturer meeting the noise specifications.

After some searching, alternative components were found – BF861A for the 1st stage and BF862 for the 2nd stage. In principal, one could use BF862 for both purposes. The only disadvantage of the BF861 is somewhat higher noise at lower frequencies (in the order of 4 nV/√Hz). The BF862 was reported to have much lower noise, below 1 nV/√Hz at 1mA and 100Hz (ref. Scott Wurcer in DIY Audio).

Both devices are readily available at affordable prices even in small quantities. A batch of 40 JFETs of each type was measured. The spread of Idss for the BF861A was between 3.8mA and 4.8mA. The same for BF862 was between 16mA and 18mA. About 50% of the JFETs can be paired to better than 1% Idss. And the rest can still be used as current sources for 1st and 2nd stage, in place of the F562 and F103.

Some changes to the original circuit are necessarily. The first stage now runs at about 4mA total bias (2mA per LTP FET). The second stage runs at about 18mA, similar to the output stage. The somewhat higher Vgs for the ZVP3306F, in addition to the reduced bias of the 1st stage, is compensated for by changing the drain resistor to around 1.5k, thus further increasing the open loop gain by some 40%.

Layout

A double-sided PCB of 10x10x0.8mm is used for holding the components. This small size will most certainly fit in any applications currently using a standard opamp in DIP package. The first stage has the least thermal dissipation, and is thus placed on the bottom side of the PCB. Both second and third stages are placed on the top side of the PCB for best thermal dissipation and direct coupling to a heatsink. A single jumper through the PCB connects the output of the first stage to the input of the second stage. The drain resistor of the differential pair is placed on the top side closed to the gate of the MOSFET, though a second location is provided on the bottom side for an additional trim-resistor for output DC offset trimming. 0603 resistors are not used as they are reported to be highly non-linear (ref. John Westlake in DIYAudio).

Thermal Management

The total dissipation of the opamp with +/- 15V rails and the bias currents as mentioned above is approximately 1.2W. Most of the components in the 2nd and output stages are running at close to their maximum power rating if not cooled additionally. A single SOT23 has a junction-to-ambient thermal resistance of about 360 K/W, limiting the power dissipation to about 300mW at a junction temperature of 150°C. However, the junction-to-case thermal resistance is around 110 K/W. Thus the use of an additional heatsink can be effective. For example, the Fischer ICK PLCC24 has an overall size of 12x12x8mm, and a thermal rating of 25K/W. This means that the heatsink temperature at 1.2W is about 55°C (assuming ambient temperature of 25°C). The junction temperature of the output JFETs can then be reduced to some 82°C. The JFETs are to be glued to the heatsink using “Arctic Silver” silver epoxy. The whole package can be potted further with thermal conductive potting compound.

The bottom-side components have much lower dissipation and are only thermally connected to the heatsink via the potting compounds.

The overall package size without the heatsink is 10x10x3mm, essentially the same size as a standard 8-pin DIP device. With the heatsink, overall size is about 12x12x11mm.

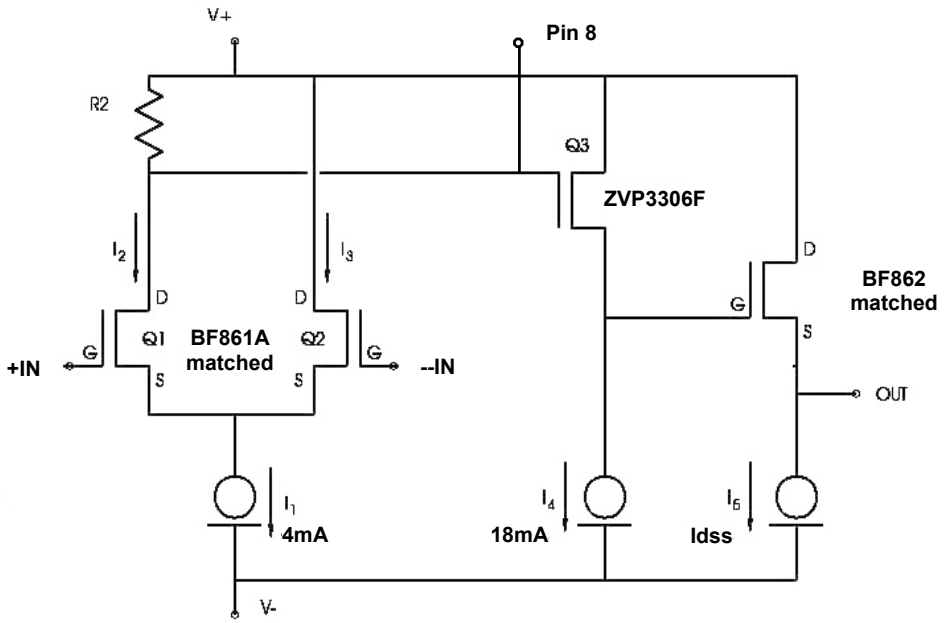

Fig. 1 Schematic Diagram

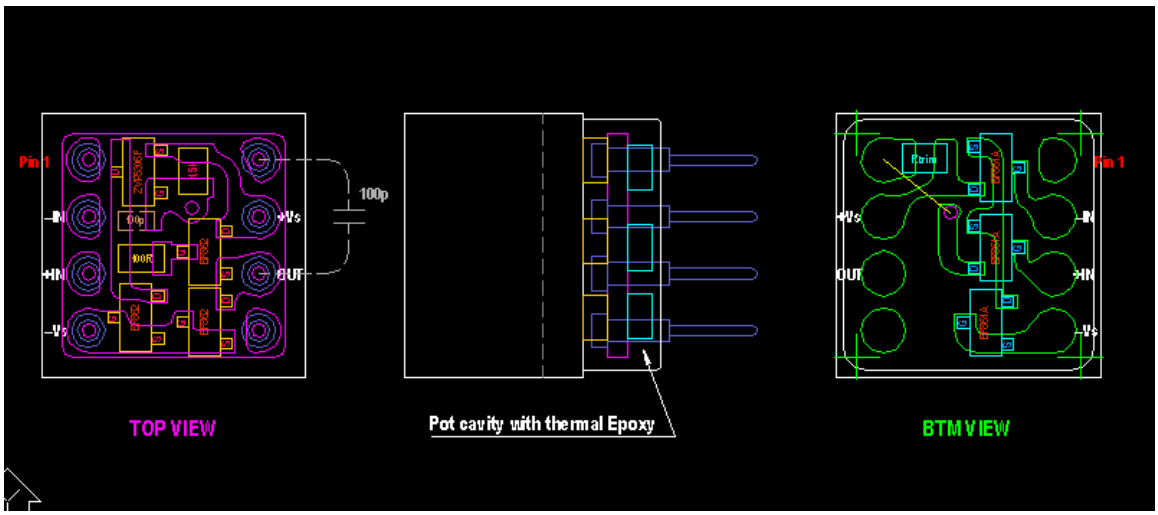

Fig. 2 PCB Layout