5.4 THE CASCODE AMPLIFIER

The DC analysis of the cascode amplifier was presented in Chapter 3. Let us now carry out the complete AC analysis for the cascode amplifier of Figure 5-27 as shown below:

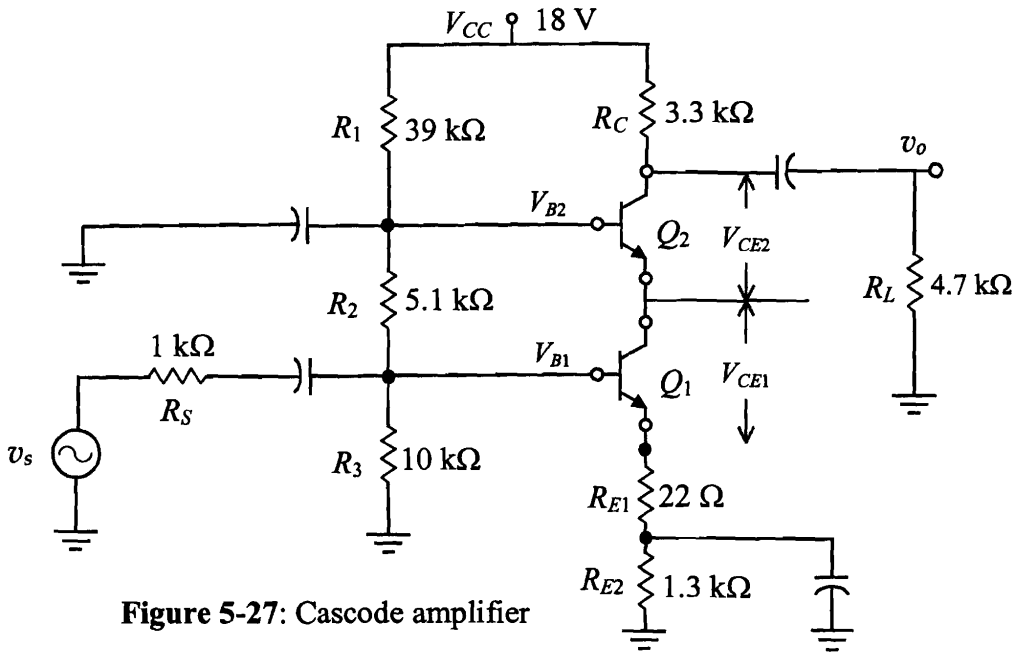

Figure 5-27: Cascode amplifier

DC analysis:

The base voltage V_{B1} is determined with Equation 3-49, as follows:

$$V_{B1} = V_{CC}\frac{R_3}{R_1 + R_2 + R_3} = 18\text{ V}\frac{10\text{ k}\Omega}{39\text{ k}\Omega + 5.1\text{ k}\Omega + 10\text{ k}\Omega} = 3.327\text{ V}$$

$$V_{E1} = V_{B1} - V_{BE} = 3.327\text{ V} - 0.7\text{ V} = 2.627\text{ V}$$

$$I_{E1} = \frac{V_{E1}}{R_E} = \frac{2.627\text{ V}}{1.322\text{ k}\Omega} \cong 2\text{ mA}, \quad I_{C1} \cong I_{E1} = I_{C2} \cong I_{E2} = 2\text{ mA}, \quad r_e = \frac{26\text{ mV}}{I_E} = 13\ \Omega$$

For the 2N2222 transistor, the I_C of 2 mA corresponds to $\beta = 160$.

The base voltage V_{B2} is determined with Equation 3-56, as follows:

$$V_{B2} = V_{CC}\frac{R_2 + R_3}{R_1 + R_2 + R_3} = 18\text{ V}\frac{10\text{ k}\Omega + 5.1\text{ k}\Omega}{39\text{ k}\Omega + 5.1\text{ k}\Omega + 10\text{ k}\Omega} = 5\text{ V}$$

$V_{E2} = V_{C1} = V_{B2} - V_{BE} = 5 - 0.7\text{ V} = 4.3\text{ V}$

$V_{C2} = V_{CC} - I_C R_C = 18 - (2\text{ mA} \times 3.3\text{ k}\Omega) = 11.4\text{ V}$

$V_{CE1} = V_{C1} - V_{E1} = 4.3 - 2.6\text{ V} = 1.7\text{ V}$

$V_{CE2} = V_{C2} - V_{E2} = 11.4\text{ V} - 4.3\text{ V} = 7.1\text{ V}$

AC analysis:

We will start the AC analysis with the AC equivalent circuit, which will be a cascade of a common-emitter followed by a common-base configuration, as shown in Figure 5-28 below:

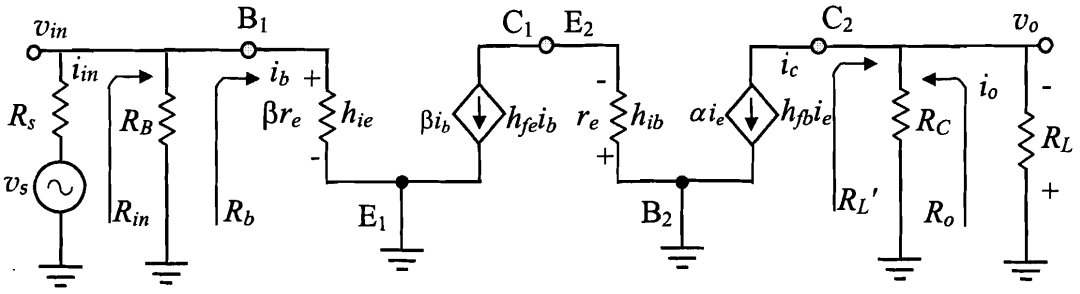

Figure 5-28: Small-signal equivalent circuit of Figure 5-27

First stage (common-emitter):

$$R_b = \beta(r_e + R_{E1}) \tag{5-61}$$

$R_b = 160(13\ \Omega + 22\ \Omega) = 5.6\ \text{k}\Omega$

The resistance R_B is the parallel combination of R_2 and R_3.

$$R_B = R_2 \parallel R_3 \tag{5-62}$$

$R_B = 10\ \text{k}\Omega \parallel 5.1\ \text{k}\Omega = 3.77\ \text{k}\Omega$

The input resistance R_{in} is the parallel combination of R_B and R_b.

$$R_{in} = R_B \parallel R_b \tag{5-63}$$

$R_{in} = 3.77\ \text{k}\Omega \parallel 5.6\ \text{k}\Omega \cong 2\ \text{k}\Omega$

$$R_o = R_C \tag{5-64}$$

$R_o = 3.3\ \text{k}\Omega$

The load for the first stage is the input resistance of the second stage, which is simply r_e. Hence, the gain of the first stage is determined with Equation 5-43 as follows:

$$A_{v1} = \frac{v_{C1}}{v_{in}} = -\frac{R_{L1}'}{r_e + R_{E1}} = -\frac{r_e}{r_e + R_{E1}} \tag{5-65}$$

Second stage (common-base):

The load for the second stage is the parallel combination of R_C and R_L.

$$R_L' = R_C \parallel R_L \tag{5-66}$$

$R_L' = 3.3\ \text{k}\Omega \parallel 4.7\ \text{k}\Omega = 1.94\ \text{k}\Omega$

The gain for the second stage is determined as follows:

$$A_{v2} = \frac{v_o}{v_{C1}} = \frac{\alpha i_e R_L'}{\beta i_b r_e} \cong \frac{\beta i_b R_L'}{\beta i_b r_e} = \frac{R_L'}{r_e} \tag{5-67}$$

The overall voltage gain is the product of the two gains.

$$A_v = \frac{v_o}{v_{in}} = \frac{v_{C1}}{v_{in}} \cdot \frac{v_o}{v_{C1}} = A_{v1} \cdot A_{v2}$$

$$A_v = -\frac{R_L'}{r_e + R_{E1}} \tag{5-68}$$

$$A_v = -\frac{1.94\,\text{k}\Omega}{35\,\Omega} = -55.429$$

$$v_{in} = v_s \frac{R_{in}}{R_s + R_{in}} = 100\,\text{mV}\frac{2\,\text{k}\Omega}{3\,\text{k}\Omega} = 66.667\,\text{mV}$$

$$v_o = A_{v(WL)}\, v_{in} = 55 \times 66.667\,\text{mV} = 3.667\,\text{V}$$

Practice Problem 5-5

Cascode Amplifier

ANALYSIS

Determine all the amplifier parameters for the following cascode amplifier:

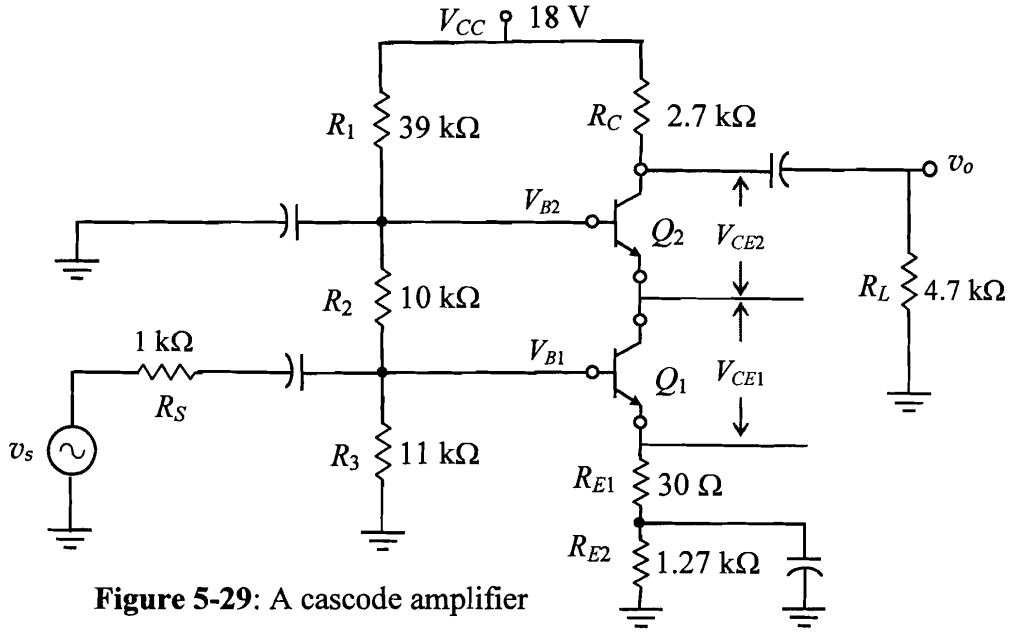

Figure 5-29: A cascode amplifier

Answers:

$I_C = 2$ mA, $V_{CE2} = 7$ V, $R_{in} = 2.975$ kΩ, $R_o = 2.7$ kΩ, $A_v = -40$

Section Summary — Cascode Amplifier — **ANALYSIS**

Summary of Equations for the Analysis of the Cascode BJT Amplifier

DC analysis:

$$V_{B1} = V_{CC}\frac{R_3}{R_1 + R_2 + R_3}, \qquad V_{E1} = V_{B1} - V_{BE}, \qquad I_{E1} = \frac{V_{E1}}{R_E}$$

$$I_{C1} \cong I_{E1} = I_{C2} \cong I_{E2} \qquad r_e = \frac{26\text{ mV}}{I_E}$$

$$V_{B2} = V_{CC}\frac{R_2 + R_3}{R_1 + R_2 + R_3}, \qquad V_{E2} = V_{C1} = V_{B2} - V_{BE}$$

$$V_{C2} = V_{CC} - I_C R_C, \qquad V_{CE1} = V_{C1} - V_{E1}, \qquad V_{CE2} = V_{C2} - V_{E2}$$

AC analysis:

If R_E is split; that is, $R_E = R_{E1} + R_{E2}$

$$A_v = -\frac{R_L'}{r_e + R_{E1}}$$

where R_{E1} is the unbypassed portion of the R_E, otherwise

$$A_v = \frac{R_L'}{r_e}$$

$$R_B = R_2 \parallel R_3, \qquad R_{in} = R_B \parallel R_b, \qquad R_b = \beta(r_e + R_{E1}), \qquad R_o = R_C$$

$$A_i = \frac{i_o}{i_{in}} = A_{v(WL)}\frac{R_{in}}{R_L}$$

$$A_p = A_i \times A_{v(WL)}$$

$$v_{in} = v_s\frac{R_{in}}{R_s + R_{in}}$$

$$v_{o(WL)} = A_{v(WL)}v_{in}$$

8.7 ANALYSIS OF THE FET *CASCODE* AMPLIFIER

Similar to the BJT *cascode* amplifier, which is a cascade of common-emitter and common-base configurations, the FET *cascode* amplifier is a cascade of common-source and common-gate configuratios. Recall that the common-source amplifier can provide a very high input resistance, and the common-gate offers a much desirable high-frequency response, but it suffers from a very low input resistance. The FET *cascode* configuration utilizes the superior characteristics of both configurations, while avoiding their undesirable characteristics. The circuit of a JFET cascode amplifier is shown in Figure 8-41 below.

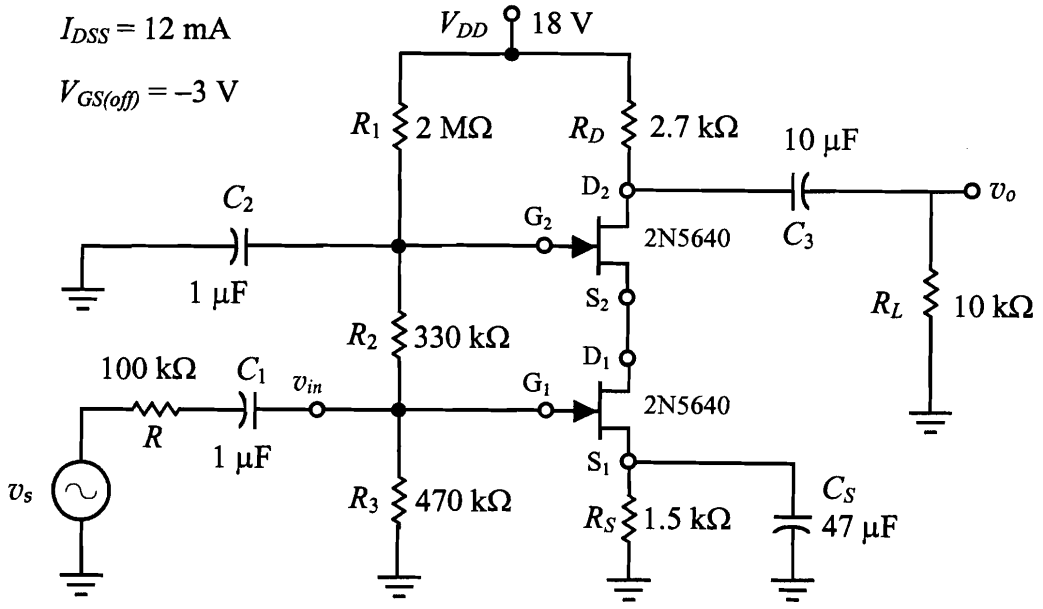

Figure 8-41: A JFET *cascode* amplifier circuit

DC analysis:

Applying the voltage divider rule at G_1, we can solve for the voltage V_{G1}, as follows:

$$V_{G1} = V_{DD}\frac{R_3}{R_1 + R_2 + R_3}$$

$$V_{G1} = 18\text{ V}\frac{470\text{ k}\Omega}{2\text{ M}\Omega + 330\text{ k}\Omega + 470\text{ k}\Omega} \cong 3\text{ V}$$

V_{GS1} is determined with Equation 7-32, as follows:

$$V_{GS}\Big|_{n-channel} = \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$

where,

$$a = \frac{I_{DSS}R_S}{V_P^2} \qquad a = \frac{12\text{ mA} \times 1.5\text{ k}\Omega}{(3\text{ V})^2} = 2 \qquad V_p = |V_{GS(off)}|$$

$$b = \frac{2I_{DSS}R_S}{|V_P|} + 1 \qquad b = \frac{2 \times 12\text{ mA} \times 1.5\text{ k}\Omega}{3\text{ V}} + 1 = 13$$

$$c = I_{DSS}R_S - |V_G| \qquad c = (12\text{ mA} \times 1.5\text{ k}\Omega) - 3 = 15$$

$$V_{GS1} = \frac{-13 + \sqrt{(13)^2 - 4 \times 2 \times 15}}{2 \times 2} \cong \mathbf{-1.5\text{ V}}$$

Having determined V_{GS}, I_D can be determined with Equations 7-15, as follows:

$$I_D = \frac{V_G - V_{GS}}{R_S} \qquad I_D = I_{D1} = I_{D2} = \frac{3\text{ V} + 1.5\text{ V}}{1.5\text{ k}\Omega} = 3\text{ mA}$$

$$g_m = \frac{2I_{DSS}}{|V_{GS(off)}|}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \qquad g_m = \frac{2 \times 12\text{ mA}}{3\text{ V}}\left(1 - \frac{1.5\text{ V}}{3\text{ V}}\right) = 4\text{ mA/V}$$

Applying the voltage divider rule at G_2, we can solve for the voltage V_{G2}, as follows:

$$V_{G2} = V_{DD}\frac{R_2 + R_3}{R_1 + R_2 + R_3}$$

$$V_{G2} = 18\text{ V}\frac{330\text{ k}\Omega + 470\text{ k}\Omega}{2\text{ M}\Omega + 330\text{ k}\Omega + 470\text{ k}\Omega} = 5.14\text{ V}$$

Both transistors being identical, and drain currents being equal, the gate-source voltages V_{GS1} and V_{GS2} must be equal. This can also be verified easily with Shockley's equation.

$$V_{GS1} = V_{GS2} = -1.5\text{ V}$$

$$V_{GS2} = V_{G2} - V_{S2} = -1.5\text{ V}$$

$$V_{S2} = V_{G2} + 1.5\text{ V}$$

$$V_{S2} = V_{D1} = 5.14\text{ V} + 1.5\text{ V} = 6.64\text{ V}$$

$$V_{S1} = I_D R_S = 3\text{ mA} \times 1.5\text{ k}\Omega = 4.5\text{ V}$$

$$V_{DS1} = V_{D1} - V_{S1} = 6.64\text{ V} - 4.5\text{ V} = 2.14\text{ V}$$

$$V_{D2} = V_{DD} - I_D R_D = 18\text{ V} - (3\text{ mA} \times 2.7\text{ k}\Omega) = 9.9\text{ V}$$

$$V_{DS2} = V_{D2} - V_{S2} = 9.9\text{ V} - 6.64\text{ V} = 3.26\text{ V}$$

Small-signal analysis:

The small-signal equivalent circuit of the cascode amplifier of Figure 8-41 is shown in Figure 8-42 below.

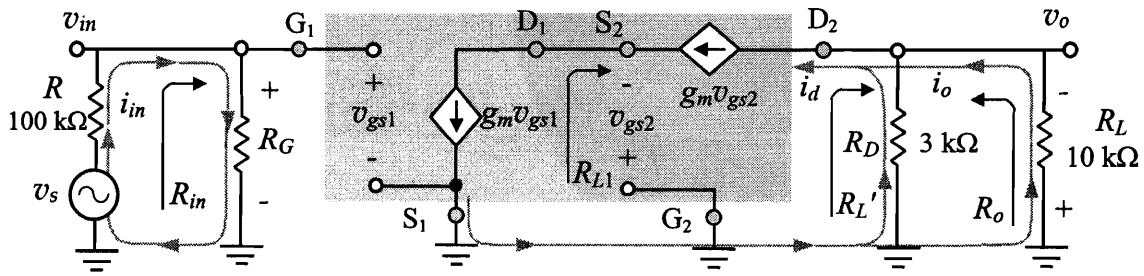

Figure 8-42: Small-signal equivalent circuit of Figure 8-41

Input resistance:

The input resistance R_{in} is the parallel combination of R_3 and R_2:

$R_{in} = R_G = R_3 \parallel R_2$ $\qquad R_{in} = 470\ \text{k}\Omega \parallel 330\ \text{k}\Omega = 194\ \textbf{k}\Omega$

Output resistance:

The output resistance R_o is simply R_D

$R_o = R_D$ $\qquad R_o = \textbf{2.7 k}\Omega$

First stage load resistance:

The load of the first stage (R_{L1}) is the input resistance (R_{in2}) of the second stage, which is a common-gate configuration, and its input resistance is simply given by

$R_{L1} = R_{in2} = r_m = 1/g_m = 1/\ 4\ \text{mA/V} = 250\ \text{A/V}$

Second stage load resistance:

$R_{L2} = R_L' = R_D \parallel R_L$ $\qquad R_L' = 2.7\ \text{k}\Omega \parallel 10\ \text{k}\Omega = 2.126\ \text{k}\Omega$

First stage voltage gain:

$$A_{v1} = \frac{v_{o1}}{v_{in}} = \frac{-g_m v_{gs} r_m}{v_{gs}} \qquad A_{v1} = \frac{v_{o1}}{v_{in}} = -g_m r_m \tag{8-63}$$

Second stage voltage gain:

$$A_{v2} = \frac{v_o}{v_{o1}} = \frac{-g_m v_{gs} R_L'}{-g_m v_{gs} r_m} \qquad A_{v2} = \frac{v_o}{v_{o1}} = \frac{R_L'}{r_m} \tag{8-64}$$

Overall voltage gain:

$$A_v = A_{v1} A_{v2} = -g_m r_m \frac{R_L'}{r_m} = -g_m R_L' \tag{8-65}$$

$$A_v = -g_m R_L' \tag{8-66}$$

$A_v = -g_m R_L' = -4\ \text{mA/V} \times 2.125\ \text{k}\Omega = -8.5$

Note that the effect of the transistor r_o was neglected in the process for two reasons: (1) to make the analysis simpler, (2) its effect is negligible with the cascode configuration. However, if r_o is to be accounted for, then R_o and R_L' would be as follows:

$$R_o = 2r_o \,||\, R_D \cong R_D$$

$$R_L' = 2r_o \,||\, R_D \,||\, R_L \cong R_D \,||\, R_L$$

Practice Problem 8-7 JFET Cascode ANALYSIS

Analyze the JFET *cascode* amplifier of Figure 8-43, and determine the following: V_{GS}, I_D, V_{DS1}, V_{DS2}, R_{in}, R_o, A_v.

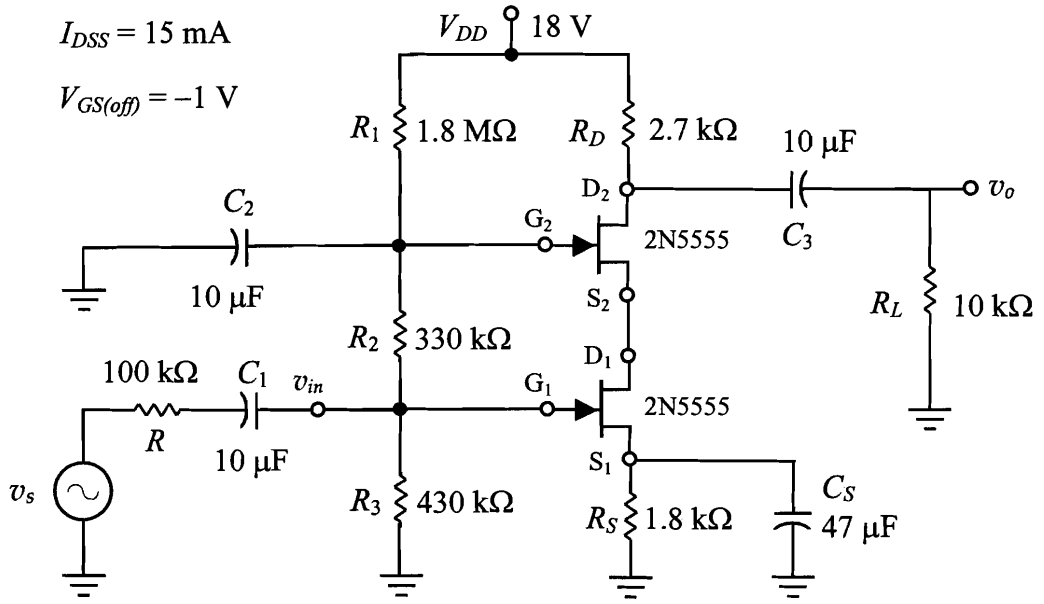

Figure 8-43: A JFET *cascode* amplifier circuit

Answers:

V_{GS} = −0.633 V, I_D = 2 mA, V_{DS1} = 2.37 V, V_{DS2} = 6.6 V, R_{in} = 187 kΩ, R_o = 2.7 kΩ, A_v = −23.37

8.8 DESIGN OF SMALL-SIGNAL JFET AND MOSFET AMPLIFIERS

Although the approach to designing the JFET or MOSFET amplifiers for a set of given specifications is somewhat different from that of the BJT amplifiers; however, the same basic design strategies apply equally to FET amplifiers. That is, we will first design the DC bias for an optimum and stable operating point that allows maximum signal swing at the output. In addition, we will employ a configuration that permits designing for a specific gain without significantly altering the established Q-point.

Example 8-5 n-channel JFET DESIGN

Let us design a common-source JFET amplifier for the following set of specifications:

Supply voltage: V_{DD} = 16 V
Drain current: I_{DQ} = 2 mA
No load voltage gain: $|A_{v(NL)}|$ = 26
Output voltage swing: $v_{o(max)} \geq$ 6 V(p-p)
Input Resistance $R_{in} \geq$ 330 kΩ
Output Resistance $R_o \leq$ 3.3 kΩ
Stability considerations: