

Dr. JKILL

Description

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*«..yes, I know that there are no sounds in Space.
And, now You can ask your questions.»*

G. Lucas, to journalists, about the “Star Wars, Episode I”»

Yes, I know that Robert Louis Stevenson wrote this name as “Jekyll”, but I write “JKILL” because it is “Jitter **KILL**er”, and is intended to eliminate this phenomenon in the digital audio signal.

Sometimes ago, I wrote a small article “Bits In Time” to describe in a simple words what is the jitter and how to do with it. You can find it at my web site.

As it was mentioned at the end of this article, most of the digital sources have audible jitter.

Bi phase coding and encoding, in the SPDIF/Toslink communication have a big influence to the sound quality. The jitter is affected by the clock signal at the receiver side, where the clock signal is reconstructed from the input signal by PLL method.

Transmitting the signal over synchronous I2S bus (it might be also LJ or RJ, but we will call everything “I2S”), without SPDIF/Toslink conversion; Nice to have, if the source can be clocked by the high quality (low jitter) oscillator, and the DAC is clocked by the same signal. But, do you know many signal sources at the market that can do this? And without a big hardware upgrade inside?

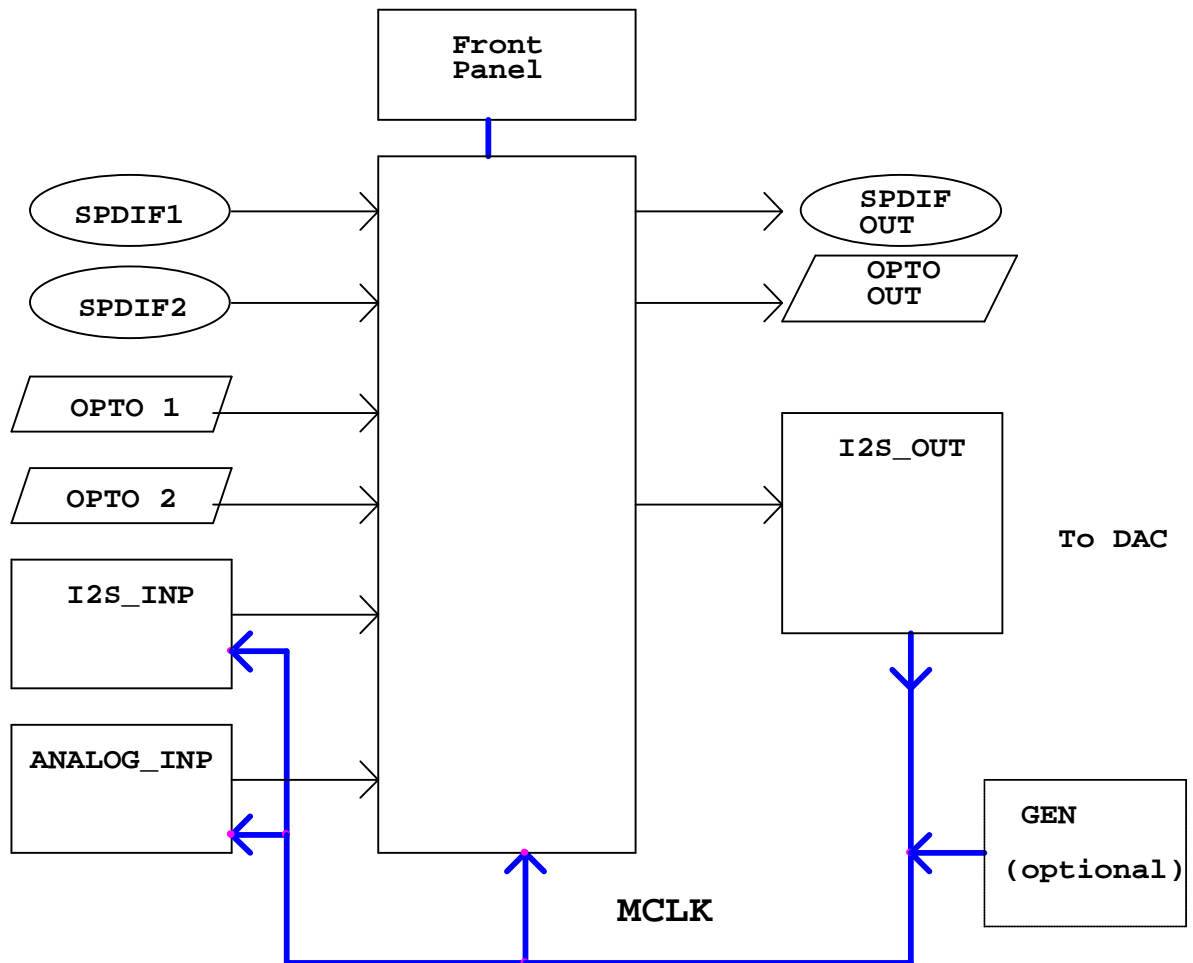
This device is intended to help the people, who want to use the conventional audio sources, like CD, DVD or media players, without any upgrades and penetration. The heart of the system is the FIFO buffer memory, working by the principle “Firs In, First Out”. Input signal (SPDIF, Toslink or I2S) comes to the buffer memory, clocked by the source’s oscillator (that has not good jitter performance), also ADC connection is implemented in the last version (for example – to get analog signal from turntable or tape). DSD receiving (as DoP) will be implement soon.

The output signal is the I2S bus, clocked from the low jitter oscillator, usually located close to the DAC. Because of this signal is clocking the DAC, it will determine the total sound quality, and this quality will not depends of the source oscillator.

So, the main user’s task is to find very good 2-frequencies clock oscillator and to use JKILL! (2 frequencies are for the 44.1/48kHz scale). There are also the place for additional SPDIF/Toslink outputs at the Main Board, if somebody wants to keep SPDIF/Toslink, but just to reduce the jitter..

The buffer is needed to compensate the source and DAC clock frequency differences.

JKILL's block diagram:



Front Panel – 3 pushbuttons or 1 encoder, plus small 1.8” TFT display to the user convenience. This unit can be simplified by using leds instead of TFT, to indicate the active input only. Also IR remote control receiver is located at the Front Panel. (This feature does not implement in the firmware, yet).

Main Board has USB-A connector, to firmware upgrade from the USB-Flash (Disc-On-Key). For easy device installation, the simple sound generator is implemented – which generates 1kHz triangle signal at the I2S Bus with 16/24/32bit resolution, 44.1-192kbit sample rate and various bus formats (I2S, LJ, RJ24, RJ16).

You even can check your source device “bit-perfect” with the great JKILL’s bit-perfect analyzer!

If bit-detector is turned on, JKILL automatically check the input signal resolution (16 or 24 bit), if the dithering is also turned on at the same time – it will be add to the 16-bit signal as eight additional low bits.

JKILL is able to switch ON/OFF the DAC or/and the amplifier power, JKILL can control the volume, with a help of 4-5-6 relays (16, 32 or 64 steps), which is so called “Nikitin Volume Control” (Alex Nikitin was a Lead R&D Engineer at Creek Audio, England).

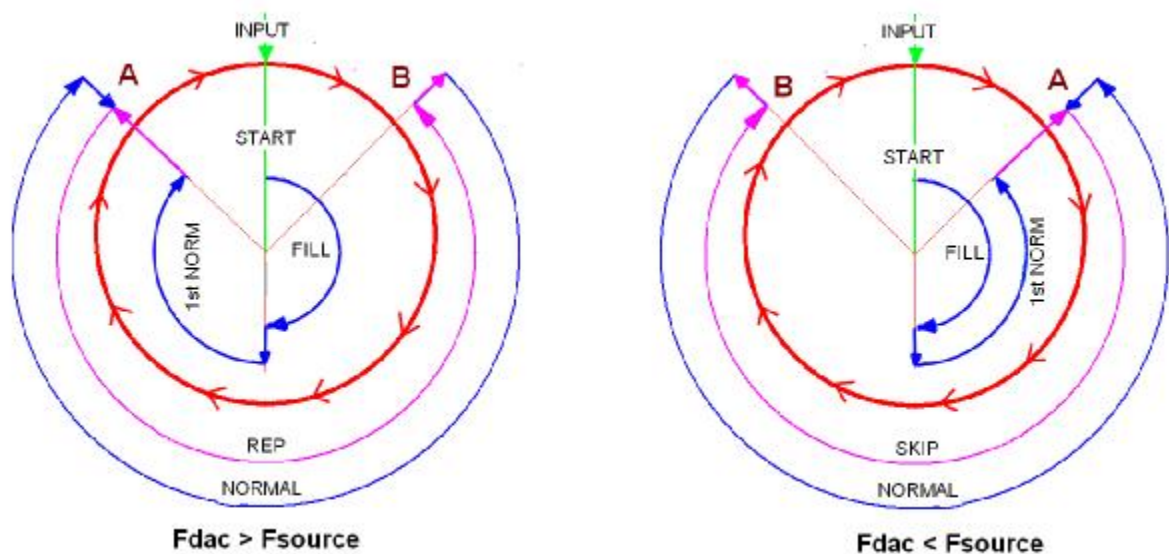
FIFO Operation

At the picture below you can see how FIFO buffer works.

Let imagine the buffer as the clockwise spinning ring (red). CPU writes the incoming data to the memory, always at the top (upper point). Reading the buffer occurs later – at the ring surface. If there is no signal at the input, device is at the idle state. The reading point is set at the half buffer length – at the bottom. The reading point is not moving, and the output signal is muting.

When the valid signal will be detected, CPU set the I2S bus according to the signal parameters (F_s) and passes to the “fill” state. There is a time delay, during which the half of the buffer is filling.

After the first incoming data has reach the bottom point, the output is unmuted and the “normal” mode began. Since this moment the sound starts.



If the incoming and outgoing sample rates will be exactly the same (on the MCLK level), writing and reading point will be unmoving, and the buffer makes a small time delay only.

But, in reality, they are always different, and the distance between the write and read points depends of this difference.

If the source clock frequency is lower then the DAC oscillator frequency (see the left picture), the reading point is moving forward, and reach the A point in time. Then the device starts to repeat some input data, to prevent the buffer overflow. The relative speed is negative, and the reading point moves backward, since it reaches the point B (“repeat” state). From this point the normal reading occurs, again up to the point A. CPU set the minimum relative speed, according to the frequency difference.

If the source frequency is higher then the DAC one (right picture), the reading point moves for the point A, then some data should be skipped during the reading (“Skip” mode), and the reading point moves forward, up to the point B. Then the normal reading starts again.

So, it is like a swing – :normal” mode turned to “repeat” or “skip” mode, then back to “normal” again. This is running on until the input signal is valid. When the signal become non valid, JKILL plays the rest of the buffer (“dry” state) and passes to the “idle” state.

The time, when device is at the normal state, depends of a frequency difference and the sample rate (higher Fs produce the lower time duration), and of course – of a buffer length.

We can claim than in “Normal” state there is total input jitter elimination, the output jitter depends only of the used DAC oscillator quality.

Skipping or repeating the data occurs with a very low frequency, combined with the special processing, and at the most cases are non audible. Even if that states are easy visible on a spectrum analyzer.

The experiments with the various audio sources, with the bit-perfect confirmed shows that there are no difference in the sound quality between the expensive CD/DVD players, media players, computer soundcards with SPDIF output, etc.

To minimize the time in skip/repeat states, the silence detector is implemented in software – every time the silence is detected, JKILL goes to the “dry” state and then to “idle”. If the signal appears again, all process starts from the beginning.

So, every silence (i.e. - between the tracks or disks) clears the reading pointer and increase the normal state time. Silence Detector threshold time can be adjusted in the device’s parameters.

All timings depends off the input signal sample rate (Fs), source and DAC oscillator frequencies, also of the buffer length. The table below shows the time delay (lag) and the minimum normal time for the some sample rates and the frequency differences. I should say, that only one or two times I have seen the frequency difference more then 200ppm.

Frq.diff,ppm	44		96		192	
	Lag, sec	1 st NORM,min	Lag, sec	1 st NORM,min	Lag, sec	1 st NORM,min
50	0.24	80.94	0.11	37.18	0.06	18.59
100	0.24	40.47	0.11	18.59	0.06	9.30
250	0.24	16.19	0.11	7.44	0.06	3.72
500	0.24	8.09	0.11	3.72	0.06	1.86
1000	0.24	4.05	0.11	1.86	0.06	0.93

Here:

- Frq.diff - source/DAC oscillator frequency difference, in parts per million (ppm).
- Lag – time of the first buffer filling, and the average delay between the input and output signals, n seconds.
- 1st NORM – minimum “normal” state time after the fill mode, in minutes.

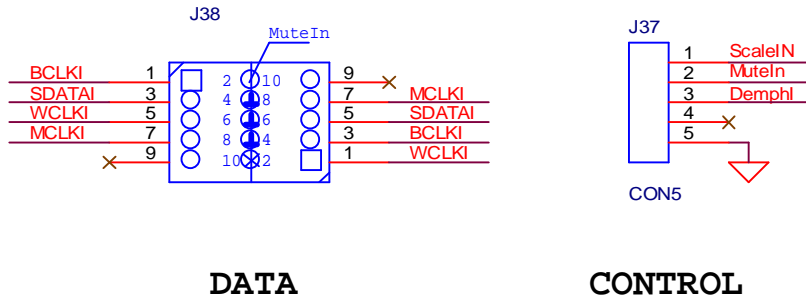
Notice, that after the “1st normal” it will be “skip” or “repeat” mode, and after that, the next “normal” mode will be twice of a “1st normal” time!

Even at the highest possible (for JKILL) sample rate as 192kbit, and oscillators frequency difference 50-100ppm, the 1st normal time is more then 9 minutes, that is usually more then the average track length. And with less then 500pm difference and CDDA format (44.1/16), normal state will continue 80 min, more then the regular (650Mb) Compact Disk!

So, most of the tracks will be played at “normal” state without the jitter, and without any data correction, keeping its bit-perfect condition.

Input signals and connectors.

- 1) 2xTOSLINK inputs at the Main Board.
- 2) 2xSPDIF input connectors (2 pin, connect the external BNC or RCA) – transformer isolated.
- 3) External ADC header.
- 4) I2S input data and control signals header– 15 pin “data” + 5 pin “control”.



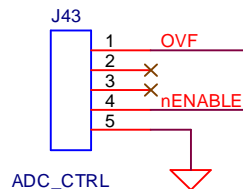
DATA

CONTROL

15 pin header is used to 10 pin flat, using one or another side. This was done for 2 special I2S sources devices, with the different pinouts. For other devices any side can be used.

Control signals are Mute, Demph, and the clock scale (44/48)

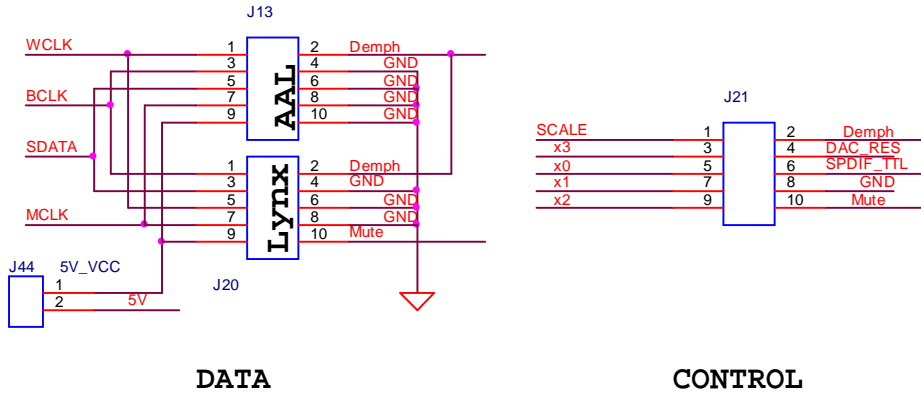
- 5) Optional ADC control header have two signals – ADC Enable and ADC Overload (OVF).



ADC Data comes from the ADC chip through the Z-state buffer, which is controlled by the enable signal directly to the DAC. JKILL’s outputs are at the Z-state in this mode. Only overload is indicated at the TFT Display.

Output signals and connectors.

- 1) Optional TOSLINK output, at the Main Board..
- 2) Optional SPDIF output header (2 pin), with transformer isolation.
- 3) I2S output – 2x 10-pin headers (2 different pinouts) for DATA. MCLK signal is input. It is possible to use 3.3 and 5v signals.
JKILL works by default with 512*Fs ((22/24MHz) and 1024*FS (45/49MHz) oscillators. Using of 768*Fs or 384*Fs (96kbit max.) is possible with the minor modification (user can order the JKILL with this modification ready).

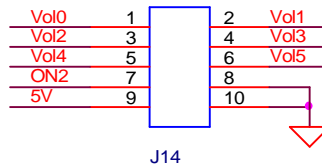


Control header consists of the Mute, Demph signals, the Scale signal to the DAC oscillator. Also the DAC Reset signal is present. 4 control signals are intended for the DAC control, X1X2 reflects the bus format (I2S, LJ, RJ24, RJ16), X3X4 controls the digital filter.

X1,X2,X3,X4 are user defined, for each sample rate (44/48/88/96/176/192) separately.

SPDIF_TTL output is present at the control header temporary, in the future PCB revision it may be avoided.

4) Volume control header:



Vol0-Vol5 – 6 bit parallel bus for the “nikitin volume control”.

ON2 – Power Amplifier ON.

, +5V – auxillary voltage, for optocouplers, for example.

Except the parallel relays control, some kind of a serial protocols are implemented (SPI, NEC, etc.).

Display and Control

Front Panel with 1.8” TFT Display, 3 pushbuttons or encoder, IR RC receiver.

Pushbutton functions::

SW1/or encoder press – inputs switch, power On/Off (long press).

SW3/encoder rotating clockwise - Volume “+”

SW4/encoder rotating counterclockwise - Volume “-“

SW3+SW4 – Utility Mode enter.

With encoder – after the long press (Off) will be small menu, where it is possible to enter the Utility Mode, Power Off (it will occur after 10s automatically), back to the working mode.

Utility Mode adopts Parameter Setup, Test Generator, Bit-Perfect Test, Firmware Upgrade.

If JKILL is used without the volume control, only one button is need for operation (input switch), encoder can be avoided.

Also 5 leds can be used for input indication, instead of TFT Display. But there will be a lack of the signal information, no Utility Mode (except the firmware upgrade).

Remote Control:

(this is not fully tested, so not present in the current firmware)

- IR RC, which you can adjust to the any remote control unit, working at one of the 6 standards -NEC, RC5, SIRC, SAMSUNG, JAP (Panasonic).
- External UART signal.

Indication:

1.8" TFT Display shows:

- the current active input
- current input signal sample rate,
- current input signal resolution (if bit detector is turned on),
- volume control position (if the volume control is used),
- signal level (VU-meter),
- FIFO state,
- input/output I2S bus format,
- resolution and silence detectors mode (on/of) and state, dithering enable and state.

The external display view depends of a "skin". This time only one skin is developed, with most test information. Graph skin is under development. User can draw it's own skin (request the requirements by E-Mail), send me this drawing and I will try to put it into the firmware.

Bit Perfect Test

You can select this mode from the Utility Menu.

You need the special data file, that you sound source should play. This file should consists of the constant value. Examples will be downloadable soon.

Received data are indicates at the screen in various forms with 1s test period.

You can see if there is a bit perfect or no, if no – which bits are corrupted.

Some sources add dithering and corrupt only 1-2 LSB.

Attention: select the necessary input before entering this mode..

Firmware and parameters.

All device parameters can be adjusted in 2 ways – through the screen menu, or with the special PC program.

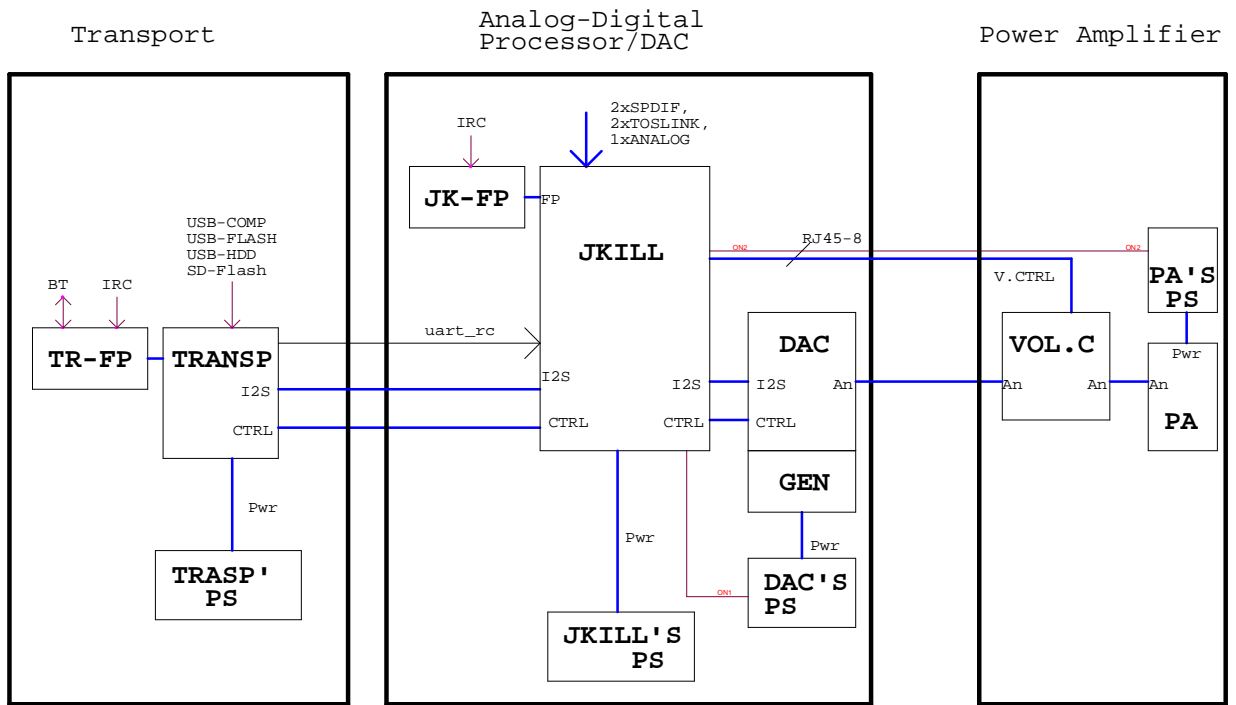
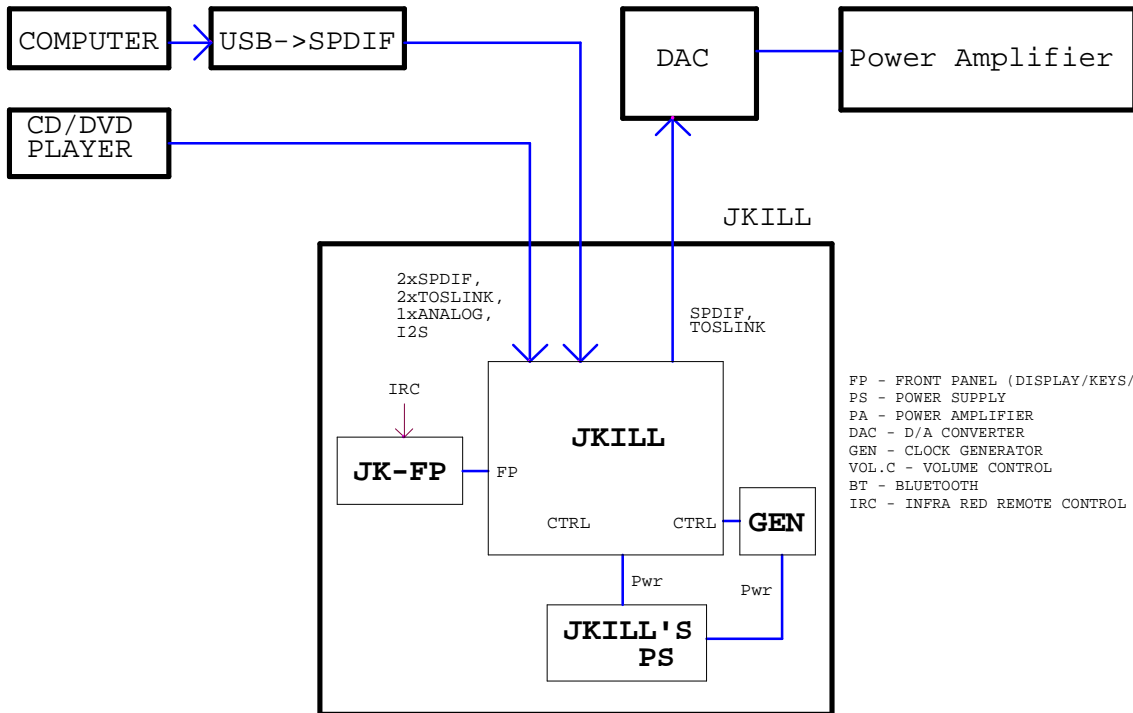
Go from Utility Mode to the Firmware Upgrade, put a USB-Flash to the USB connector and follow the instructions at the screen. JKILL will restart in a boot loader mode.

If USB-Flash have firmware upgrade file or/and parameters file – they will be used for upgrade. Power restart is need after upgrade.

There is an unconditional entering to the boot loader: power up JKILL with the volume control header pin 1-2 shorted. (Don't forget to power off JKILL before!)

Some JKILL applications:

JKILL can be used as the stand alone device, as a DAC input selector, also as the advanced digital "pre-amplifier". Below you can find some application schematics.



FP - FRONT PANEL (DISPLAY/KEYS/ENCODER)
PS - POWER SUPPLY
PA - POWER AMPLIFIER
DAC - D/A CONVERTER
GEN - CLOCK GENERATOR
VOL.C - VOLUME CONTROL
BT - BLUETOOTH
IRC - INFRA RED REMOTE CONTROL

Technical Parameters:

Sample Rates: 44.1, 48, 88.2, 96, 176.4, 192 kbit/s
Resolution: 16, 24 bit for SPDIF/Toslink inputs, 32bit for I2S input
Output bus formats: I2S, LJ, RJ24, RJ16, DSD.
Input MCLK: 512*Fs or 1024*Fs, 3.3v or 5v.
768*Fs (by the special request)
384*Fs (by the special request, the highest sample rate is limited to 96)

Power Consumption: 7.5-9VDC, 0.3A max

Good Luck!