# Digital audio generator signals
# JK-GEN 384-12

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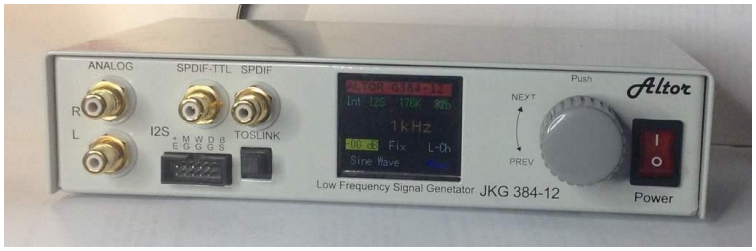


This device is intended for R&D process, testing, debugging and repairing of the modern audio systems.

JK-GEN generates 11 different waveforms, using Digital Direct Synthesis (DDS), with sampling rates up to 384kHz, bit depth to 32-bit, in digital and analog form, to supply the equipment under the test.
A main feature of this device is that it is able to generate the signals in digital form (I2S, SPDIF, TOSLINK), usually not presented in the conventional signal generators.

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# 1. Introduction.

The most significant element of the modern audio equipment is DAC (Digital-to-Analog Converter). Usually, Audio DAC chip has I2S bus input, which technically is a kind of the synchronous serial interface (SPI). In this case the name of "I2S" refers only to the sense of the incoming data signal (SDATA), bit (BCLK) and channel synchronization (WCLK or LRCLK, which are the same) and general synchronization (MCLK). Physically, the signals may be TTL / CMOS, PECL, LVDS, RS-485, etc., and a logical protocol can be Philips-I2S, Left Justify (LJ), Right Justify with a different digit (RJ 24, RJ 16), DSP, TDMCA, etc.
Input of the whole device "DAC" (not chip itself) can be SPDIF / TOSLINK (optical or coaxial serial bit-phase) or I2S. In general, “DAC" as device is usually consists of SPDIF / TOSLINK - receiver (SPDIF/TOSLINK to I2S converter) and DAC-chip, with optional digital filter and reclock circuit between.

In the development, debugging, validation or repairing of the DACs, you should provide the necessary input signal. Usually this is done by using CD/DVD player - for delivering SPDIF/TOSLINK, using the disc with the relevant test signals tracks, or computer with a sound card with these outputs.
A lot of people use simple USB audio Interfaces (PCM 27 xx, PCM 29, xx), some of which are except SPDIF have I2S output, and allow you to work directly with the DAC itself, bypassing the receiver.
These simple interfaces can work at 48/16 format, for the higher resolution formats it is necessary to use more advanced USB device - Amanero, EDEL, Flamenco, Bolero, etc. Such interfaces with computer have the great flexibility to generate different test signals.

Testing analog circuits is generally provided by feeding them with the analog input test signals of different shapes. That signals may also be obtained using computer (with either internal or external sound card).

JK - GEN 384 -12 is designed for the same purpose, but unlike a computer – it is compact, stand alone (and possibly battery powered - device consumes only a few watts.). There are also some advantages in operation (switching bus frequency, bus format and other parameters are much faster than in the case of computer interfaces, in which some things are generally difficult or impossible to change, i.e. - this device is more flexible and friendly.

# 2. Basic signals, operation modes, technical characteristics.

## *2.1 Output Signals.*

- Buffered I 2 S (SDATA, BCLK, WCLK, MCLK), 3.3V CMOS;
- Output Bus Formats: I2S, LJ, RJ24, RJ16 *;
- Output Bus transmitted data: 16, 24, 32 bits;
- Output Bus Sample Rate (Fs): 44.1, 48, 88.2, 96, 176.4, 192, 352 ** 384 ** kHz
- Optical TOSLINK interface;
- Coaxial SPDIF output
- SPDIF_ CMOS output
- Analog stereo output from the internal DAC.

* - Generation of an analog signal is produced only when the bus is set to I2S or LJ.
** - Bus frequency 352kHz 384kHz are complementary, correct generation of analog signals, as well as the integrity of the transmitted signals on a digital bus is provided, but not guaranteed. The main purpose of these frequencies - verification of the signal pass.

## *2.2. Output Connectors.*

- RCA - to connect coaxial cable with SPDIF signal;
- RCA - to connect coaxial cable with SPDIF_CMOS signal;
- TOTX - for the fiber optic cable, the signal TOSLINK;
- IDC 10 – output I2S Bus signals, external oscillator management;
- 2 xRCA - analog output signal.

## *2.3. Signals shapes.*

Group I: Sine, Sine 200ms bursts, triangle wave, saw wave, square wave.
Group II: Sweep Frequency Sine, dual tone (IMD) Sine, White Noise, Pink Noise, Constant Value, Digital Zero.

When using triangle, saw and square wave analog signals it is recommended to set the sampling rate at 352 or 384 kHz – to avoid artefacts, associated with the DAC's digital filter operation.

## *2.4. Signals frequency.*

Group I signals: a series of fixed frequency of 0.1, 1, 5, 10, 20, 50, 100, 200, 500, 1000 Hz, 5, 10, 15, 20, 30, 40, 50, 60 kHz, also smooth change (bit by bit) rate to 0.1 to 99999.9Hz.
If the desired generated frequency >Fs/2 (Kotelnikov/Nyquist frequency violation), the frequency is displayed in red;
For Sweep Frequency Sine Wave the starting and finishing frequency are set from the fixed values (see above). Frequency step - 1/24 octave, each step duration - 20ms, the time between packets - 200ms.
For a "Constant Value" it is possible change every bit, by adjusting each digit (4 bits of the 32 total), the default number is transmitted 0xA1B2C3D4.

"Dual tone" signal is to check IMD, and has three modes:
- 60/7000 Hz with amplitudes ratio 4:1,
- 250/8020 Hz, ratio is 4:1,
- 6000/7000 HZ, ratio is 1:1,
- 19000/20000 Hz, ratio is 1:1.

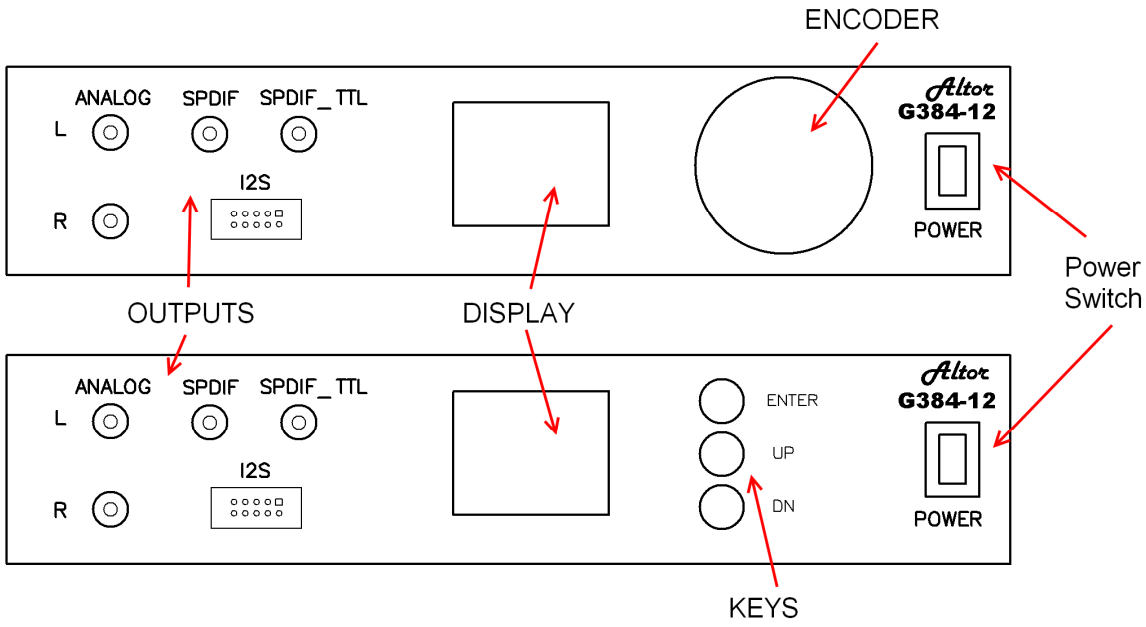
### *2.5. Signals amplitude.*

- Output digital signals: 3 V CMOS;
- Analog output: 1.7Vrms (TBD);
- Digital amplitude adjustment from 0 to -60 dB in 1 dB steps;
- Control Stereo: left + right (L + R), only the left (L), only the right (R), both off (Mute – digital zero is transmitting at both channels).

* To test the analog devices where ultralow THD value is necessary, you can use an external high-quality audio DAC connected to the digital outputs, or use a band pass filter at a given frequency, to reduce harmonics generated by the device's own analog signal.

## 3. User interface.

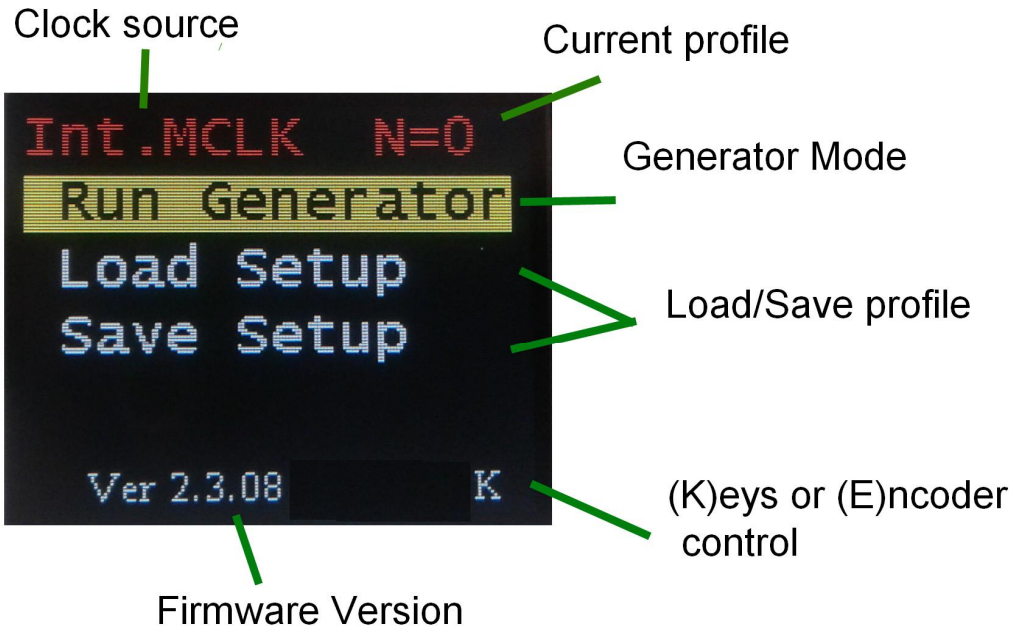
### *3.1 Front Panel.*



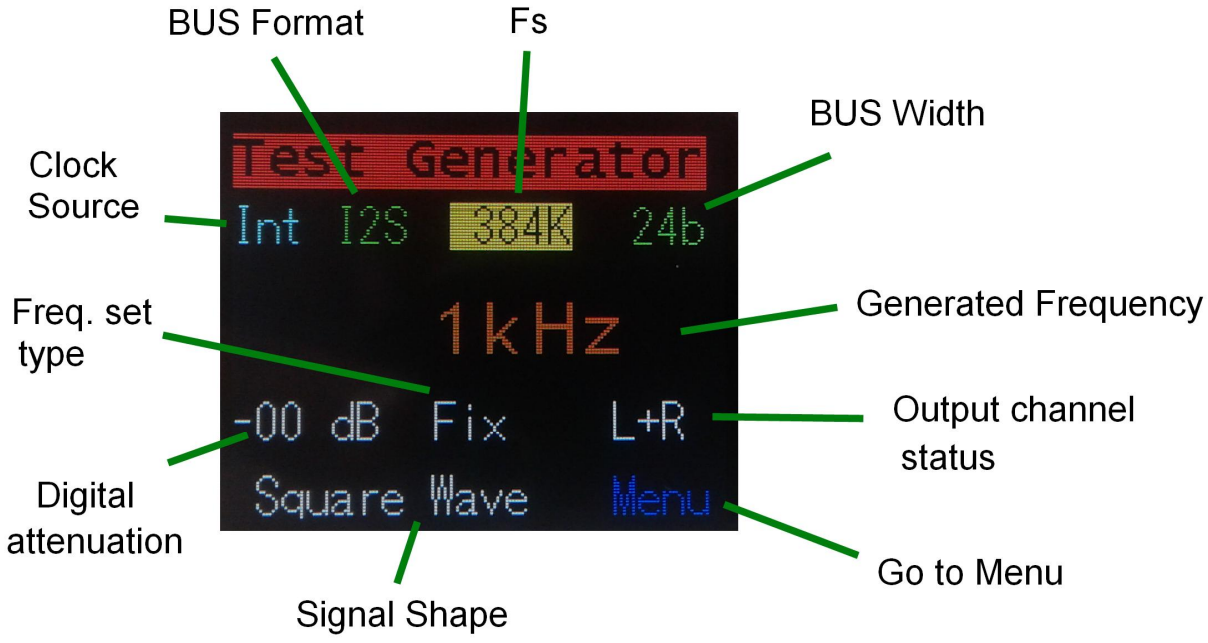

- 3 push buttons or one encoder (depend of a model) control;
- encoder rotation – select parameter, encoder push – change parameter;
- in case of pushbuttons control – two buttons for selection (up/down) and one for change.
- indication: 1.8” color TFT display;
- firmware upgrade from USB Flash (DiscOnKey) connector at the back panel;
- up to 8 user’s setups are stored in the internal flash memory;

### *3.2 Display.*

Menu:




Operating device screen:




Note: display view can have some differences in the future firmware versions.

# 4. Additional functions and parameters.

## *4.1 Clock.*

- Internal clock from the built-in dual-frequency generator, frequency (MCLK) 22.5792/24.576 MHz (512 Fs),
- External clock (when applying 3-5V input to "EXT" signal MCLK output switches to the bus input) of 512*Fs or 1024*Fs
- To control the external generator (switch the frequency) it is issued the signal "Scale"), with automatic polarity.

## *4.2 User's Setups*

The device has 8 different configurations (setups or profiles):
Configuration 0 - is factory default, cannot be overwritten after the manual changes.
Configuration 1-7: Anytime can be stored in non-volatile memory, and used later.

## *4.3 Power.*

Depending on the version, the device can be powered by:
- AC 100-240 V 50/60Hz from external adapter
- DC 7.5-9V,

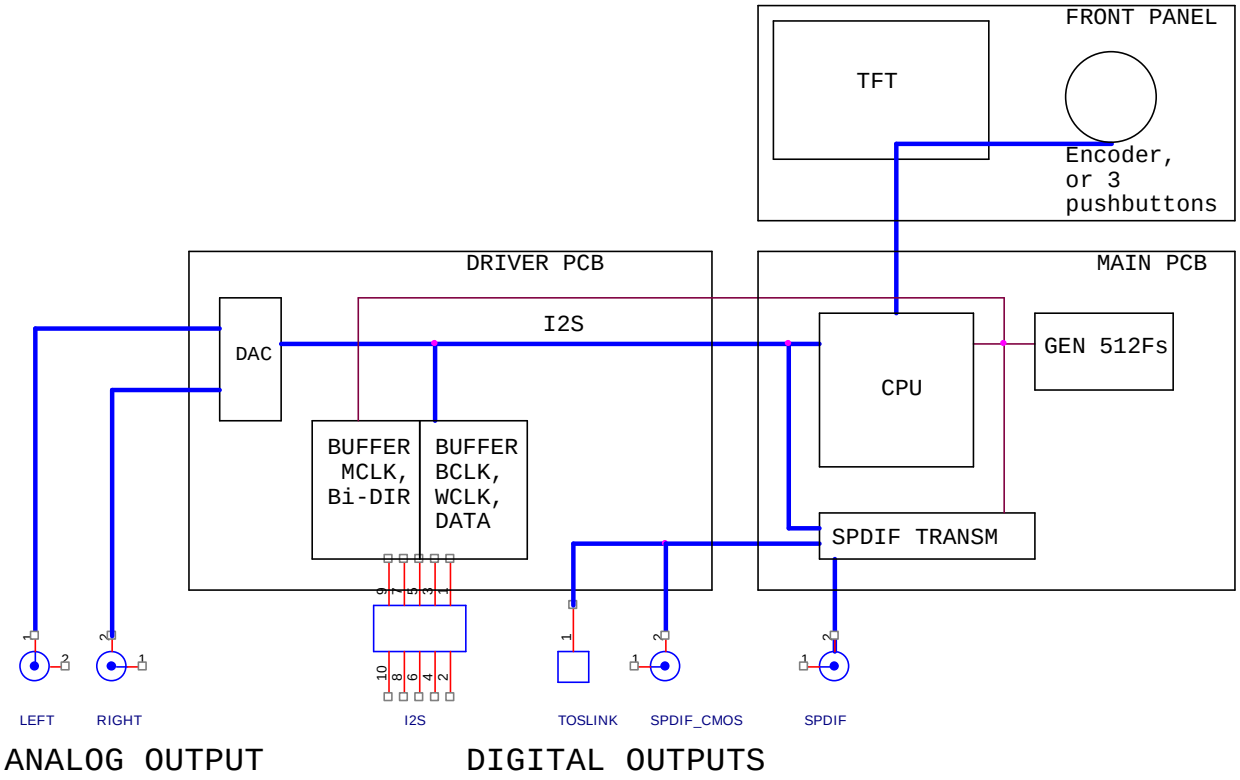
Power Consumption: 2.5W (when using DC voltage 7.5V, the internal clock, without additional devices *).

* Additional external signal devices can be used to provide the galvanic isolation, and/or to convert the bus signals to RS-485 CMOS, LVDS, LVPECL, etc.

## *4.4 Product Variants.*

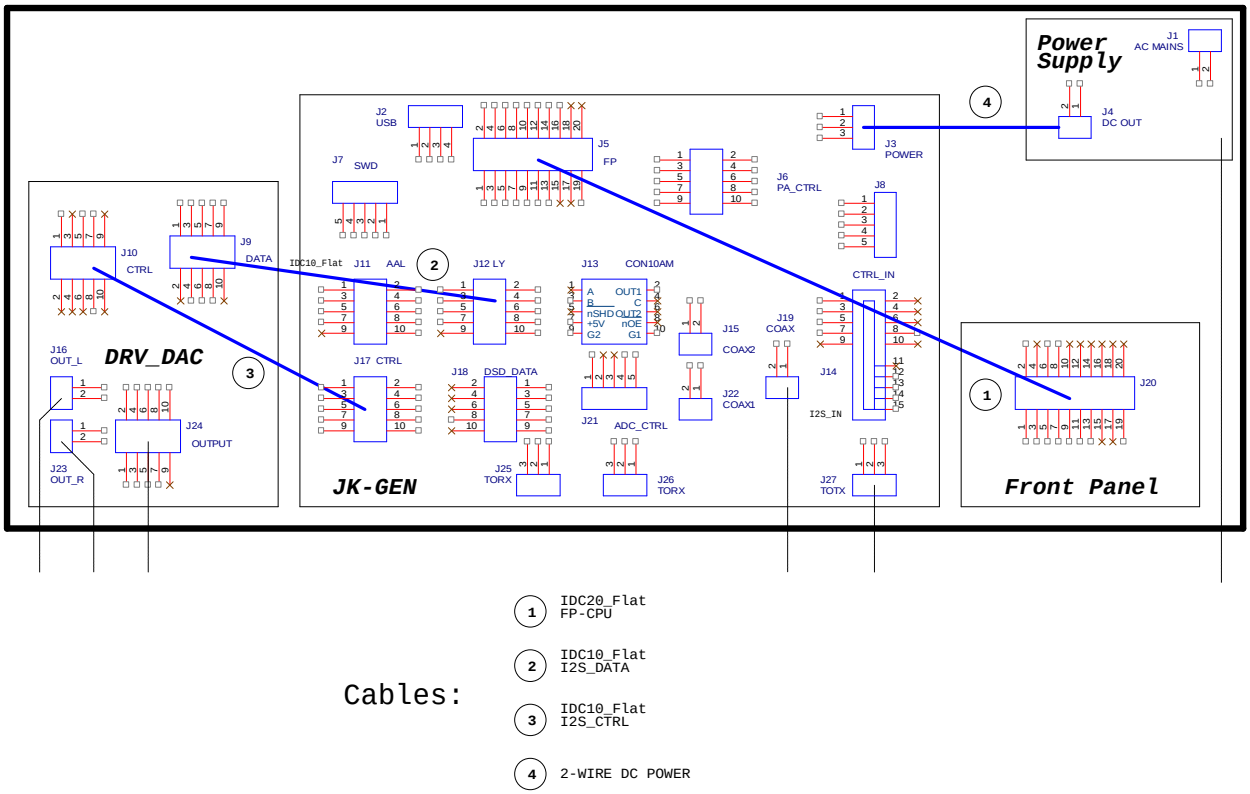
Depending on the model, there may be 5 variants of the product:
1) Completed device with or without the external power supply (wall adapter).
3) OEM-set: a set of fully assembled boards (CPU board, clock module, output board, front panel board with encoder or pushbuttons)
4) DIY - Kit - CPU board with firmwared CPU installed with their environment, empty output PCB, empty front panel.
5) Total DIY Kit – 4 bare PCB (CPU, output and front panel boards) and non assembled CPU with boot loader firmware.
By special agreement, additional components can be included at variants 4 and 5 (other chips, display, etc.) for additional price.

## 5. Block Diagram:




The device consists of a microprocessor control with TFT display and input buttons (or encoder). Clock performed by internal or external dual-frequency oscillator.
CPU's I2S bus signals are connected with SPDIF – transmitter, internal digital-to-analog converter (DAC), and to I2S output device through the buffer, as well.

# 6. Modules Wiring Diagram:




Cables:

1. IDC20_Flat FP-CPU
2. IDC10_Flat I2S_DATA
3. IDC10_Flat I2S_CTRL
4. 2-WIRE DC POWER

Structurally, the device consists of 3 parts: CPU board, Buffer board with DAC, and the front panel. The internal oscillator is a module that is installed into the connector on the CPU board. Front panel and CPU board are connected with 20-wire ribbon cable (1).
Buffer board with DAC is connected to the CPU board with two 10 - wire flat cables (2 and 3). Separate, cables connects the output RCA connectors with the buffer board (Left, Right analog outputs, SPDIF-CMOS) and CPU board (SPDIF)

Power inlet is connected to CPU board throw the power switch.

# 7. Firmware Upgrade.

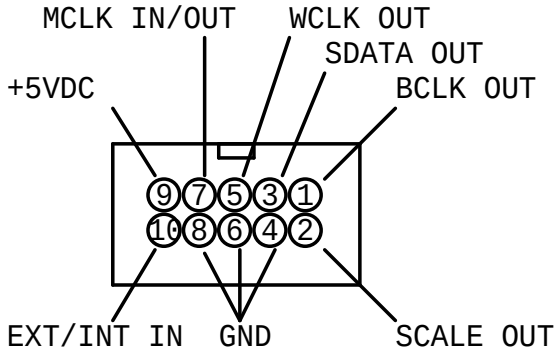
To eliminate the errors found in the work, as well as for the further development and improvement of the device, a firmware upgrade is provided.
Using the internal boot loader by the following procedure:
- Switch off your device
- Turn the device while pressing the pushbutton at the device's back pane (after entering the boot mode, you can release the button)
- Insert the USB plug the flash drive (DiscOnKey), with new firmware file. The update process will be displayed on the screen. Upon detection of the correct firmware file will be given a 10-second countdown. If for some reason you change your mind to update the firmware - just turn off the power or remove the USB DOK.
- After the upgrade - switch off the device, remove the USB flash, and turn on the device.

# 8. Appendix.

## *8.1 Output connectors pinout*

Output analog and SPDIF connectors - such as RCA, the central wire is signal.

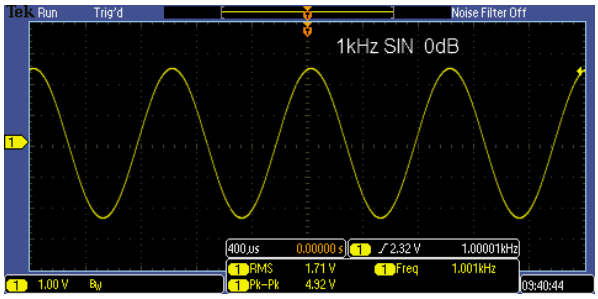
Digital I2S output - IDC 10 connector with the following signals:

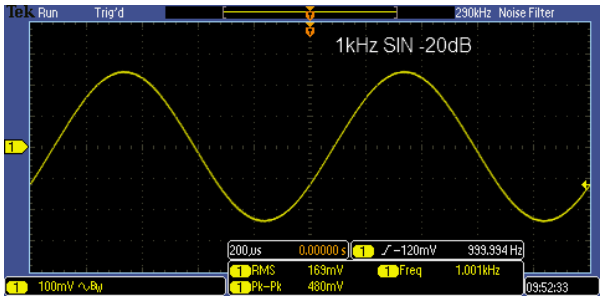


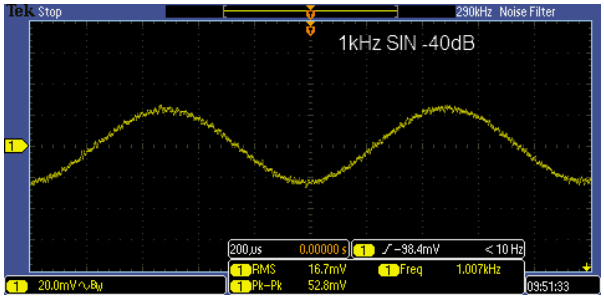

+5V signal EXT / INT connects your device to the external oscillator. For this purpose, you can use the output of +5 VDC.
Also +5VDC output can be used to power additional devices (I2S isolators, etc.). Up to 100mA.
Signal “Scale” (3 V CMOS) toggles the clock frequency generator (44/48), required signal polarity is determined automatically.

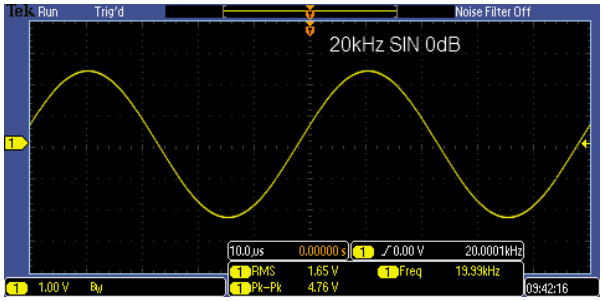
## *8.2 Signal Shapes (scope screen shots).*

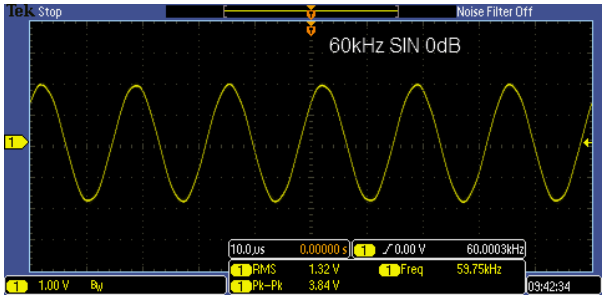
Analog output signals:

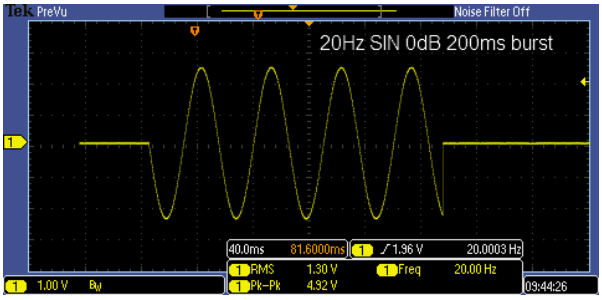


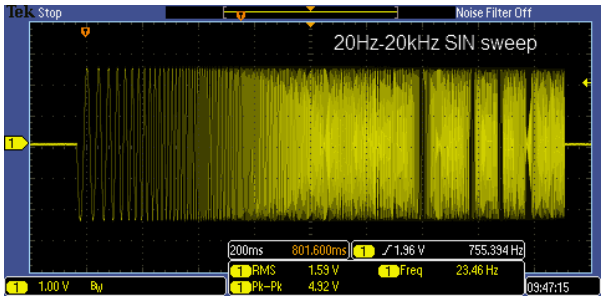



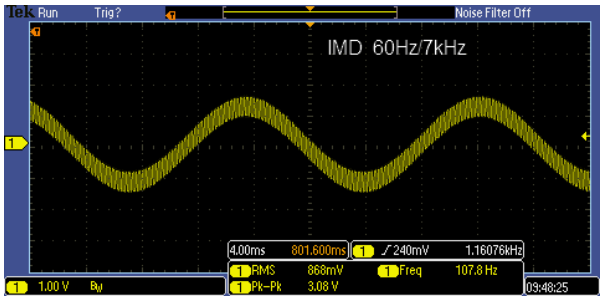



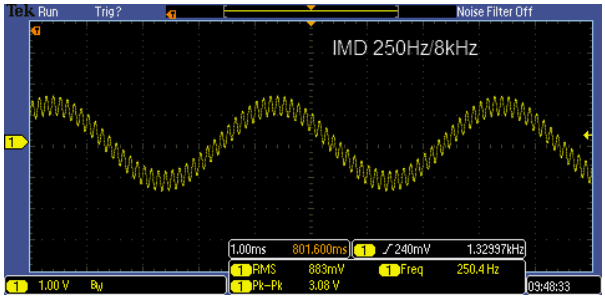



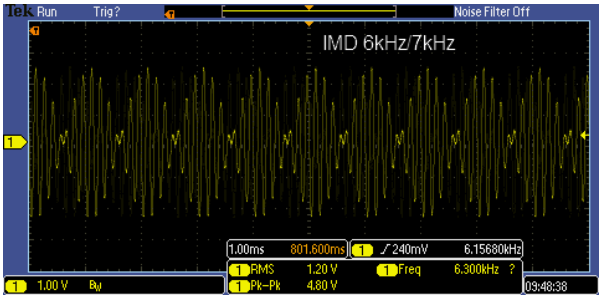



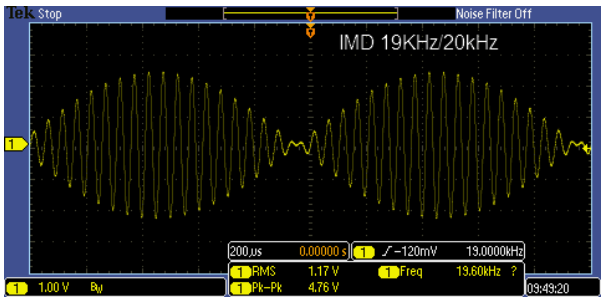



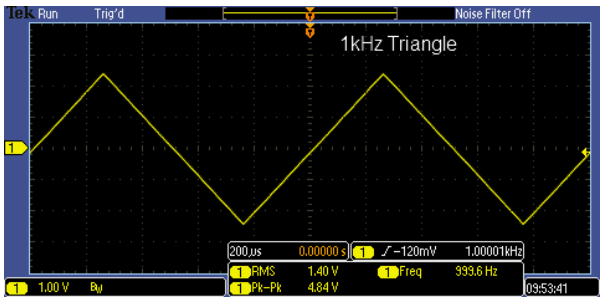



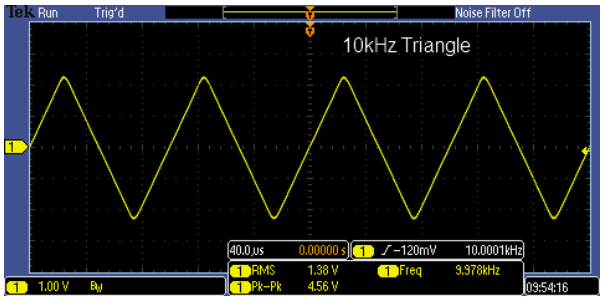



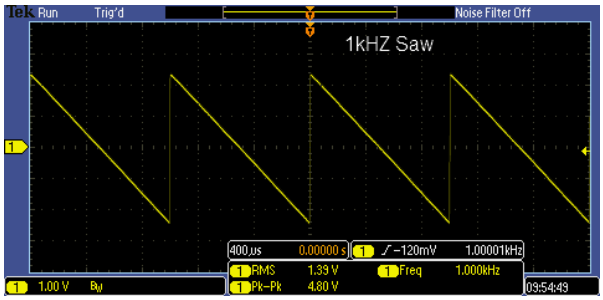



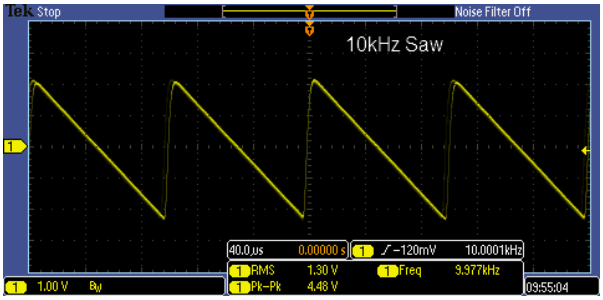



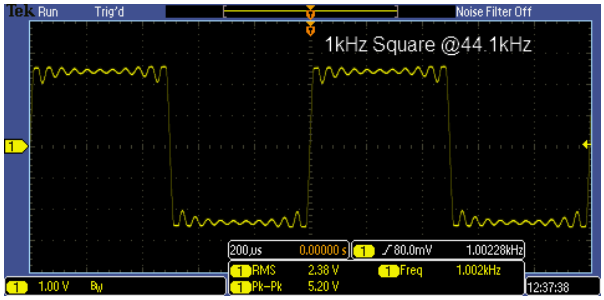

Tek Stop
Noise Filter Off
IMD 19KHz/20kHz
200 µs 0.00000 s
−120mV 19.0000kHz
RMS 1.17 V
Freq 19.60kHz
Pk-Pk 4.76 V
1.00 V
09:49:20

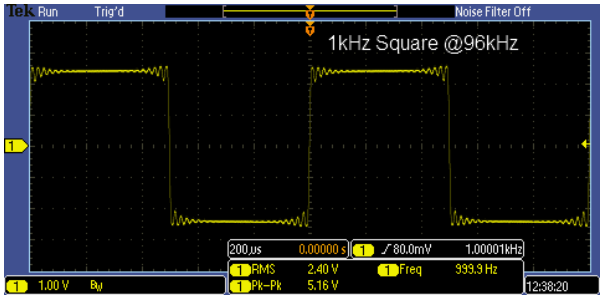

Tek Run Trig'd
Noise Filter Off
1kHz Triangle
200 µs 0.00000 s
−120mV 1.00001kHz
RMS 1.40 V
Freq 999.6 Hz
Pk-Pk 4.84 V
1.00 V
09:53:41

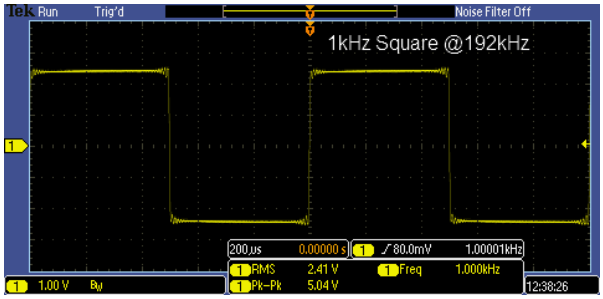

Tek Run Trig'd
Noise Filter Off
10kHz Triangle
40.0 µs 0.00000 s
−120mV 10.0001kHz
RMS 1.38 V
Freq 9.378kHz
Pk-Pk 4.56 V
1.00 V
09:54:16

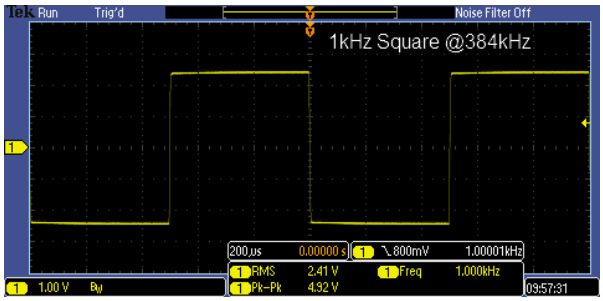

Tek Run Trig'd
Noise Filter Off
1kHZ Saw
400 µs 0.00000 s
−120mV 1.00001kHz
RMS 1.39 V
Freq 1.000kHz
Pk-Pk 4.80 V
1.00 V
09:54:49

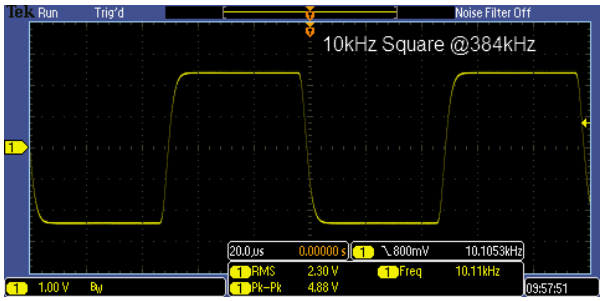

Tek Stop
Noise Filter Off
10kHz Saw
40.0 µs 0.00000 s
−120mV 10.0001kHz
RMS 1.30 V
Freq 9.377kHz
Pk-Pk 4.48 V
1.00 V
09:55:04

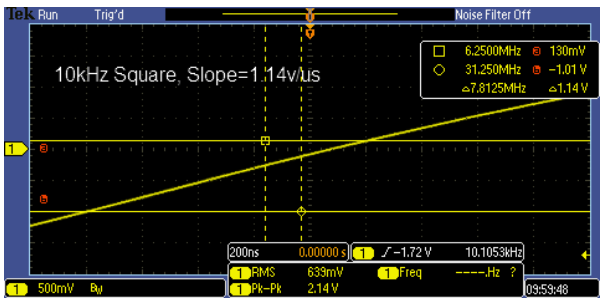

Tek Run Trig'd
Noise Filter Off
1kHz Square @44.1kHz
200 µs 0.00000 s
80.0mV 1.00228kHz
RMS 2.38 V
Freq 1.002kHz
Pk-Pk 5.20 V
1.00 V
12:37:38

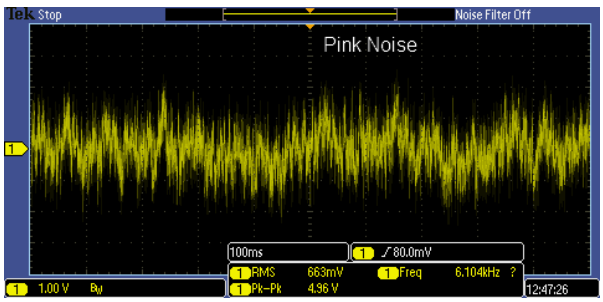

Tek Run Trig'd
Noise Filter Off
1kHz Square @96kHz
200 µs 0.00000 s
80.0mV 1.00001kHz
RMS 2.40 V
Freq 999.9 Hz
Pk-Pk 5.16 V
1.00 V
12:38:20


Tek Run Trig'd
Noise Filter Off
1kHz Square @192kHz
200 µs 0.00000 s
80.0mV 1.00001kHz
RMS 2.41 V
Freq 1.000kHz
Pk-Pk 5.04 V
1.00 V
12:38:26


Tek Run Trig'd
Noise Filter Off
1kHz Square @384kHz
200 µs 0.00000 s
800mV 1.00001kHz
RMS 2.41 V
Freq 1.000kHz
Pk-Pk 4.92 V
1.00 V
09:57:31


Tek Run Trig'd
Noise Filter Off
10kHz Square @384kHz
20.0 µs 0.00000 s
800mV 10.1053kHz
RMS 2.30 V
Freq 10.11kHz
Pk-Pk 4.88 V
1.00 V
09:57:51

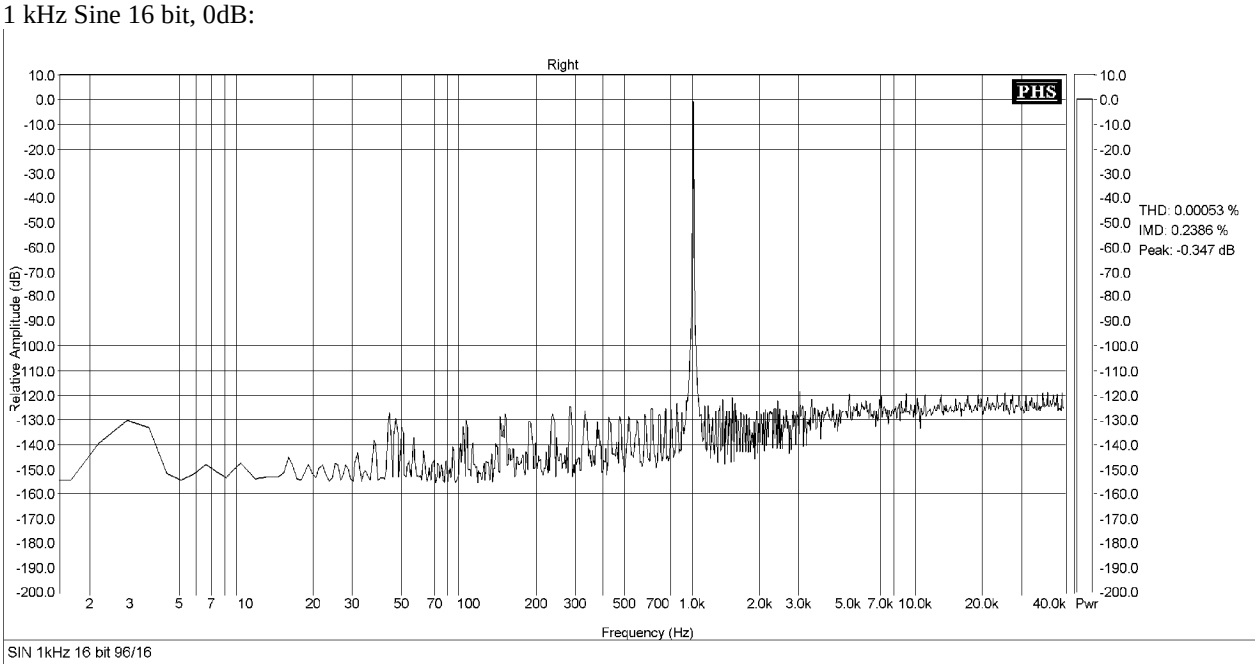

Tek Run Trig'd
Noise Filter Off
10kHz Square, Slope=1.14v/us
6.2500MHz 130mV
31.250MHz −1.01 V
Δ7.8125MHz Δ1.14 V
200ns 0.00000 s
−1.72 V 10.1053kHz
RMS 639mV
Freq ----.Hz
Pk-Pk 2.14 V
500mV
09:59:48


Tek Stop
Noise Filter Off
Pink Noise
100ms
80.0mV
RMS 663mV
Freq 6.104kHz
Pk-Pk 4.96 V
1.00 V
12:47:26

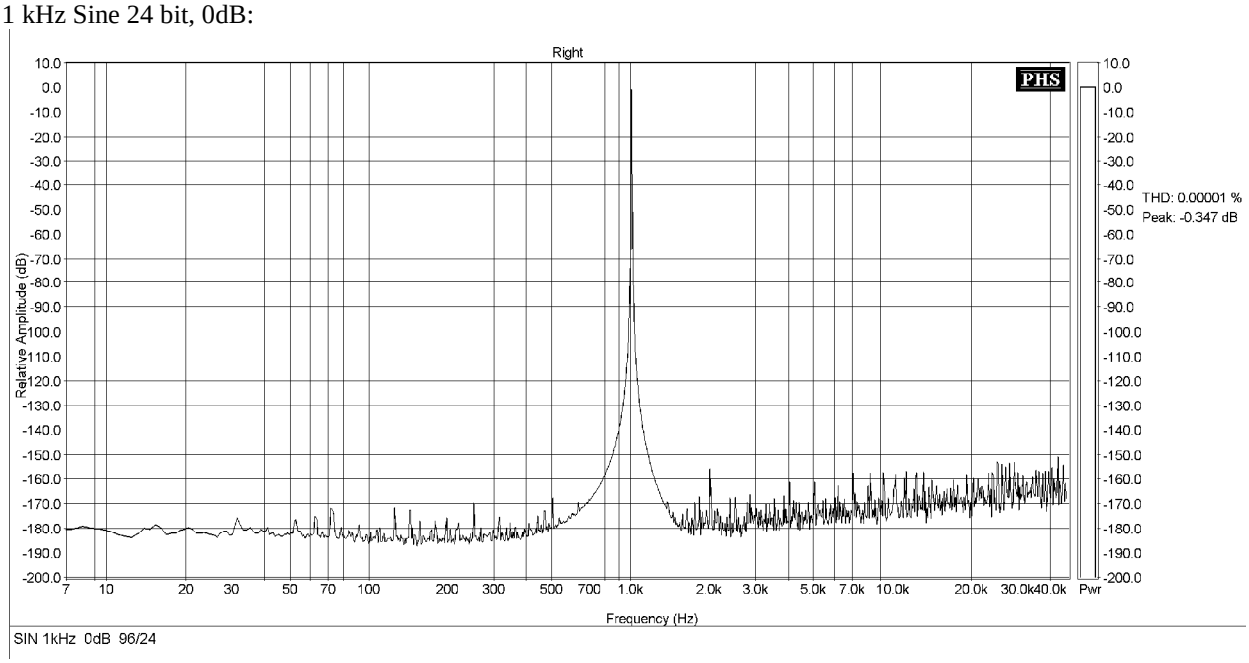
## *8.3 Signals Spectrum.*

Synthesized signals at digital outputs spectrum:
As PC input it was used USB-interface “Flamenco-Light” with I2S 96/24 input.

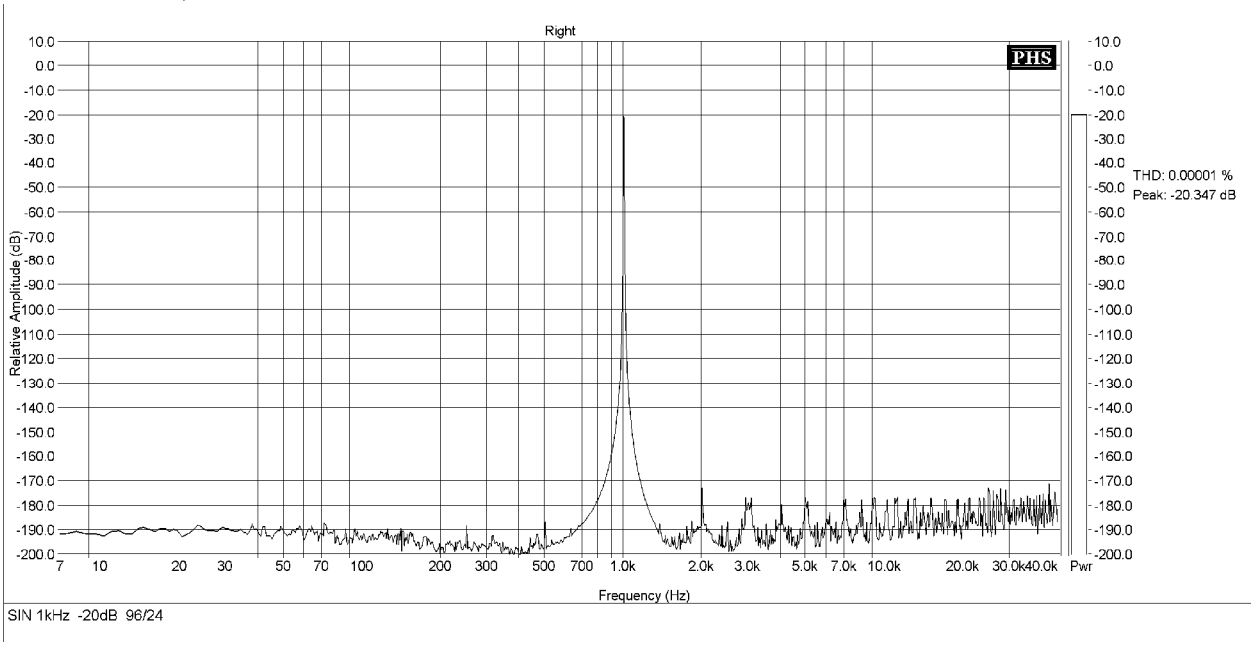
1 kHz Sine 16 bit, 0dB:



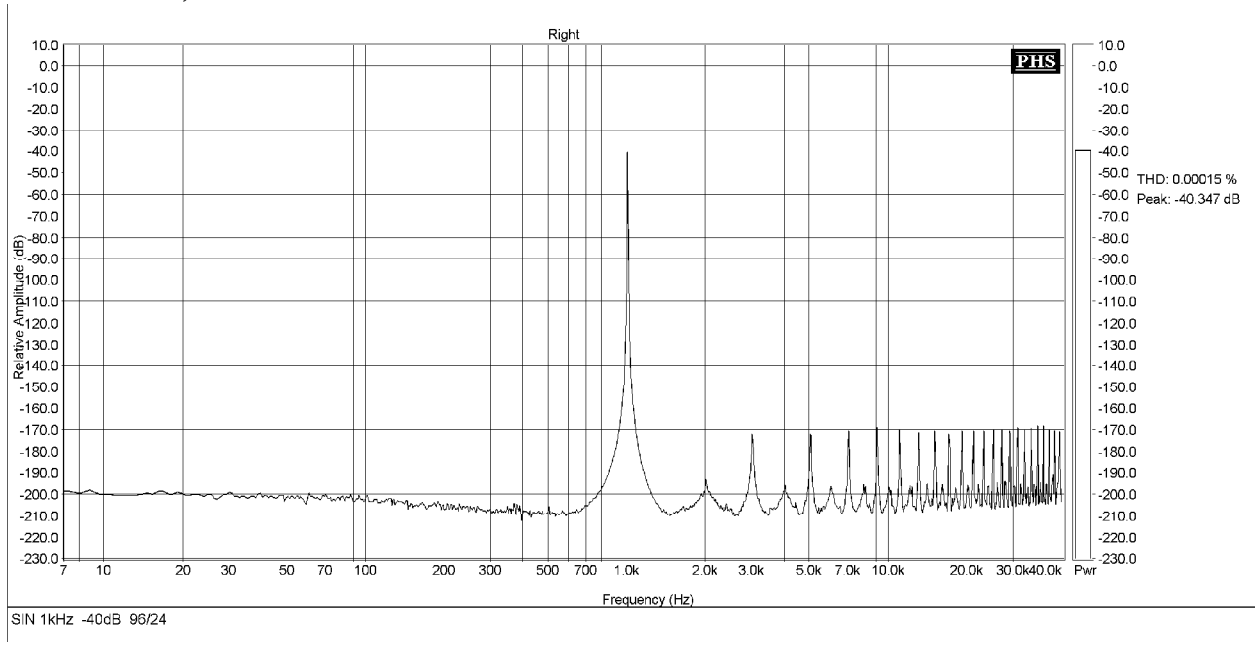

1 kHz Sine 24 bit, 0dB:



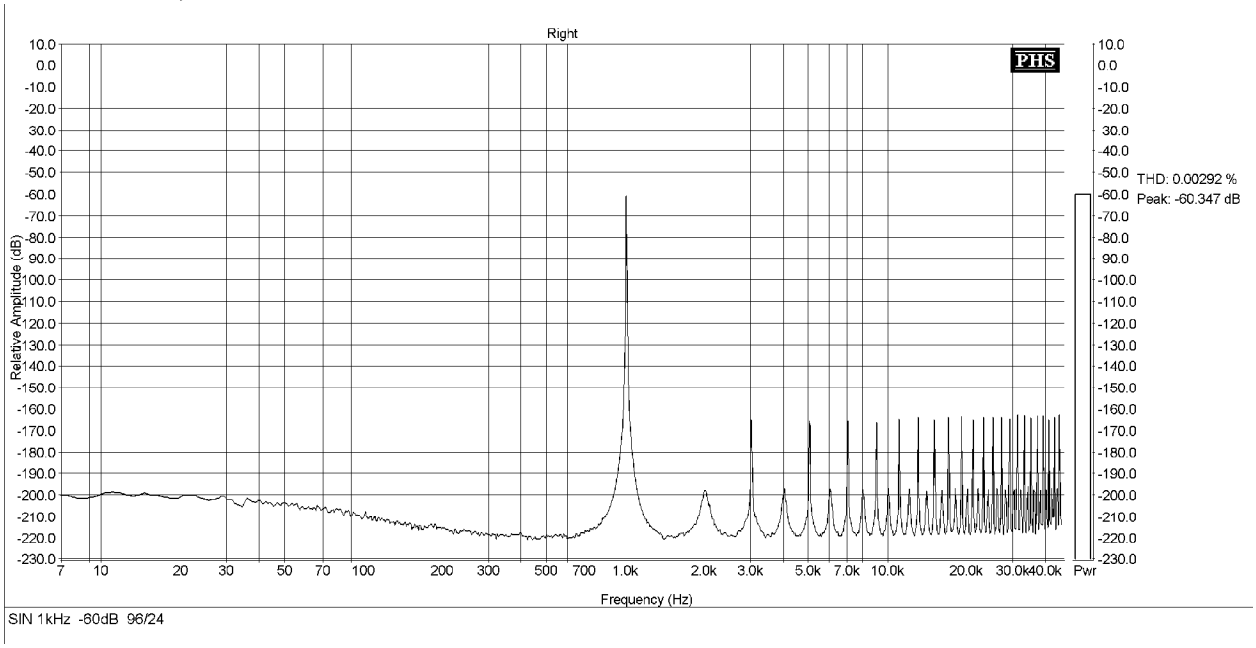
1 kHz Sine 24 bit,  -20dB:



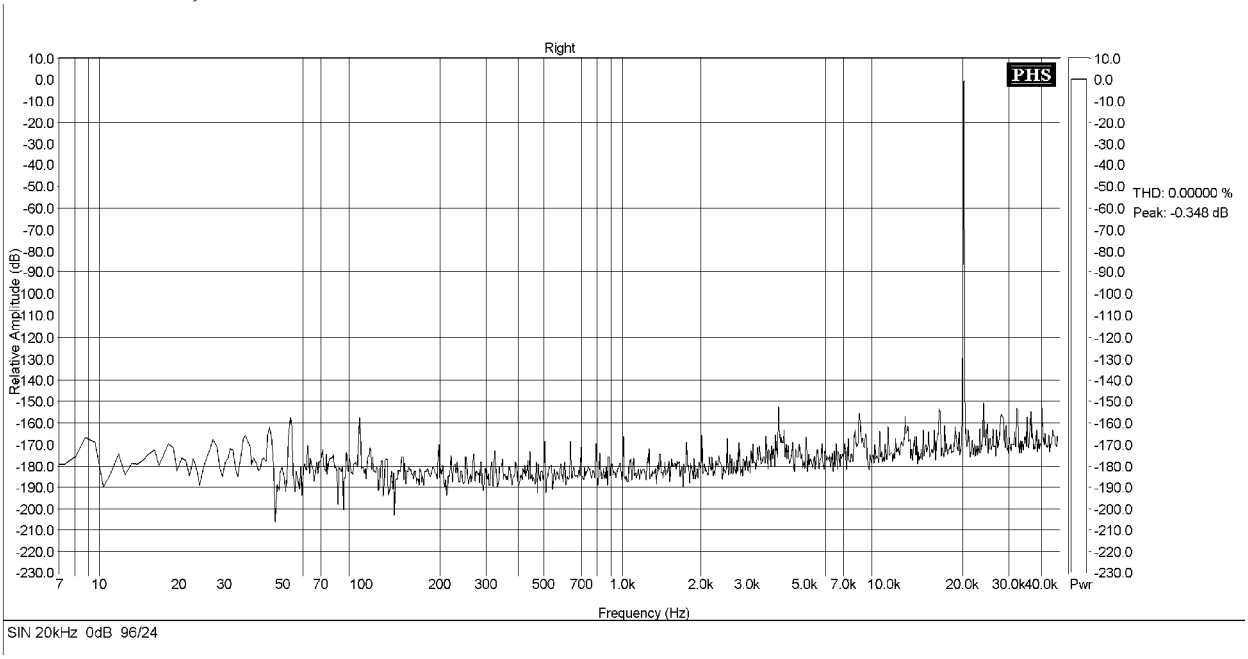

1 kHz Sine 24 bit,  -40dB::



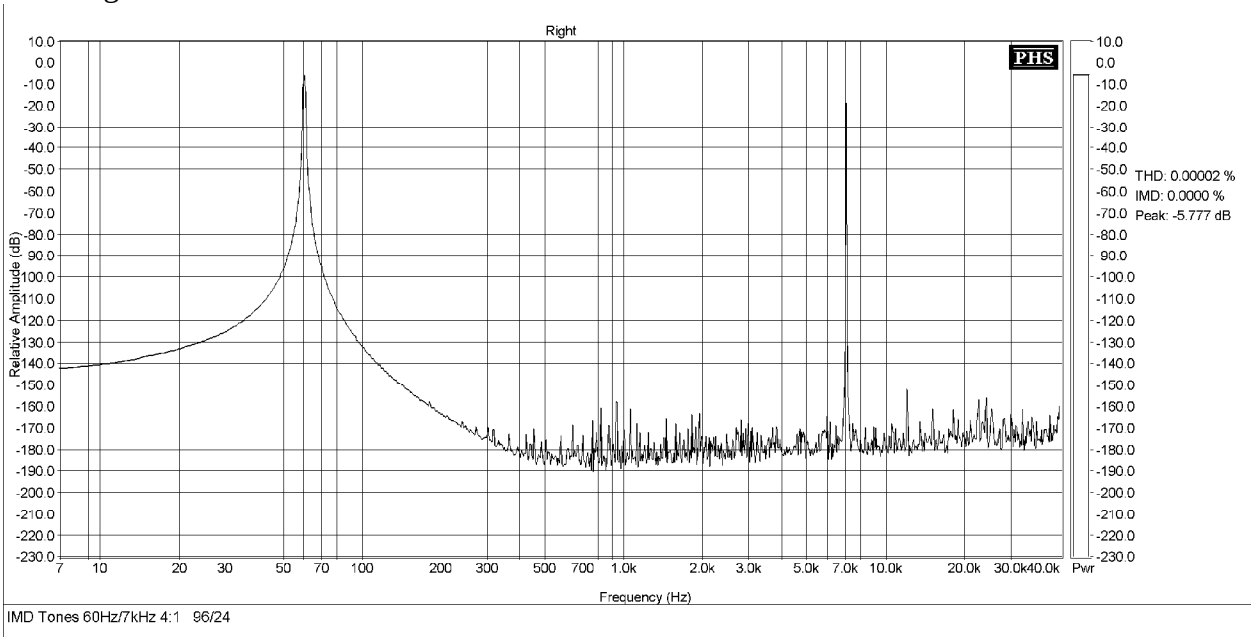
1 kHz Sine 24 bit, -60dB:



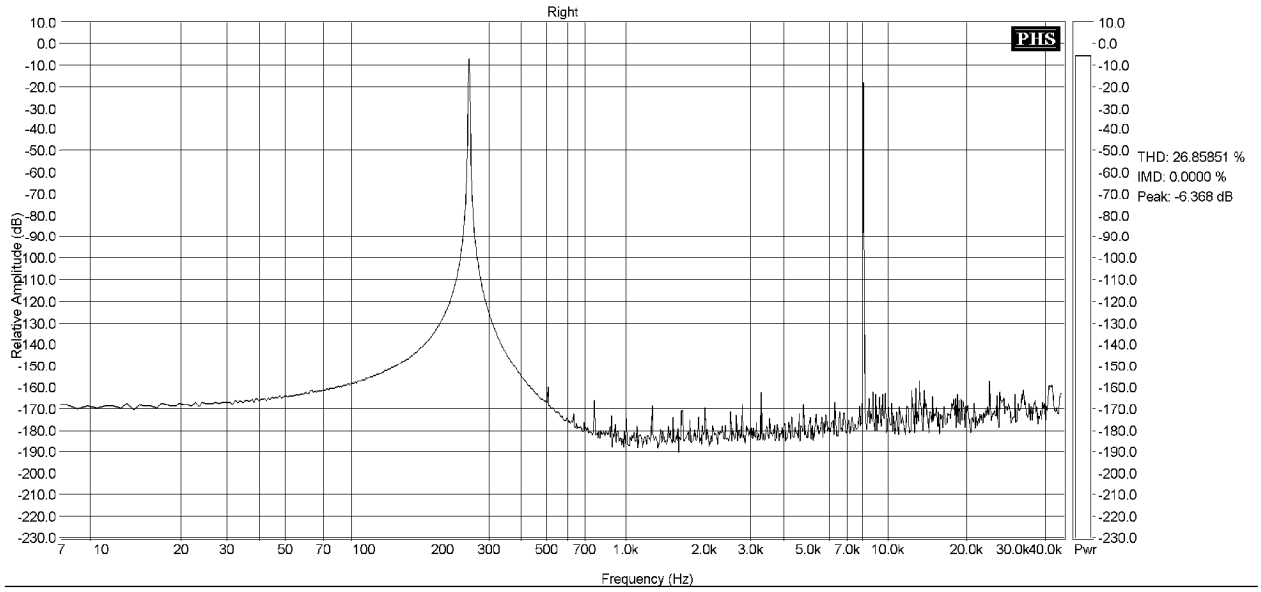

20 kHz Sine 24 bit, 0dB:



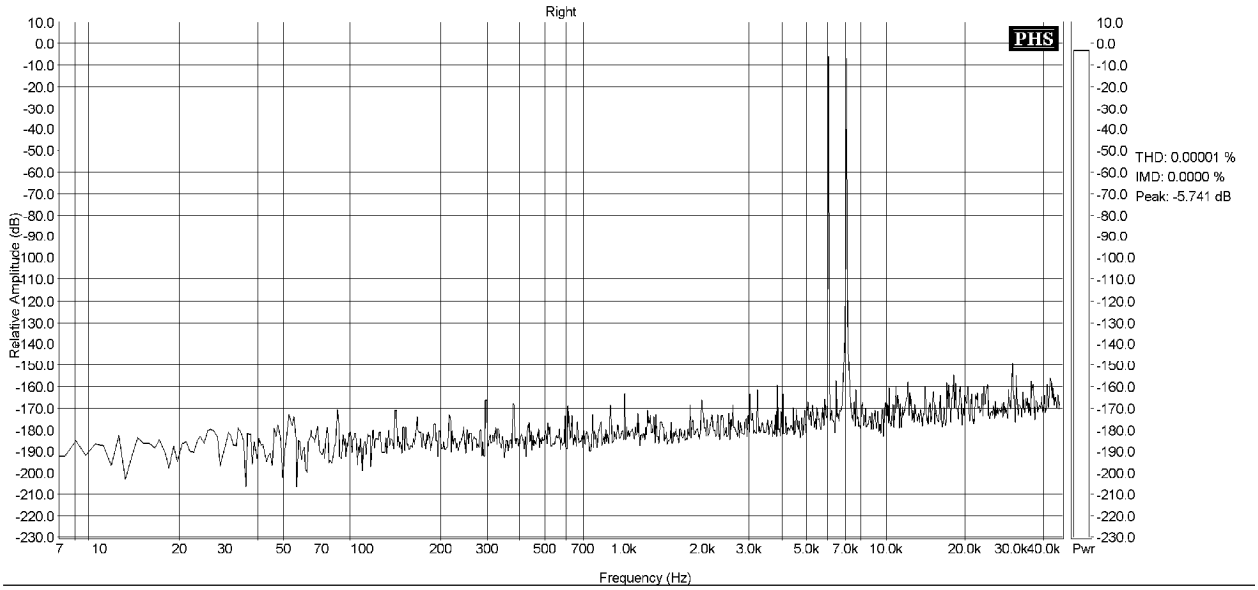
IMD signals:



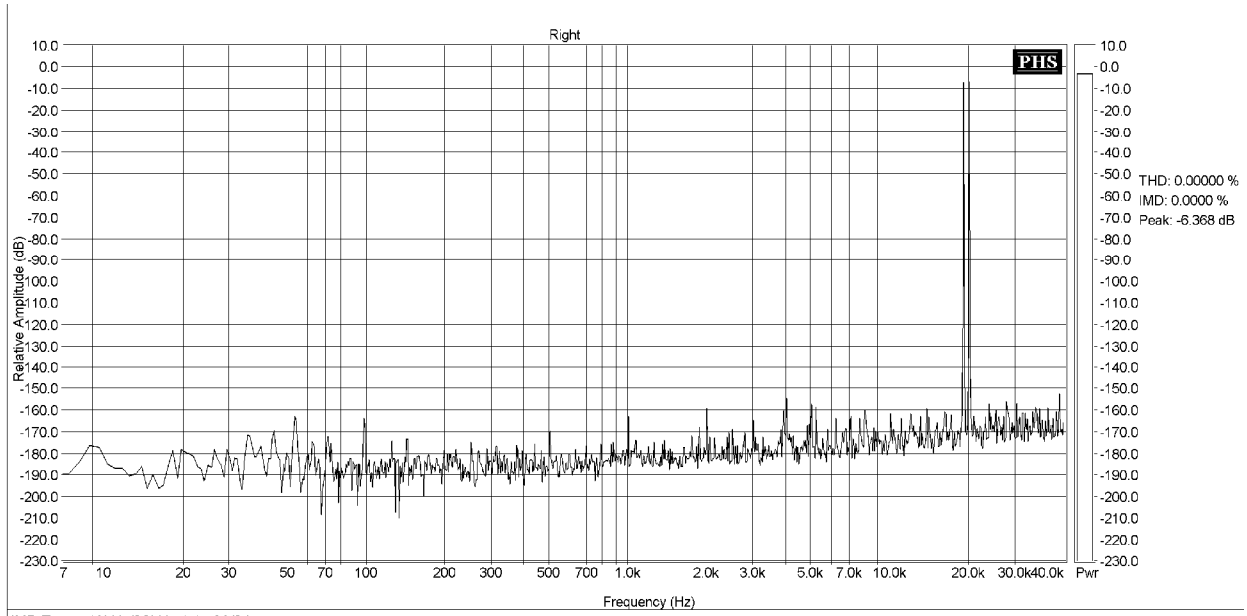

IMD Tones 60Hz/7kHz 4:1 96/24




IMD Tones 250Hz/8kHz 4:1 96/24

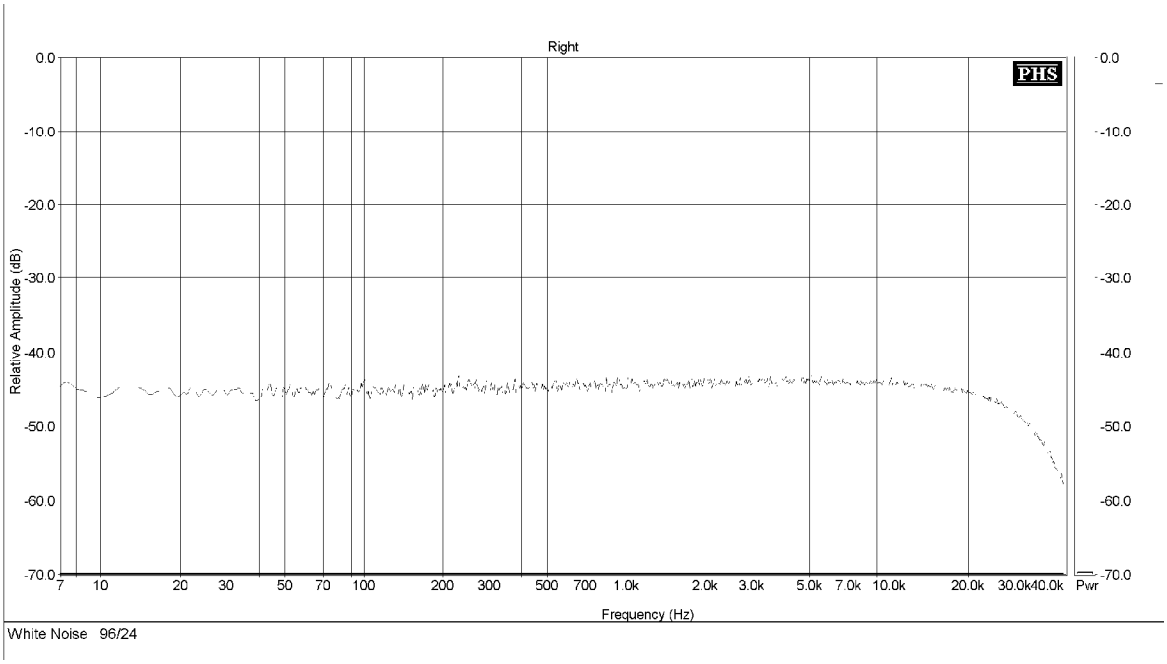



IMD Tones 6kHz/7kHz 1:1 96/24

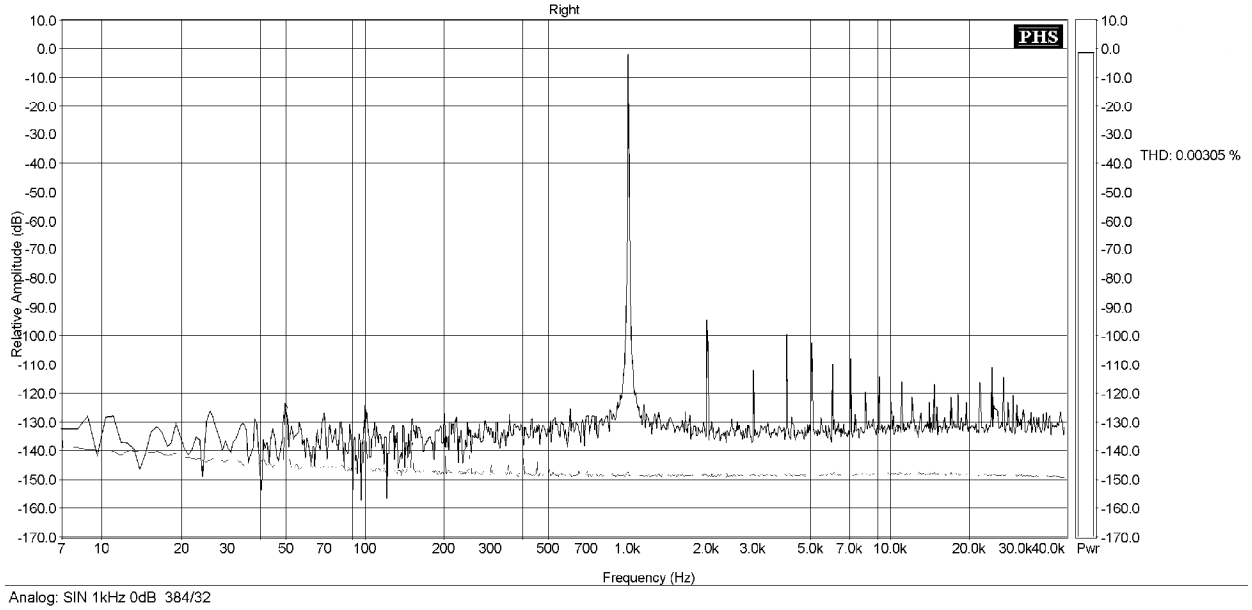


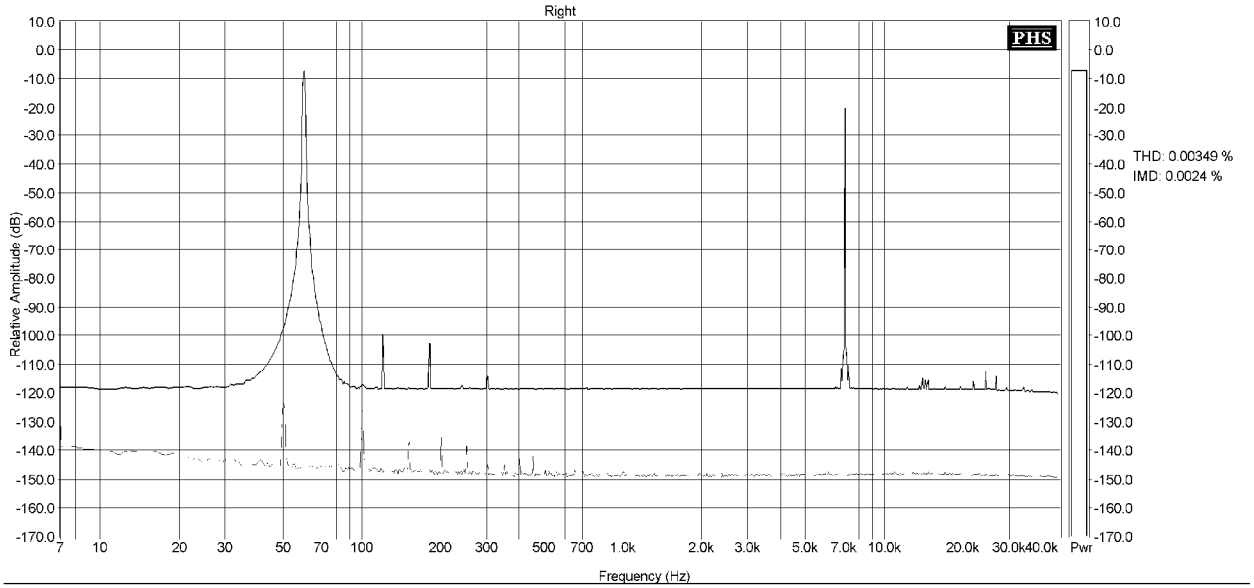

IMD Tones 19kHz/20kHz 1:1 96/24

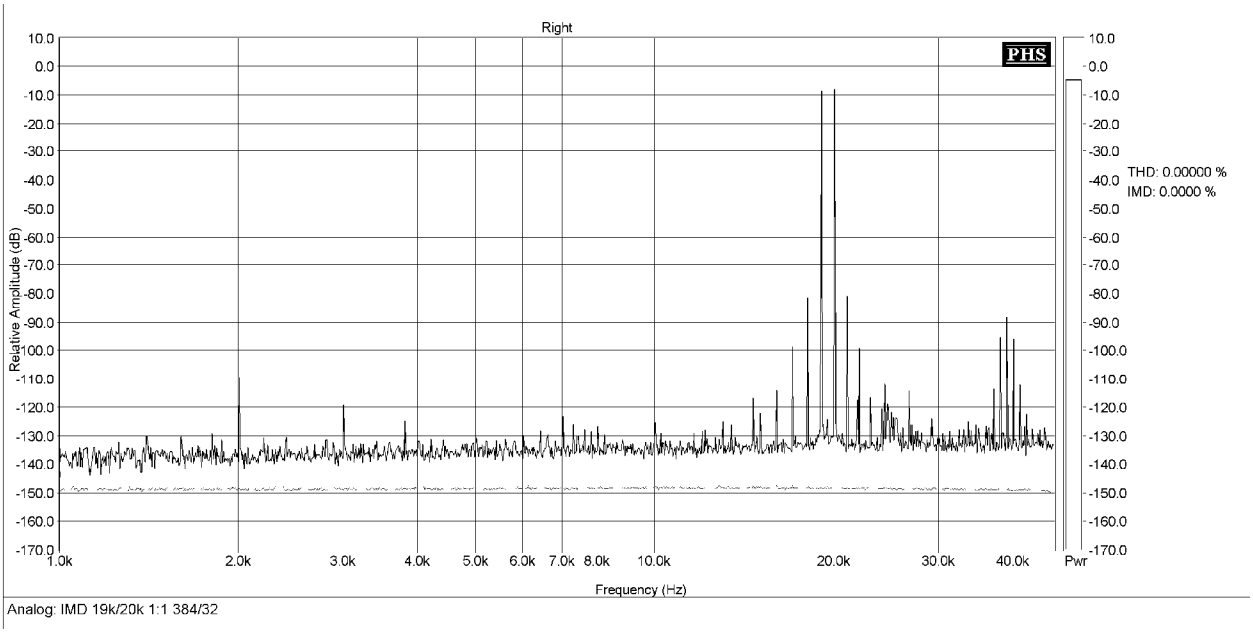
White Noise:




Analog output signals spectrum:






*<u>Note</u>: analog outputs spectrum is the result of the total distortion of synthesized signals, generator's digital-to-analog converter and distortion of analog-to-digital converter, used to capture the signal. Whenever possible, these spectrums will be measured at a higher quality measurement setup.*

## *8.4 Technical Parameters Table.*

| Parameter | Value |
|---|---|
| Digital Output Bus Format | • I2S (16, 24, 32bitt)<br>• Left Justify (16, 24, 32bit)<br>• Right Justify24 (16, 24bit),<br>• Right Justify16 (16bit) |
| Digital Serial Outputs Format | • SPDIF,<br>• SPDIF_CMOS,<br>• TOSLINK |
| Digital outputs level | SPDIF: 1.2v peak-peak @ 75 Ohm<br>SPDIF_CMOS: 5V CMOS<br>I2S/LJ/RJ: 3,3V CMOS<br>EXT, SCALE: 3.3V CMOS (5V tolerant) |
| Digital Output Bus Sample Rate | Fs: 44.1/48/88.2/96/176.4/192/352.8/384 kHz |
| Internal Clock | MCLK frequency: 22.5792/24.576 MHz<br>Initial accuracy: ±1.5ppm<br>Total Stability: ±20ppm<br>Phase Jitter (12kHz-20MHz) - <0.7ps<br>Period Jitter @1000 cycles: 2ps p-p, 14ps rms |
| External Clock | 512Fs (22.5792/24,576 MHz) or<br>1024Fs (45,4584/49.152 MHz), 3-5V CMOS |
| Signal Shapes | 1. Sine wave<br>2. 200ms Sine wave bursts<br>3. Triangle Wave<br>4. Saw Wave<br>5. Square Wave<br>6. Sweep Frequency Sine Wave<br>7. 2 Tone Signal (IMD tests)<br>8. White Noise<br>9. Pink Noise<br>10. Constant Value<br>11. Digital Zero |
| Signal Frequency | Fixed:<br>0.1, 1, 5, 10, 20, 50, 100, 200, 500, 1000 Hz,<br>5, 10, 15, 20, 30, 40, 50, 60 kHz.<br>Variable: 0.1-99999.9 Hz with 0.1 Hz resolution |
| Synthesized Sinus THD | 0.00001% @1000 Hz/0dB<br>0.00015% @1000 Hz/-40dB<br>0.003% @1000 Hz/-60dB |
| Synthesized Sinus IMD | Not measurable. |
| Square Wave rise/fall time | 1/Fs |
| Analog signals level | Sin: 1.7 Vrms (TBD)<br>Triangle/Saw/Square: 4.8V p-p |
| Analog signals output impedance | 500-600 Ohm |
| Analog sinus THD | <0.003% @1000 Hz/0dB |
| Analog Sinus IMD | <0.003% |
| Analog Square Wave rise/fall time | ~5us |
| Analog Square Wave slope | 1.14V/us |
| Dimensions | 205x140x45mm |
| Weight | <1.2kg |

# 9. Remarks

All sketches and photos related to the current model and current firmware version. In later versions may differ slightly, and will be described in the relevant documents.

# 10. Copyright notice

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