

Considerations for Proper Layout of a HIGH-SPEED PCB

A review of the signal integrity demands of digital and analog components. by SYED W. ALI, C.I.D.+

An endless variety of software tools exist to ensure signal integrity at the board level. The critical tool, however, is careful evaluation of considerations to maintain PCB signal integrity.

Take the power supply, for example. A misstep or two here can have adverse effects on the board, and subsequent problems when that design undergoes EMC compliance. If digital high-speed signals aren't correctly routed, they can cause jitter or, worse, a device's complete malfunction. Analog devices, especially those with low-end amplitude analog signals, pose another problematic scenario. Those signals are extremely prone to noise. If digital noise seeps into them from the planar capacitance located between digital and analog planes, those analog devices won't function properly.

What follows are the key considerations for signal integrity, using a high-speed design as an example (FIGURE 1).

The first step is to review board requirements by checking out the schematics or "A" document that relates to the OEM's layout. The crucial data to be clearly identified here include critical signals, digital and analog sections, low amplitude analog sections, high frequencies, low-voltage essential signals (LVES), and high-frequency clocks.

After completing the PCB library and importing the netlist, preliminary component placement is performed based on cus-

tomers input, the various application notes and component data-sheets, combined with layout engineer's expertise. At this point, isolate the critical areas involving analog and digital ICs, FPGAs and connectors that need to be placed at specific locations.

Reviewing the stackup is the second step. The stackup is crucial and is the difference between a highly efficient design with low noise and EMC compliance versus a poorly designed board. An effective stackup relies on certain factors. First is specific board thickness; it cannot be any less or more than the specified maximum thickness. For example, a compact PCI card calls for maximum board thickness of 0.062" because of connector constraints.

The second is the minimum number of layers required for routing; that is typically governed by FPGA depth. The third factor is the impedance requirement on the layout. The thickness requirement can be like the typical 50Ω, 65Ω for PCI and 100Ω for differential signals, as well as sometimes 75Ω for video outputs. The most typical is 50Ω and 100Ω. Basically, 100Ω differential is equivalent to 50Ω single-ended.

Power and ground plane requirements are the next factor to consider. It's known that a reference plane is required for impedance control signals. An ample amount of ground planes meet these particular signals, and they should be unbroken with no voids or splits. The next factor is the number of power planes that depend on the power requirements of the board.

Then, the PCB layout engineer determines if there is a planar capacitance requirement. In recent times, greater numbers of designs require planar capacitance, which is capacitance between the power and ground planes (FIGURE 2). Here, power and ground planes are stacked next to each other with an extremely

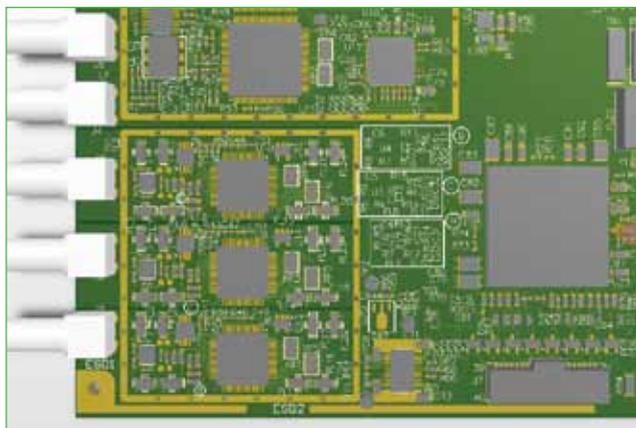


FIGURE 1. Example of a high-speed mixed-signal layout.

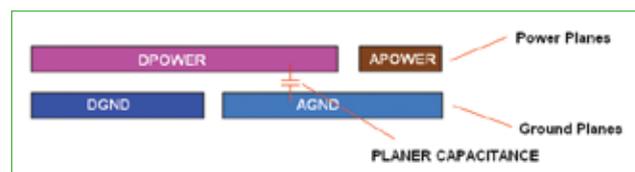


FIGURE 2. Planar capacitance between digital and analog planes can induce noise.

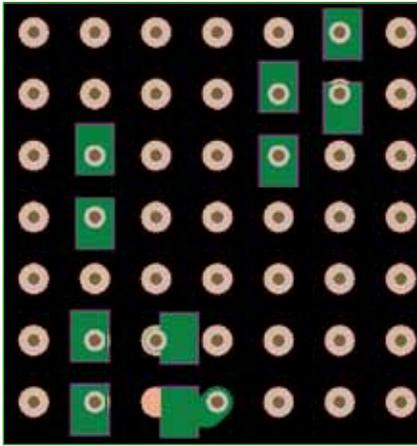


FIGURE 3. Placement of decoupling capacitors on the opposite side of the BGA.

small dielectric between them, for instance 0.003" to 0.005". This provides a blazingly fast switching planar capacitance on the board, and it reduces the requirement for many decoupling capacitors on that particular board.

The type of board material is the last, but not the least, factor associated with stackup. Materials such as FR-4 and its equivalents can be used for up to 5GHz with little or no problems. Higher rise times call for the use of the more exotic materials like Nelco's and Rogers'. The reason: They have a low dielectric constant (Dk) value, which provides for faster signaling and low dielectric losses. However, there are cases where OEMs specify FR-4 at even higher speeds. A major recommendation in this regard is for those OEMs to add filtering to the signals to compensate for the Dk inconsistencies that FR-4 produces.

The actual weave of the material also requires special attention. Weaves come in different types: For example, version 106 is tailored for extremely low speed, while 1080 is an exotic material designed for extremely high speed. The difference is that the high-density 1080 glass weave provides for more constant, uniform dielectric all over the board. It is highly desirable to maintain this uniform dielectric, especially for high-speed signals. Without a uniform dielectric, skews are created. But there are compromises between these two material weaves, such as a medium woven glass style like 2116. It is not very exotic or overly expensive, but acceptable for high-speed signals.

The factors described above are the ones affecting stackup. Once the stackup

is created, it is sent to the printed circuit board fabricator, which verifies it has all necessary materials in-house. At the same time, the layout designer works with the fabricator to work up the trace geometry details based on the impedance requirements on the board.

The Layout

Layout continues once the necessary data come from the fabricator. At this point, take a close look at the skin effect associated with extremely high-speed traces. The higher the speed, the more skin effect there is. To counter this problem, gold plating is used on the high-speed traces and pads, which needs to be specified on the fab drawing.

Laying out the power supplies is the first step. A good idea is to identify all the power supplies on the board, create small blocks of power supplies, and precisely follow manufacturer's guidelines and switchers' datasheets. Switchers are extremely noisy, and most of the noise on the board is due to the power supplies; hence, they should be dealt with first. Power supplies switching nodes need to have very low inductance. Also, feedback traces on the power supplies should be very clean and placed away from these switching nodes.

Once the power supply layout is completed, then the isolation of analog and digital signal starts. That is done during placement as well as routing, so it is an ongoing process during the entire layout phase. At this juncture, digital-to-analog converters (DACs), analog-to-digital converters (ADCs), clock circuitry, and FPGAs are placed, and the power supplies should be isolated by placing them on one of the edges or corners.

Think about the traces not just in terms of routing, but also visualize the returns. While returns are not yet specified as signals, visualize they are going through the ground planes as returns. When a ground plane is created, it must be split between separate analog and digital sections.

Power planes are the next consideration. Isolation between analog and digital power rails and between digital ground and analog ground is recommended. If any of the digital power or ground overlaps with the analog power or ground, it will cause capacitive coupling, which can cause digital noise to be transferred into analog traces. Figure

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1 shows how an overlap between digital and analog planes can induce noise.

Proper placement of decoupling capacitors is a next step to ensure signal integrity. They must be placed ~~right~~ near the IC power and ground pins and connected to a very low inductance trace, both with the pin and to the ground plane through a via. By doing this, ground bounce and VCC sag are avoided during switching. During switching, current can flow through ground traces, hence the need to have a low inductance to the power and ground plane. Also, it helps considerably when planar capacitance is added.

Still another key consideration is proper decoupling capacitors for BGAs. It is recommended that decoupling caps be placed right on the opposite side of the BGA right below the pin itself (**FIGURE 3**). Therefore, BGAs will be fanned out with a via that is on the pad. It's filled either with a conductive or nonconductive filling. Some manufacturers recommend the use of a nonconductive filling because it provides a surface that is more flat after the plating. Vias are placed shut and have a flat finish on the topside. At the opposite side of the BGA, on the bottom side, are the decoupling caps. This provides a low inductance path from the BGA to the power system.

If an FPGA is used in this high-speed design, I/O optimization is necessary before routing is started. This option can be considered either in the layout or in the schematic, and is performed to optimize those signals, because most of those data pins are pin swappable. The schematic designer can switch those I/Os, and once the net list is re-imported, a cleaner view of the rat's nest can be achieved. Consequently, routing becomes simpler and clean once those signals are routed. **PCD&F**

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