

■ Audio Serial Interface Format

The DIF0, DIF1 and DIF2 pins can select eight serial data formats as shown in Table 14. In all formats the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are Slave Modes, and BICK is available up to 128fs at fs=48kHz. In the format equal or less than 20bit (Mode0-2), LSBs in sub-frame are truncated. In Mode 3-7, the last 4LSBs are auxiliary data (see Figure 29).

When the Parity Error, Biphase Error or Frame Length Error occurs in a sub-frame, AK4114 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, AK4114 output "0" from SDTO. In case of using DAUX pin, the data is transformed and output from SDTO. DAUX pin is used in Clock Operation Mode 1, 3 and unlock state of Mode 2.

The input data format to DAUX should be left justified except in Mode5 and 7(Table 14). In Mode5 or 7, both the input data format of DAUX and output data format of SDTO are I²S. Mode6 and 7 are Slave Mode that is corresponding to the Master Mode of Mode4 and 5. In salve Mode, LRCK and BICK should be fed with synchronizing to MCKO1/2.

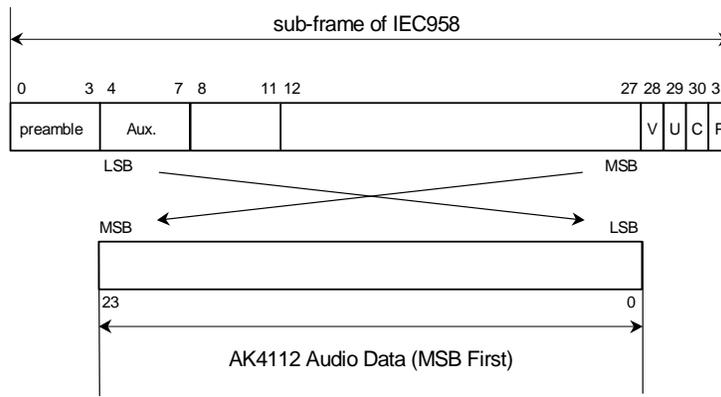


Figure 29. Bit configuration

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK	
							I/O		I/O
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O
5	1	0	1	24bit, I ² S	24bit, I ² S	L/H	O	64fs	O
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I
7	1	1	1	24bit, I ² S	24bit, I ² S	L/H	I	64-128fs	I

Default

Table 14. Audio data format