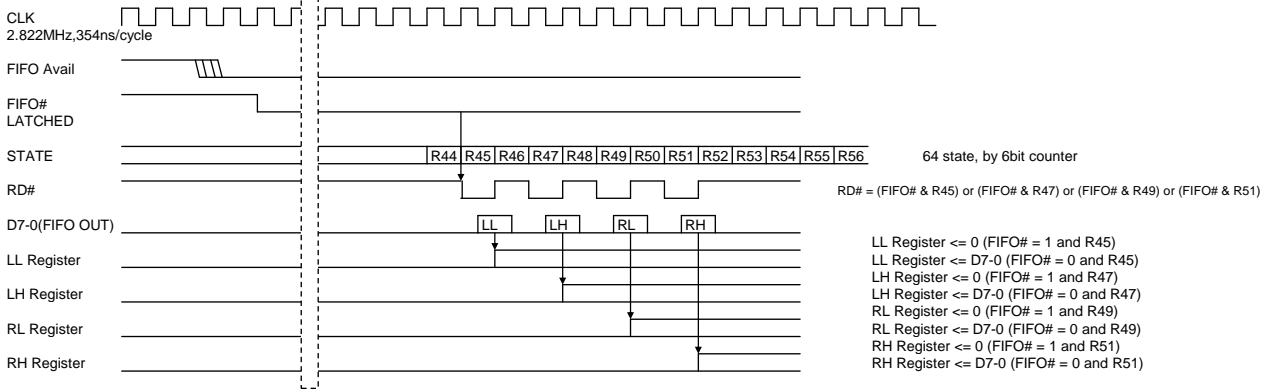
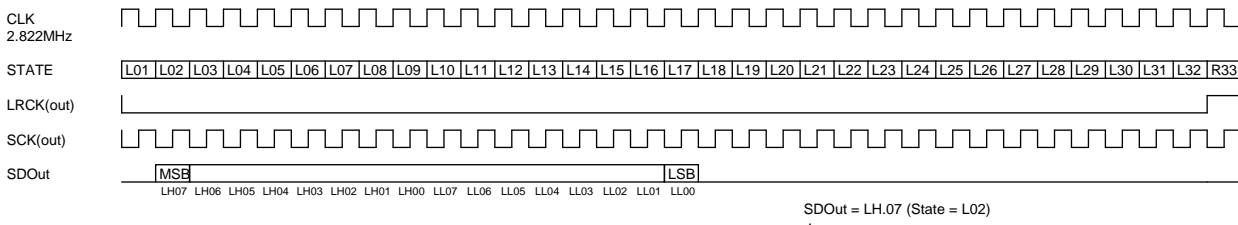


FIFO to I2S CPLD

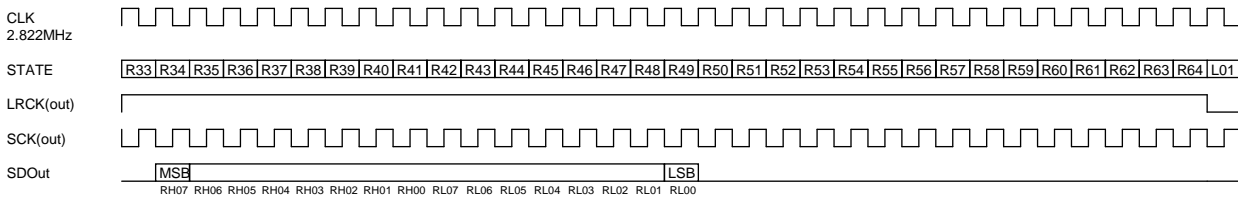
(1) FIFO to Register operation



(2) Register to Output (Left)



(3) Register to Output (Right)



Supposed Circuit Diagram

