Advance Information

PMD200

24-Bit 192kHz HDCD® Decoder

The PMD200 HDCD® Process Decoder is a sophisticated Digital Signal Processor that performs precise decoding of HDCD® encoded audio recordings. The Decoder also functions as a state-of-the-art digital filter when fed data from non-HDCD® recordings. It is designed to interface directly with popular data receivers and digital-to-analog converters, eliminating the need for conventional monolithic digital filters. The PMD200 has been carefully designed to maximize performance and ease of use in a wide variety of applications. The PMD200 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors from Motorola.

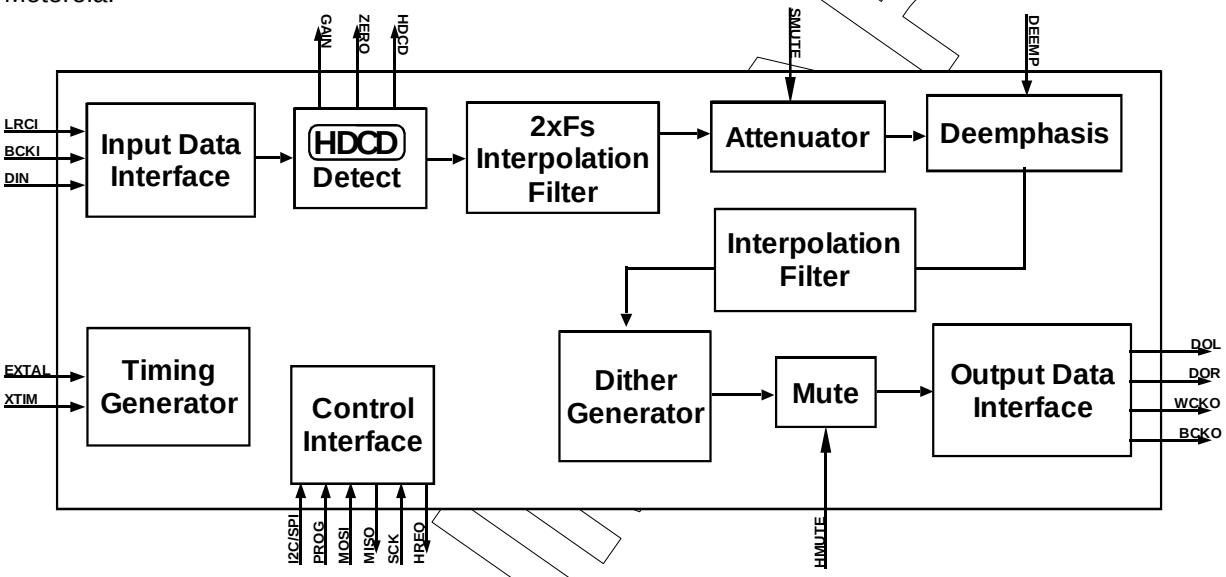

Figure 1 PMD200 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Advance Information

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Data Sheet Conventions

This data sheet uses the following conventions

$\overline{\text{OVERBAR}}$ Used to indicate a signal that is active when pulled low (For example, the RESET pin is active when low).

"asserted" Means that a high true (active high) signal is high, or that a low true (active low) signal is low.

"deasserted" Means that a high true (active high) signal is low, or that a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

High Quality Audio Processing

- 24-bit or Greater Accuracy
- Up to 24-bit Input Data Passed Without Truncation
- HDCD Process Decoding
- High-Quality HDCD Filters
- Digital Domain De-emphasis for 44.1/48 kHz
- SilentConversion™ Technology

Flexible Inputs

- EIAJ/IIS Input Compatible
- 44.1/48/88.2/96/176.4/192 kHz Input Sample Rate Capable
- 16/20/24 Bit Input Capable

Flexible Outputs

- 20/24 bit Output Capable
- Selectable Dither Levels for Optimum Converter Performance
- 8xFs, 4xFs, and 2xFs Output Data Rates for use with a Wide Variety of D-to-A Converters

Convenient System Integration

- 256/384/512/768 x Fs (at 44.1/48 kHz input rate) System Clock Compatible
- Soft and Hard Mute Functions
- Digital Phase Invert Function
- PMD-100 Applications Compatible
- Software Programmable through I2C or SPI Bus
- Hardware Configurable via Pins
- Programmable Digital Attenuator in 0.188dB Steps

DOCUMENTATION

Table x lists the documents that provide a complete description of the PMD200 and are required to design properly with the part. Documentation is available from a local Pacific Microsonics distributor, a Pacific Microsonics sales office, or through the Pacific Microsonics home page on the Internet (the source for the latest information).

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the PMD200 are organized into functional groups, which are listed in **Table 1-1** and illustrated in **Figure 1-1**.

Table 1-1 Functional Groups

Functional Group	Number of Signals	Detailed Description
Power (V_{CC})	18	**Table 1-2**
Ground (GND)	14	**Table 1-3**
Clock and PLL	4	**Table 1-4**
Mode Control and Reset	4	**Table 1-5**
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Serial Audio Input	3	**Table 1-9**
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Unconnected Pins	28	**Table 1-11**

Figure 1-1 Signals Grouped by Function

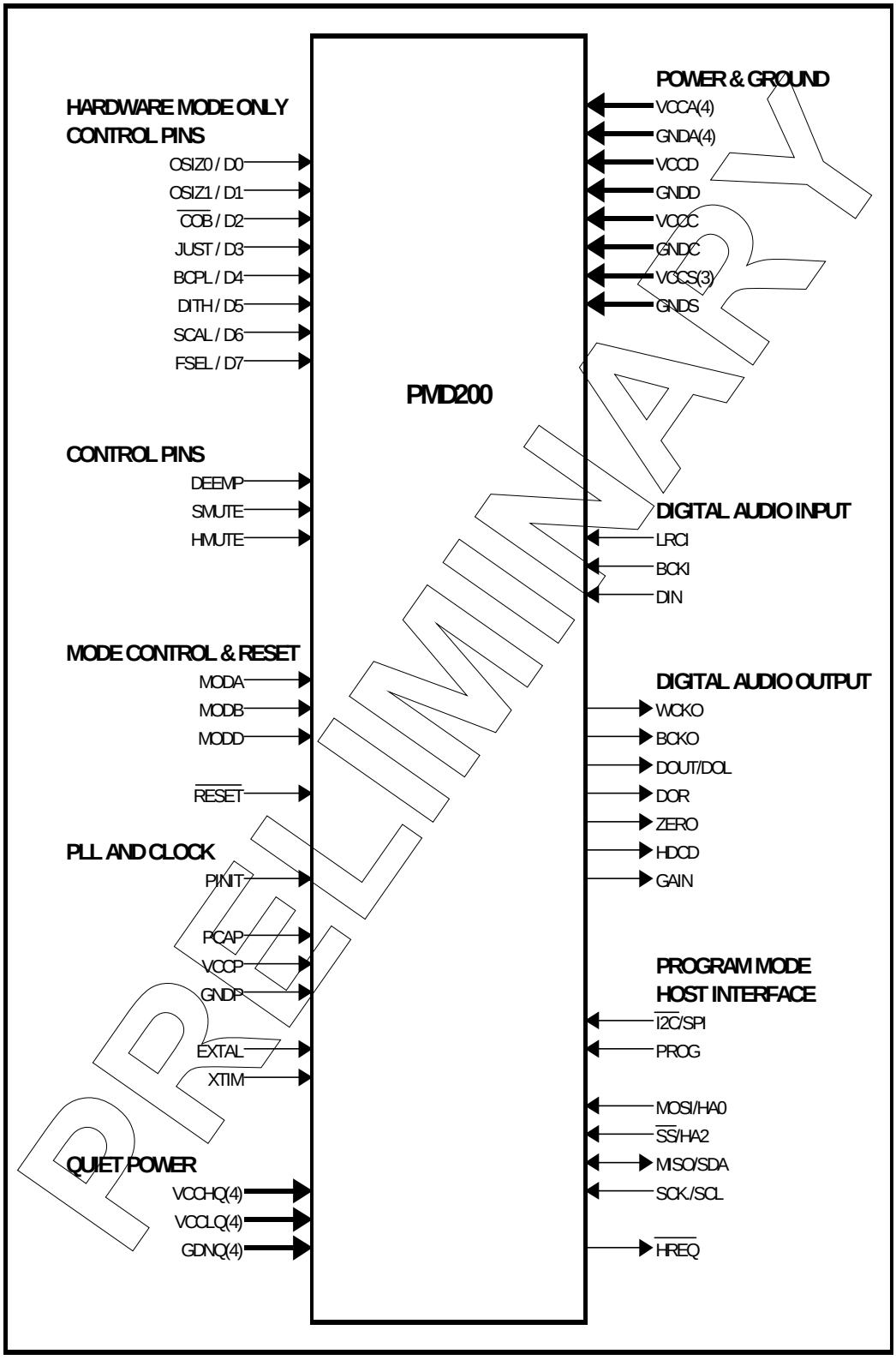


Table 1-2 Power (V_{CC})

Power Name	Description
V_{CCP}	**PLL Power** – V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL}(4)	**Quiet Core (Low) Power** – V_{CCQL} is an isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQL} inputs.
V_{CCQH}(4)	**Quiet External (High) Power** – V_{CCQH} is a quiet power source for I/Ø lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are four V_{CCQH} inputs.
V_{CCA}(4)	**Address Bus Power** – V_{CCA} is an isolated power source for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCA} inputs.
V_{CCD}(1)	**Data Bus Power** – V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCD} input.
V_{CCC}(1)	**Bus Control Power** – V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCC} input.
V_{CCS}(3)	**SHI and SAI** – V_{CCS} is an isolated power for the SHI and SAI. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three V_{CCS} inputs.

Table 1-3 Ground (GND)

Ground Name	Description
GND_P	**PLL Ground** – GND_P is ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GNDP by a 0.47uF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_Q(4)	**Quiet Ground** – GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections
GND_A(4)	**Address Bus Ground** – GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.
GND_D(1)	**Data Bus Ground** – GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_D connections.
GND_C(1)	**Bus Control Ground** – GND_C is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_C connections.
GND_S(3)	**SHI and SAI Ground** – GND_S is an isolated ground for sections of SHI and SAI. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are three GND_s connections.

Table 1-4 Clock & PLL

PMD200 Pin Name	DSP56364 Pin Name	Description
EXTAL	EXTAL	**External Clock Input (input)** – EXTAL is the master clock input for the PMD200.
XTIM	PC5	**External Clock Mode (input)** – XTIM determines if the master clock is 384xFs (HIGH) or 256xFs (LOW) where Fs is either 44.1 or 48 kHz. Additional master clock rates of 512 or 768 x Fs are available from Program mode. *This input is 5V tolerant.*
PCAP	PCAP	**PLL Capacitor (input)** – PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}.

PINIT	PINIT	**PLL Initial (input)** – During assertion of RESET, the value of PINIT is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. PINIT should be pulled low.

Table 1-5 Mode Control & Reset

PMD200 Pin Name	DSP56364 Pin Name	Description
MODA	MODA	**Mode Select A (input)** – This pin should be tied LOW for normal operation. *This input is 5V tolerant.*
MODB	MODB	**Mode Select B (input)** – This pin should be tied LOW for normal operation. *This input is 5V tolerant.*
MODD	MODD	**Mode Select D (input)** – This pin should be tied LOW for normal operation. *This input is 5V tolerant.*
RESET	RESET	**Reset (input)** –RESET is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly-rising input (such as a capacitor charging) to reset the chip reliably. When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODD inputs. The RESET signal must be asserted during power up. A stable EXTAL signal must be supplied before deassertion of RESET. *This input is 5V tolerant.*

Table 1-6 Operation Control

PMD200 Pin Name	DSP56364 Pin Name	Description
PROG	PB2	**Program Mode Select (input)** – HIGH enables Program mode. LOW enables Hardware mode
SMUTE	PC2	**Soft Mute (input)** – Soft Mute ramps the attenuation one step (0.188dB) every 16 input sample periods at 441/48kHz, and 128 periods at 88.2/96kHz. Un-muting is done in the reverse order. *This input is 5V tolerant.*
DEEMP	PC7	**De-emphasis (input)** – Selects the de-emphasis filter (HIGH). DEEMP is only valid for 44.1kHz and 48kHz input rates.

		This input is 5V tolerant.
HMUTE	PC9	**Hard Mute (input)** – Muting is accomplished in one sample. *This input is 5V tolerant.*

Table 1-7 Hardware-mode Only Control

PMD200 Pin Name	DSP56364 Pin Name	Description
OSIZ0	D0	**Output Word Size (input)** – These two pins select the output word size. See table x-x for settings.
OSIZ1	D1	
$\overline{\text{COB}}$	D2	**Complimentary Offset Binary (input)** – Selects between two's-compliment (HIGH) and complimentary-offset-binary (LOW) output formats.
JUST	D3	**Input Justification (input)** – Selects whether the input is right-justified (HIGH) or left-justified (LOW) with respect to LRCI.
BCPL	D4	**Input Bit Clock Polarity (input)** – Determines if input data is latched on the rising edge (HIGH) or the falling edge (LOW) of BCKI.
DITH	D5	**Dither Enable (input)** – In Hardware Mode, DITH selects either TPDF dither (HIGH), or minimal HDCD dither (LOW).
SCAL	D6	**Gain Scale Selection (input)** – When SCALE is LOW, Digital Gain Scaling is enabled (the 6dB gain matching for HDCD Peak Extend vs. non-Peak Extend recordings takes place internal to the processor). When set HIGH, Analog Gain Scaling is enabled (the 6dB gain matching is performed externally, usually in the analog domain, thus optimizing dynamic range performance). See GAIN pin description.
FSEL	D7	**Input Frequency Select (input)** – In Hardware mode, FSEL selects between 44.1 kHz (LOW) and 48 kHz (HIGH) sampling rates. This selection is used to configure the digital de-emphasis filter.

Table 1-8 I2C/SPI Input

PMD200 Pin Name	DSP56364 Pin Name	Description
SPI/$\overline{\text{I2C}}$	PC8	**SPI/I2C Interface Selection (input)** – This pin selects between SPI host interface mode (HIGH) and I2C interface mode (LOW).
D7..D0	D7..D0	**I2C Base Address** - When the PROG pin is HIGH (program mode selected), and I2C is selected, D7..D0 determine the I2C

		base address. D7..D0 are only read after RESET is deasserted.
SCK	SCK	**SPI Serial Clock (input)** – The SCK signal is a Schmitt-trigger input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if the slave select (/SS) signal is not asserted. Data is shifted on one edge of the SCK signal, and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	SCL	**I2C Serial Clock (input)** – SCL carries the clock for the I2C bus transactions in the I2C mode. SCL is a Schmitt-trigger input. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5V tolerant.*
MISO	MISO	**SPI Master-In-Slave-Out (output)** – The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. The signal is an output for the SPI Slave mode, and tri-stated when /SS is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	SDA	**I2C Data and Acknowledge (input or open-drain output)** – In I2C mode, SDA is a Schmitt-trigger input when receiving, and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5V tolerant.*
MOSI	MOSI	**SPI Master-Out-Slave-In (input)** – MOSI is the slave data input line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. The signal is a Schmitt-trigger input.
HA0	HA0	**I2C Slave Address 0 (input)** – This signal uses a Schmitt-trigger input when configured in the I2C mode. The HA0 signal is used to form the slave device address. HA0 overrides bit 0 of the base address. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5V tolerant.*

$\overline{SS}$	$\overline{SS}$	**SPI Slave Select (input)** – This signal is an active low Schmitt-trigger input when configured for the SPI mode. This signal is used to enable the SPI slave for transfer. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks, and keeps the MISO output signal in the high-impedance state.
HA2	HA2	**I2C Slave Address 2(input)** – This signal uses a Schmitt-trigger input when configured for the I2C mode. When configured for the I2C mode, the HA2 signal is used to form the slave device address. HA2 overrides bit 2 of the base address. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5V tolerant.*
$\overline{HREQ}$	$\overline{HREQ}$	**Host Request (output)** – This signal is an active low output when configured in the SPI mode. $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer, and deasserted at the first clock pulse of the new data word transfer. The signal is tri-stated during hardware, software, or individual reset. There is no need for external pull-up in this state

Table 1-9 Serial Audio Input

PMD200 Pin Name	DSP56364 Pin Name	Description
LRCI	FSR	**Input Data Frame Sync (input)** – LRCI expects a 50% duty cycle square wave at the incoming sampling frequency. Low to high transitions frame left channel data; high to low transitions frame right channel data. In the case of IIS input modes, high to low transitions frame the left channel, while low to high transitions frame the right. In addition, for IIS mode, LRCI occurs one BCKI cycle earlier than the start of the MSB. *This input is 5V tolerant.*
BCKI	SCKR	**Input Data Bit Clock (input)** – Clocks the incoming data into the serial-to-parallel input registers. Input clocking occurs on the rising edge of BCKI. *This input is 5V tolerant.*
DIN	SDI0	**Input Data (input)** – Assumed to be MSB-first 2's-compliment, left channel followed by right channel. If data is absent (all 0's for 8192 words at 44.1/48 kHz sampling rate), or either input clock is removed, an internal MUTE is activated. *This input is 5V tolerant.*

Table 1-10 Serial Audio Output

PMD200 Pin	DSP56364	Description

Name	Pin Name	
WCKO	FST	**Output Frame Sync (output)** – WCKO is the output word clock at the sampling frequency. In the case of interleaved left/right data output, when WCPL=LOW, it is a 50% duty cycle square wave with the rising edge corresponding to the start of the left channel data word, and the falling edge corresponding to the start of the right channel data word. In the case of separate data outputs and WCPL=LOW, WCKO is low-going at the conclusion of the output data word, and goes high at the start of the next word. When WCPL=HIGH, WCKO functions with opposite polarity.
BCKO	SCKT	**Output Bit Clock (output)** – BCKO is the output data shift clock. BCKO shifts data out on the falling clock edge.
DOUT/DOL	SDO0	**Output Data (output)** – Left/Right data for interleaved operation, and left channel data output for separate data outputs. Data output format is MSB first, right justified for separate outputs. When in interleaved mode, the left channel is output first followed by the right channel, and data is right justified relative to WCKO.
DOR	SDO1	**Output Data (output)** – Right channel data output in separate data mode.
GAIN	PB3	**Gain Scale Control (output)** – GAIN remains HIGH if SCALE is set LOW, but will go LOW for non-HDCD recordings, and HDCD recordings which do not use peak extension if SCALE is set to HIGH.
ZERO	PB1	**Audio Zero Detect (output)** – ZERO indicates (HIGH) that the input data has contained only zeros for 8192 consecutive samples. It resets LOW when non-zero data reappears.
HDCD	PB0	**HDCD Indicator (output)** – HDCD goes HIGH if an HDCD recording is detected. HDCD is LOW in all other cases.

Table 1-11 Unconnected Pins

PMD200 Pin Name	DSP56364 Pin Name	Description
NC0-27	A0-A17 AA0-AA1 $\overline{\text{CAS}}$ $\overline{\text{RD}}$ $\overline{\text{WR}}$ $\overline{\text{TA}}$ TCK TDI TDO TMS	**Unconnected Pins** – The listed signals are not used by the PMD200, and should be left unconnected.

SECTION 2

SPECIFICATIONS

INTRODUCTION

The PMD200 is a high-density CMOS device with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The PMD200 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or VCC). The suggested value for a pull-up or pull-down resistor is 10kΩ.

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst-case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

ABSOLUTE MAXIMUMS

Table 2-1 Absolute Maximums

Rating[1]	Symbol	Value[1,2]	Unit
Supply Voltage	V_{CC}	-0.3 to +4.0	V
All input voltages excluding “5V tolerant” inputs[3]	V_{IN}	GND–0.3 to VCC+0.3	V
All “5V tolerant” input voltages[3]	V_{IN5}	GND-0.3 to VCC+3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	-40 to +105	^oC
Storage temperature	T_{STG}	-55 to +125	^oC

Notes:
1. GND = 0V, V_{CC} = 3.3V +- 0.16V, T_J = 0^{o}C to +105^{o}C, C_L = 50pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. **CAUTION**: All “5V Tolerant” input voltages must not be more than 3.95V greater than the supply voltage; this restriction applies to “power on,” as well as during normal operation. In any case, the input voltages cannot be more than 5.75V. “5V Tolerant” inputs are inputs which tolerate 5V.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\Theta JA}$ or Θ_{JA}	49.87	$^oC/W$
Junction-to-case thermal resistance[2]	$R_{\Theta JC}$ or Θ_{JC}	9.26	$^oC/W$
Thermal characterization parameter	Ψ_{JT}	2.0	$^oC/W$

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection. (SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111.) Measurements were done with parts mounted on thermal test boards conforming to specification EIA/JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

DC ELECTIRCAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.14	3.3	3.46	V
Input high voltage					
• Bunch of signals	V_{IH}	2.0	--	V_{CC}	
• MOD, RESET, PINIT, and all ESAI/GPIO/SHI (SPI mode) pins	V_{IHP}	2.0	--	V_{CC}+3.95	V
• SHI (I2C mode) pins	V_{IHP}	1.5	--	V_{CC}+3.95	
• XTI[8]	V_{IHX}	0.8xV_{CC}	--	V_{CC}	
Input low voltage					
• A bunch of signals	V_{IL}	-0.3	--	0.8	
• A bunch of signals	V_{ILP}	-0.3	--	0.8	V
• SHI (I2C mode) pins	V_{ILP}	-0.3	--	0.3xV_{CC}	
• XTI[8]	V_{ILX}	-0.3	--	0.2xV_{CC}	
Input leakage current	I_{IN}	-10	--	10	µA
High impedance (off-state) input current (@ 2.4V/0.4V)	I_{TSI}	-10	--	10	µA
Output high voltage					
• TTL (I_{OH} = -0.4mA)[5,7]	V_{OH}	2.4	--	--	V
• CMOS (I_{OH} = -10µA)[5]		V_{CC}-0.01	--	--	V
Output low voltage					
• TTL (IOL = 3.0mA, open-drain pins IOL = 6.7mA)[5,7]	V_{OL}	--	--	0.4	V
• CMOS (IOL = 10µA)[5]		--	--	0.01	V
Internal supply current[2]	I_{CCI}	---	127	181	mA
PLL supply current		--	1	2.5	mA
Input capacitance[5]	C_{IN}	--	--	10	pF

Notes:
1. Refers to MODA, MODB, and MODD pins.
2. Power Consumption Considerations on **Page 10-4** provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC}=3.3V at T_J=105°C. Maximum internal supply current is measured with V_{CC}=3.46V at T_J=105°C.
3. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL signal is disabled during Stop state.
4. In order to
5. Periodically sampled and not 100% tested.
6. V_{CC}=3.3V +- 0.16V; T_J=0°C to +105°C, C_L=50pF
7. This characteristic does not apply to PCAP.
8. Driving XTI to low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9xV_{CC} and the maximum should be no higher than 0.1xV_{CC}.

AC ELECTRICAL CHARACTERISTICS

The specifications in the AC electrical characteristics section are derived from specifications provided in the *Motorola DSP56364 Technical Datasheet* (DSP56364/D Rev 1). Timing waveforms are tested with a V_{IL} maximum of 0.3V and a V_{IH} minimum of 2.4V for all pins except EXTAL, which is tested using the input levels shown in Note 8 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. Output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4V and 2.4V respectively.

Note: Although the minimum value for the frequency of EXTAL is 0MHz, the device AC test conditions are 15MHz and rated speed.

INTERNAL CLOCKS

Table 2-4 Internal Clocks

Characteristics	Symbol	Expression[1,2]		
		Min	Typ	Max
Internal operation frequency	f	--	(Ef x 16)/DF	--
Internal clock high period	T_H	0.47 x ET_C x DF/16	--	0.53 x ET_C x DF/16
Internal clock low period	T_L	0.47 x ET_C x DF/16	--	0.53 x ET_C x DF/16
Internal clock cycle time[3]	T_C	--	ET_C x DF/16	2 x ET_C
Instruction cycle time	I_{CYC}		T_C	--

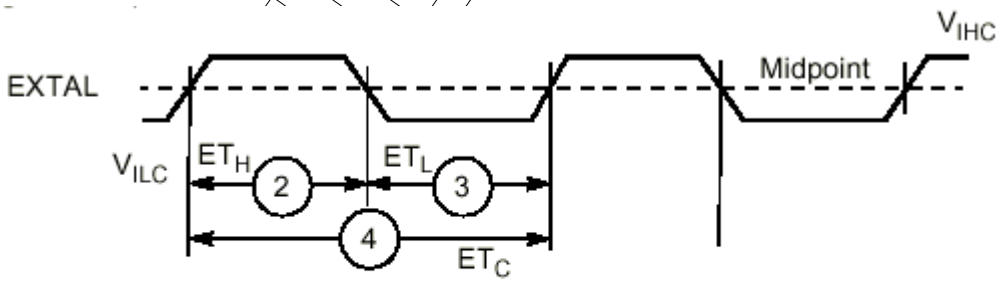
Notes:
1. DF = Internal Division Factor (see Table 3-2)
   Ef = External frequency
   ET_C = External clock cycle
   T_C = internal clock cycle
2. See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.
3. During PMD200 initialization (coming out of reset), the PMD200 has not yet enabled its PLL. Therefore, T_C during startup is specified as 2 x ET_C during this time.

EXTERNAL CLOCK OPERATION

Table 2-5 External Clocks

No.	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) – The rise and fall time of this external clock should be 3ns maximum.	Ef	1.875 MHz	18.75 MHz
2	EXTAL input high[1]	ET_H	4.67 ns	157.0 µs
3	EXTAL input low[1]	ET_L	4.67 ns	157.0 µs
4	EXTAL cycle time	ET_C	53.33 ns	533 ns

Notes: 1. Measured at 50% of the input transition



Note: The midpoint is 0.5 (V_{IHC} + V_{ILC}).

Figure 2-1 External Clock Timing

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 PLL Characteristics

Characteristics	Min	Max	Unit
VCO frequency when PLL enabled (16 x Ef x 2/DF) See Table x-x for the correct DF for a particular master clock	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1])	13.28	23.52	nF

Notes: 1. C_{PCAP} is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}). The recommended value in nF for C_{PCAP} is 17.6 nF.

RESET AND MODE SELECT TIMING

Table 2-7 Reset and Mode Select Timing

No.	Characteristics	Expression	Min	Max	Unit
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[1]	--	--	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[2]	50 x ET_C	500.0	--	ns
13	Mode select setup time		30.0	--	ns
14	Mode select hold time		0.0	--	ns

Notes: 1. Periodically sampled and not 100% tested
2. $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted and V_{CC} is valid, and the EXTAL input is active and valid.

When the V_{CC} is valid, but $\overline{\text{RESET}}$ is not asserted and the EXTAL input is not yet active and valid, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

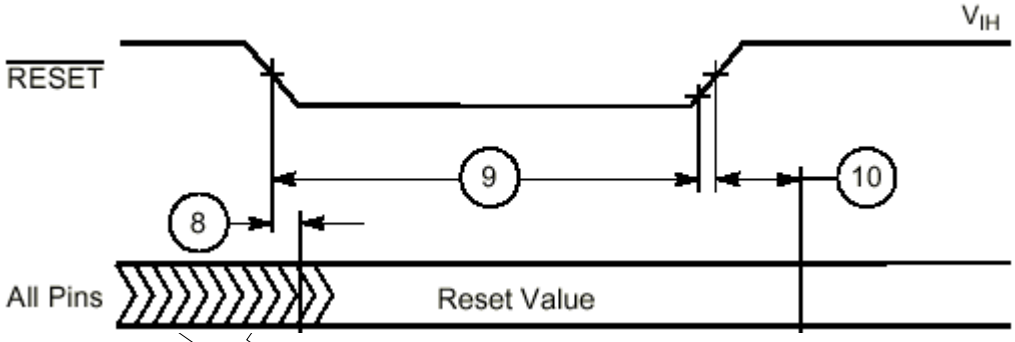


Figure 2-2 Reset Timing

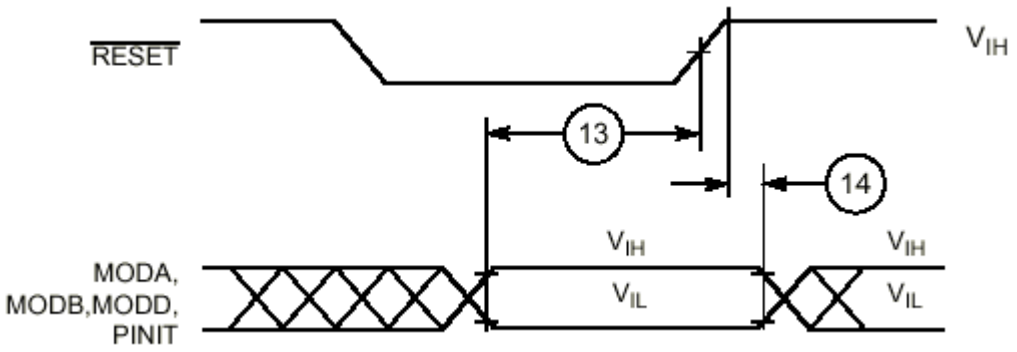


Figure 2-3 Mode Select Timing

SERIAL HOST INTERFACE SPI PROTOCOL TIMING

Table 2-8 SHI Timing, SPI Mode

No.	Characteristics	Expression	Min	Max	Unit
140	Tolerable spike width on clock or data input	--		50	ns
142	Serial clock high period	$2.5xT_C+102$	127	--	ns
143	Serial clock low period	$2.5xT_C+102$	127	--	ns
144	Serial clock rise/fall time	--	--	2000	ns
146	$\overline{SS}$ assertion to first SCK edge	0	0	--	ns
147	Last SCK edge to $\overline{SS}$ not asserted	102	102	--	ns
148	Data input valid to SCK edge (data input set-up time)	$MAX\{(20-T_C),0\}$	10	--	ns
149	SCK last sampling edge to data input not valid	$2.5xT_C+30$	55	--	ns
150	$\overline{SS}$ assertion to data out active	2	2	--	ns
151	$\overline{SS}$ deassertion to data high impedance	9	--	9	ns
152	SCK edge to data out valid (data out delay time)	$2xT_C+123$	--	143	ns
153	SCK edge to data out not valid (data out hold time)	T_C+55	65	--	ns
157	First SCK sampling edge to $\overline{HREQ}$ output deassertion	$2.5xT_C+120$	--	145	ns
158	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted	$2.5xT_C+80$	105	--	ns
Notes: Periodically sampled, not 100% tested					

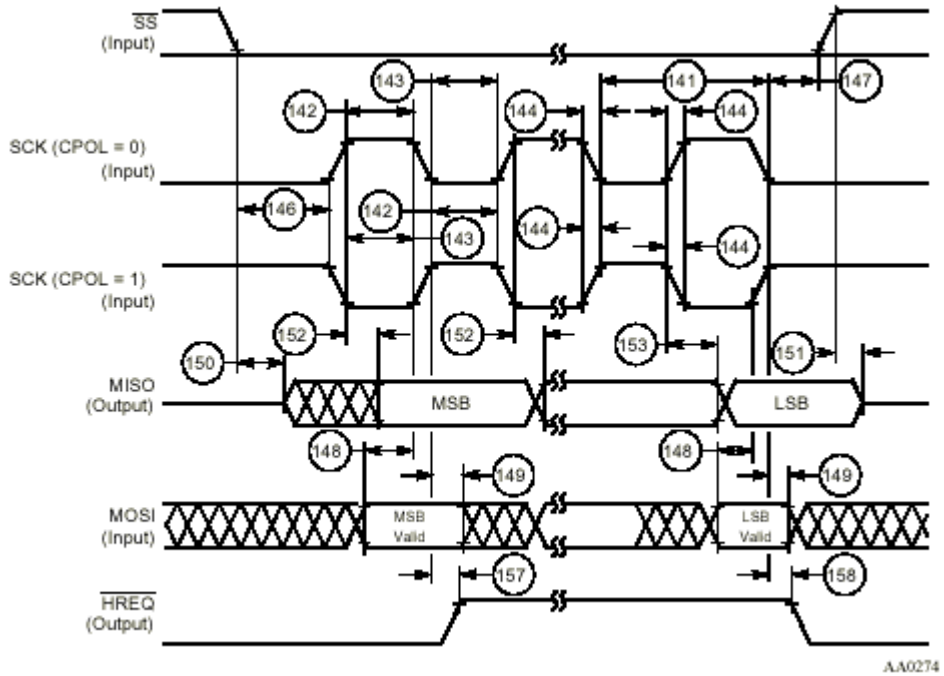


Figure 2-4 SHI Timing, SPI Mode

SERIAL HOST INTERFACE (SHI) I2C PROTOCOL TIMING

Table 2-9 SHI Timing, I2C Mode

No.	Characteristics	Symbol / Expression	Min	Max	Unit
	Tolerable spike width on SCL or SDA	--	--	50	ns
171	SCL clock frequency	F_{SCL}	--	100	kHz
172	Buss free time	T_{BUF}	4.7	--	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	--	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	--	µs
175	SCL low period	T_{LOW}	4.7	--	µs
176	SCL high period	T_{HIGH}	4.0	--	µs
177	SCL and SDA rise time	T_R	--	1000	ns
178	SCL and SDA fall time	T_F	--	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	--	ns
180	Data hold time	$T_{HD;DAT}$	0.0	--	µs
181	Stop condition set-up time	$T_{SU;STO}$	4.0	--	µs
182	Capacitive load for each line	C_b	--	400	PF
183	DSP clock frequency	F_{DSP}	11.8	--	MHz
184	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ set-up time)	$T_{SU;RQI}$	0.0	--	ns
186	First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion2	$T_{NG;RQO}$	--	140	ns
187	Last SCL edge to $\overline{\text{HREQ}}$ output not deasserted	$T_{AS;RQO}$	100	--	ns
188	$\overline{\text{HREQ}}$ in assertion to first SCL edge	$T_{AS;RQI}$	4282	--	ns
Notes:	R_p(min) = 1.5k				

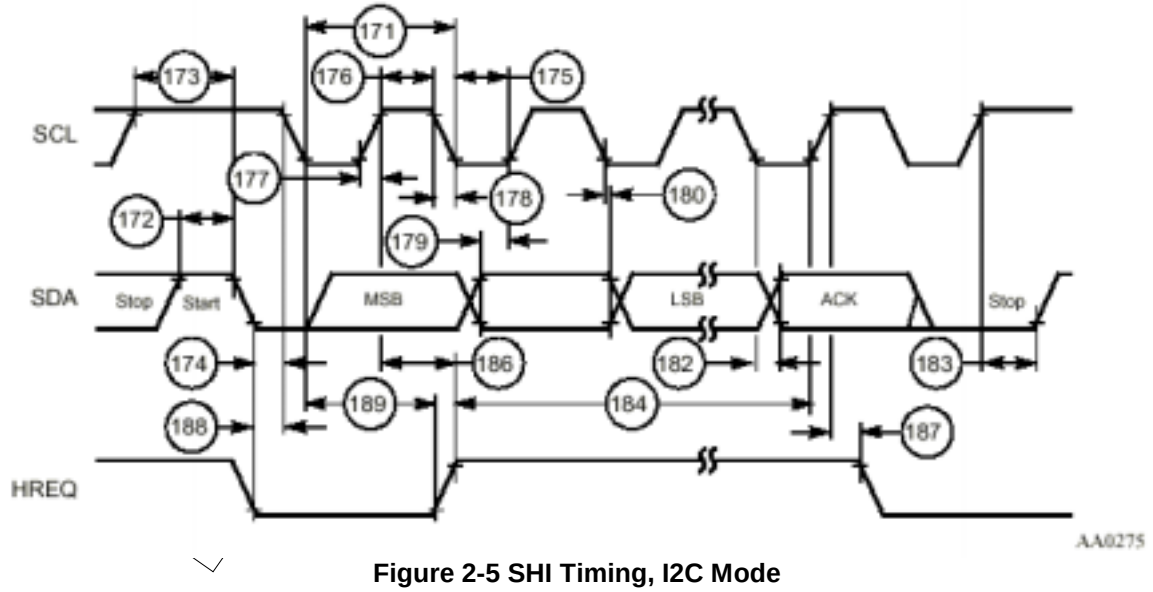


Figure 2-5 SHI Timing, I2C Mode

SERIAL AUDIO INTERFACE TIMING

Table 2-10 Serial Audio Interface timing

No	Characteristics[1,2,3]	Symbol	Expression	Min	Max	Unit
430	Clock cycle • Transmit • Receive	t_{SSICC}	 $4xT_C$ $3xT_C$	 40.0 30.0	 -- --	ns
431	Clock high period • Transmit • Receive	--	 $2xT_C - 10.0$ $1.5xT_C$	 10.0 15.0	 -- --	ns
432	Clock low period • Transmit • Receive	--	 $2xT_C$-10.0 $1.5-T_C$	 10.0 15.0	 -- --	ns
440	Data in hold time after BCKI falling edge	--	--	5.0	--	ns
442	LRCI input before BCKI falling edge	--	--	23.0	--	ns
450	BCKO rising edge to WCKO high	--	--	--	16.0	ns
451	BCKO rising edge to WCKO low	--	--	--	17.0	ns
454	BCKO rising edge to data out valid	--	--	--	21.0	ns
Notes:	V_{CC}=3.16 $^{+}_{-}$ 0.16; T_J = 0°C to +105°C; C_L = 50pF					

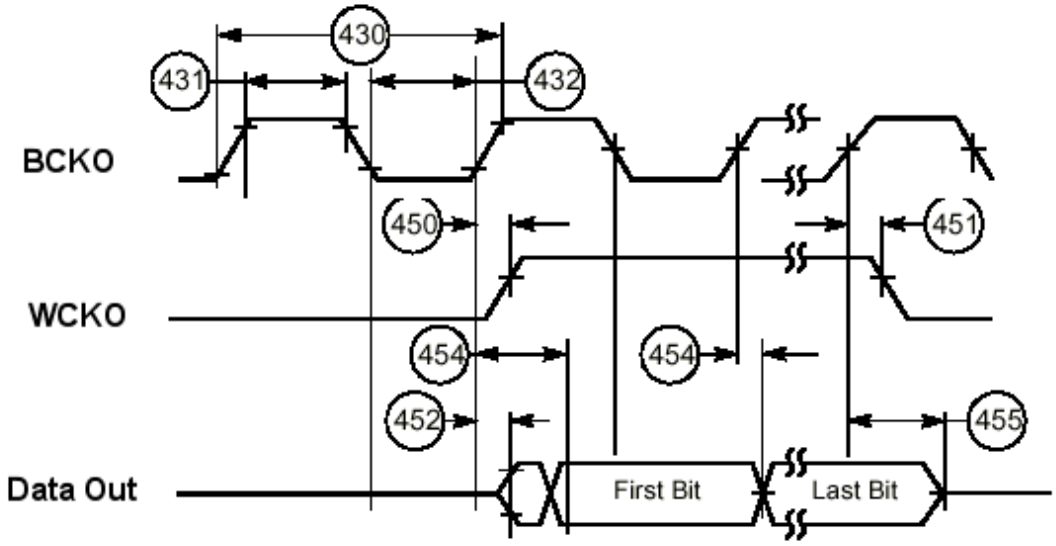


Figure 2-6 Serial Audio Output Timing

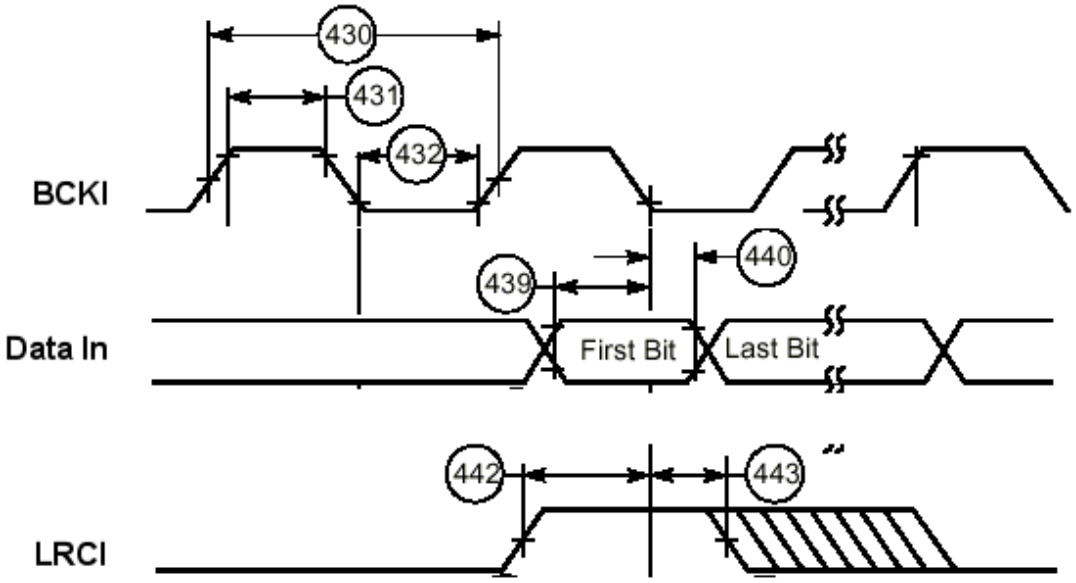


Figure 2-7 Serial Audio Input Timing

AUDIO CHARACTERISTICS

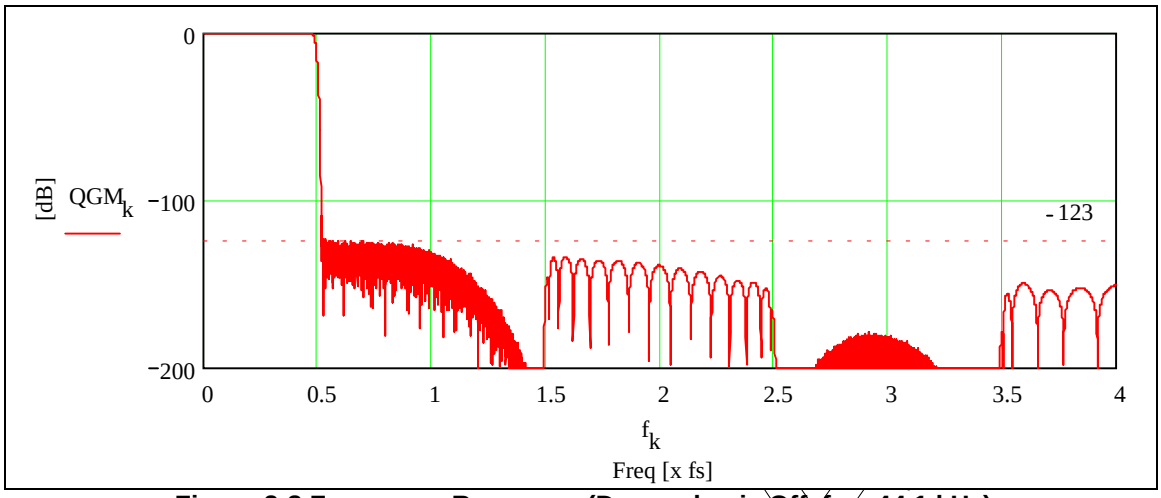


Figure 2-8 Frequency Response (De-emphasis Off, fs = 44.1 kHz)

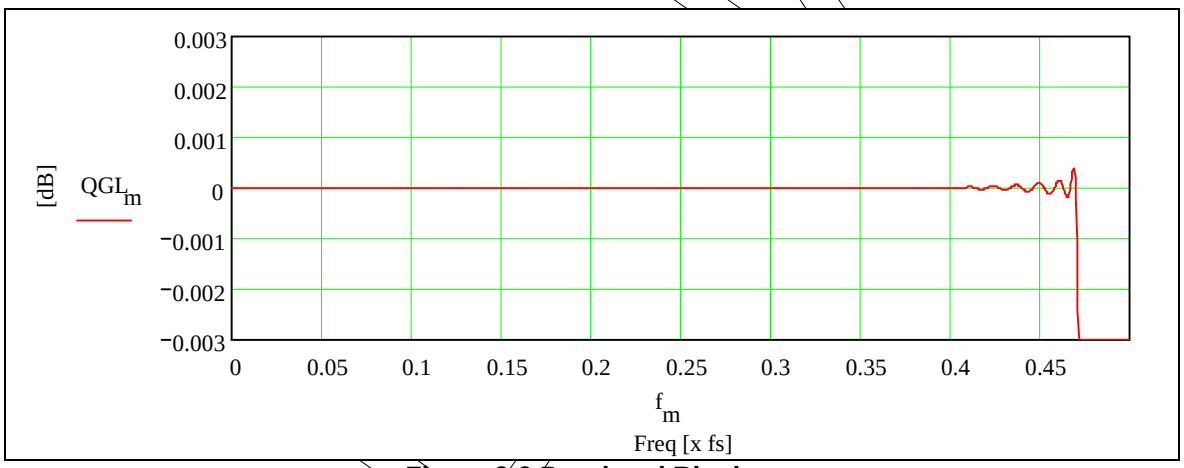


Figure 2-9 Passband Ripple

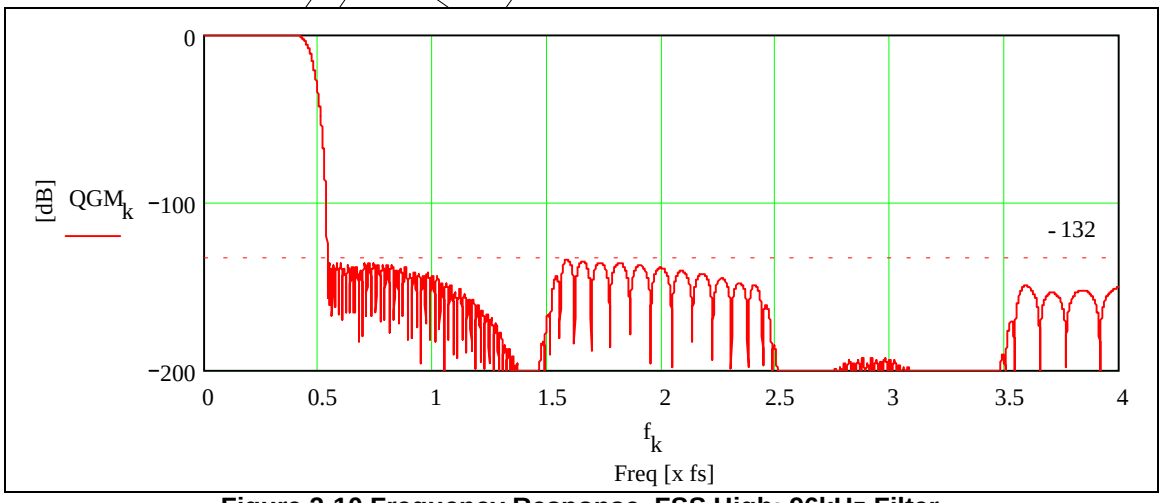


Figure 2-10 Frequency Response, FSS High: 96kHz Filter

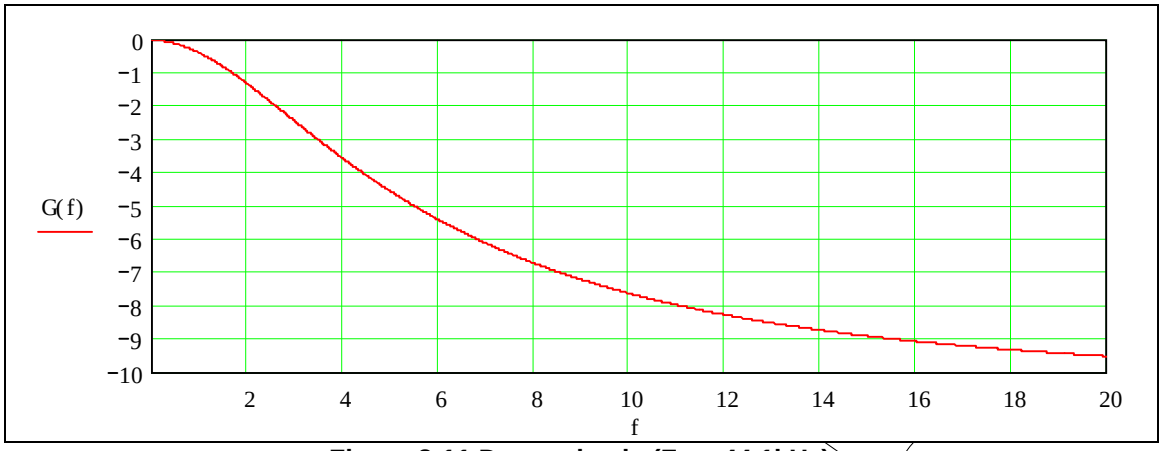


Figure 2-11 De-emphasis (Fs = 44.1kHz)

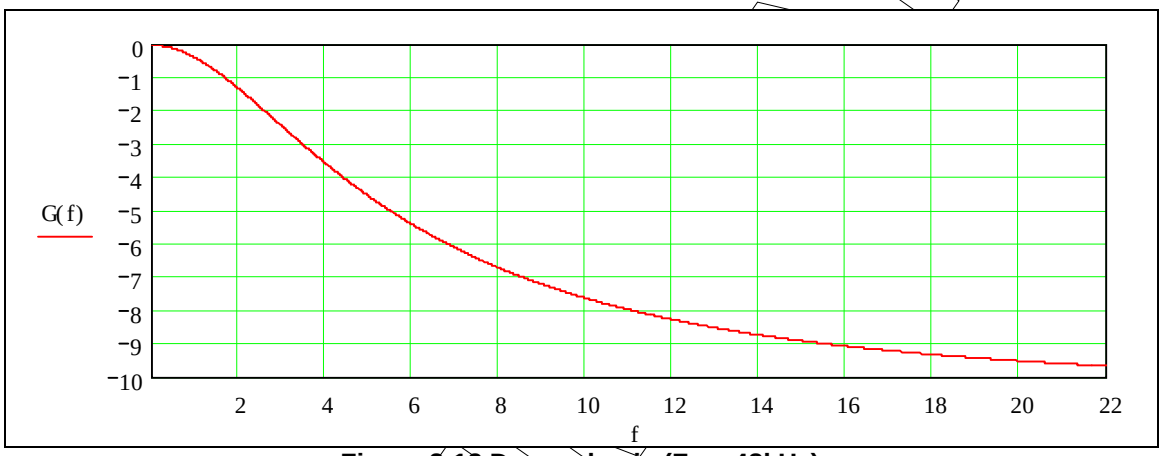


Figure 2-12 De-emphasis (Fs = 48kHz)

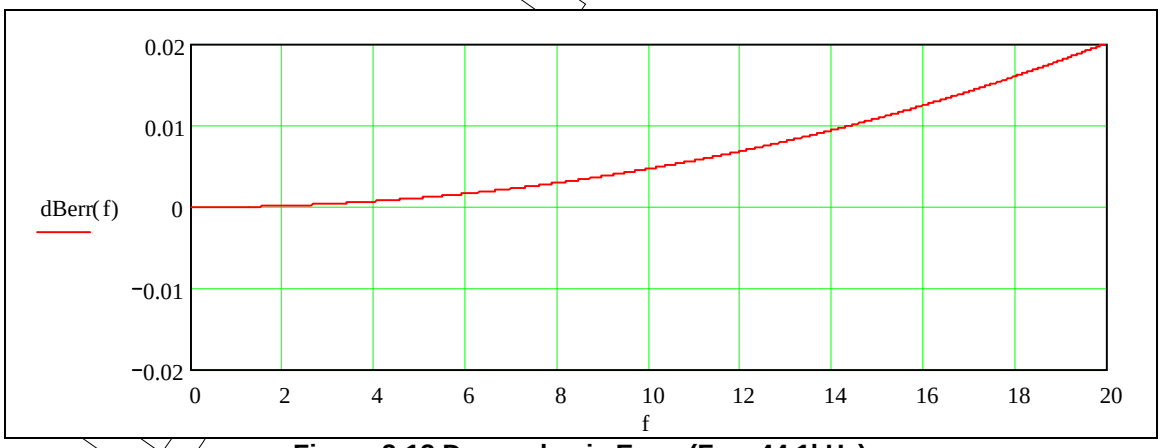


Figure 2-13 De-emphasis Error (Fs = 44.1kHz)

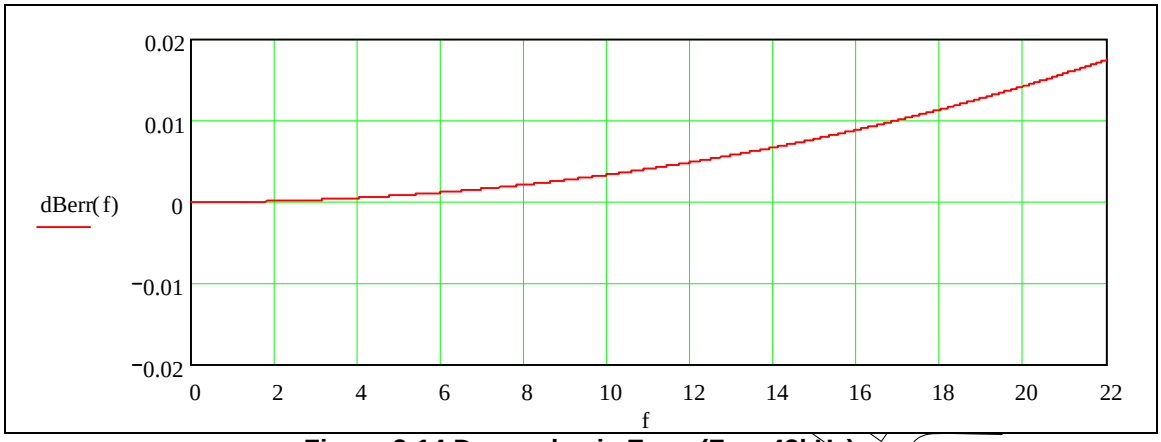


Figure 2-14 De-emphasis Error (Fs = 48kHz)

SECTION 3

CLOCK CIRCUIT

SYSTEM CLOCK

The PMD200 offers a broad variety of master clock frequencies. In Hardware mode, the master clock, can be either 256 x Fs (XTIM = LOW) or 384 x Fs (XTIM = HIGH), as selected by the XTIM pin (Fs is in the range of 16 to 50 kHz). The system clock is connected to EXTAL. In Program mode, the master clock rate can be selected between 256 x Fs, 384 x Fs, 512 x Fs, or 768 x Fs (where Fs is in the range of 16kHz to 50kHz). **Table 3-1** shows the available master clock multiples and system clock ranges. **Table 3-2** shows the internal DSP settings for use in thermal and power consumption calculations.

Table 3-1 Clock Frequencies

System Clock Range (MHz)	MasterClock Sample Rate Multiplier			Internal DSP Clock (MHz)
	16-50 kHz	32-100 kHz	64-200 kHz	
4.096 – 12.8	256	128	64	32.768 – 102.4
6.144 – 19.2	384	192	96	32.768 – 102.4
8.192 – 25.6	512	256	128	32.768 – 102.4
12.288 – 38.4	768	384	192	32.768 – 102.4

Table 3-2 Internal PLL Configuration

System Clock Multiple[1]	Internal Division Factor	Internal Multiplication Factor
256	2	16
384	3	16
512	4	16
768	6	16
Notes: 1 For Fs between 16kHz and 50kHz		

The PL Capacitor (PCAP) should be connected between the PCAP pin and PGND pin. PCAP should be a high-quality component with a tolerance of +/- 10% or better (e.g. NCO chip cap).

SECTION 4

HARDWARE MODE

INTRODUCTION
The PMD200 can be operated in a stand-alone Hardware mode. In this mode, the PMD200 emulates the functionality of the Pacific Microsonics PMD100 HDCD Decoder. The accessible functionality is a subset of the PMD200 function set.

CONTROL INTERFACE
Hardware mode is selected by tying PROG LOW. The PMD200 checks this signal as it comes out of reset. This enables the Hardware-mode-only control pins DITH, OSIZ0, OSIZ1, /COB, JUST, BCPL, FSEL, and SCAL.
NOTE: These pins are not 5V tolerant.

INPUT INTERFACE
Hardware mode supports a subset of the PMD200 input capabilities. Hardware mode only supports input sample rates of 44.1 and 48 kHz. Hardware mode does not support IIS data formats.
In right-justified mode (JUST = HIGH), only 16-bit input data is supported. In left-justified mode (JUST=LOW), data lengths up to 24 bits are supported, but only 16-bit HDCD data will be decoded (e.g. 24-bit HDCD source material will be treated as a non-HDCD source).

OUTPUT INTERFACE
Hardware mode supports a subset of the PMD200 output capabilities. The output oversampling rate is fixed at 8 x Fs. Dither is restricted to either minimal (DITH=LOW) or Triangular PDF (DITH=HIGH). Serial data is non-interleaved (left channel data on DOL, right channel data on DOR), and the word clock transitions from high to low at the end of the output word.

SECTION 5

PROGRAM MODE

INTRODUCTION

The PMD200 supports software-based configuration in the Program mode. The mode is selected when the PROG pin is HIGH when the chip comes out of reset. The PMD200 can be programmed using either the SHI or I2C bus protocols. In the case of I2C, the base address of the PMD200 is determined by the value on pins D7..D0 at reset.

Note: When in program mode, the following input pins are still valid and need to be configured: DEEMP, XTIM, HMUTE, and SMUTE.

INTERFACE FORMAT DESCRIPTION

The PMD200 reads data as 24-bit words. The 4 MSBs of the word determine the command type. The remaining 20 bits make up the data for that command. The available commands are listed in **Table 5-1**.

Table 5-1 Program Mode Commands

Command Code	Command Type
0000	Set Input Configuration
0001	Set Output Configuration
0010	Set Attenuator
0010 – 1111	Reserved

INPUT CONFIGURATION COMMAND

Table 5-2 Input Configuration Command Data Bit Values

Command Bit Number	Configuration Name	Description
0	IBCPL	**Input Bit Clock Polarity** – If BCPL is HIGH, input data is latched on the rising edge of the bit clock. On LOW, data is latched on the falling edge.
1	FSEL0	**Input Sampling Frequency** – FSEL[2..0] select the input sampling frequency. Values for FSEL[2..0] are defined in Table 5-3.
2	FSEL1	
3	FSEL2	
4	IIS	**IIS Input Mode** – When IIS is HIGH, input data starts one bit clock after the word clock edge, and input data is left-justified.
5	ISZ0	**Input Word Size** – ISZ[1..0] determine the input word size. Values for ISZ are shown in Table 5-4.
6	ISZ1	
7	JUST	**Input Data Justification** – When JUST=HIGH, input data is right-justified. When JUST=LOW, input data is left-justified.
8	XTIM0	**System Clock Multiple** – Determines the system clock frequency. See Table 5-5
9	XTIM1	
10	ISL0	**Input Slot-Length –** Determines the length in bit-clock cycles of each phase of the input word clock. Values for ISL are shown in Table 5-6
11	ISL1	
12	IFSPL	**Input Frame Sync Polarity –** When IFSPL is low, High level of the input frame sync indicates the left channel. When IFSPL is set, the high level of the input frame sync identifies left channel data
13-19	RESERVED	**Reserved** – Set to 0.
20-23	Command Type	The command code (23:20 = 0000)

Figure 5-1 Input Configuration Command Format

Table 5-3 Frequency Select Bit Values

FSEL2, FSEL1, FSEL0	Input Sampling Frequency
0,0,0	44,100
0,0,1	48,000
0,1,0	88,200
0,1,1	96,000
1,0,0	176,400
1,0,1	192,000
1,1,0	Reserved
1,1,1	Reserved

Table 5-4 Input Word Size Bit Values

ISZ1,ISZ0	Input Word Size
0,0	16 bits
0,1	18 bits (not valid for right-justified data)
1,0	20 bits
1,1	24 bits

Table 5-5 Master Clock Frequency Selection

XTIM1, XTIM0	Master Clock Multiple[1]	Master Clock Frequency Range (MHz)
0,0	256	4.096 – 12.8
0,1	384	6.144 – 19.2
1,0	512	8.192 – 25.6
1,1	768	12.288 – 38.4
Notes: 1 Master clock multiples are listed with respect to a sampling rate of 16-50 kHz		

Table 5-6 Input Data Slot Length

IFSL1,IFSL0	Input Data Slot Length
0,0	16 bit clocks
0,1	20 bit clocks
1,0	24 bit clocks
1,1	32 bit clocks

OUTPUT CONFIGURATION COMMAND

Table 5-7 Output Configuration Command Data Bit Values

Command Bit Number	Configuration Name	Description
0	$\overline{\text{COB}}$	**Complimentary Offset Binary** – When COB is LOW, output is in complimentary offset binary format. When COB is high, output is 2's-compliment.
1	DITH0	**Dither Mode** – DITH[2..0] determine the dither mode of the output. Dither modes 0-6 are increasing levels of HDCD high-frequency dither. Dither mode 7 is TPDF dither.
2	DITH1	
3	DITH2	
4	OMUL	**Output Multiplex** – When OMUL=HIGH, left and right output data is interleaved on DOL. When OMUL=LOW, left and right output data is transmitted separately on DOL and DOR.
5	OSIZ0	**Output Word Size** – OSIZ[1..0] determines the word length of output audio data. Values for OSIZ are shown in table 5-8.
6	OSIZ1	
7	POL	**Output Audio Polarity** – When POL=HIGH, the audio phase of the both output channels is inverted.
8	SCAL	**Gain Scale Enable** – When SCAL is HIGH, the 6dB gain scaling is signaled on the GAIN pin to be performed externally. When SCAL is LOW, the 6dB gain adjustment for HDCD recordings takes place digitally internal to the decoder.
9	WCPL	**Word Clock Polarity** – When WCPL is LOW, the output word clock transitions from high to low at the end of the output word. When WCPL is HIGH, the output word clock transitions from low to high at the end of the output word.
10	OVR0	**Oversampling Rate** – OVR[1..0] determine the oversampling rate of the output. Values for OVR are shown in Table 5-9. NOTE: 8x oversampling is not available for 176/192 kHz input rates.
11	OVR1	
12	OBCPL	**Output Bit Clock Polarity -** If OBCPL is HIGH, output data is valid on the rising edge of the bit clock. On LOW, data is valid on the falling edge.
13-19	RESERVED	**Reserved** – Set to 0.
20-23	Command Type	The command code (23:20 = 0001)

Figure 5-2 Output Configuration Command Format

Table 5-8 Output Word Size Bit Values

OSIZ1,OSIZ0	Output Word Size
0,0	16 bits
0,1	18 bits
1,0	20 bits
1,1	24 bits

Table 5-9 Output Oversampling Rate

OVR1,OVR0	Output Oversampling Rate
0,0	Reserved
0,1	2x
1,0	4x[1]
1,1	8x[2]

Note: 1 4x oversampling is not available at 176.2kHz or higher input sampling rates.
2 8x oversampling is not available at 88.2kHz or higher input sampling rates.

ATTENUATION COMMAND

The PMD200 implements a high-precision digital attenuator. The attenuation values are set as 9-bit values representing 0.188dB increments.

Table 5-10 Attenuation Command Bit Descriptions

Command Bit	Command Name
0-8	LeftAtten [0:8 = 0..8]
9	Reserved (set to LOW)
10-18	RightAtten[10:18 = 0..8]
19	Reserved (set to LOW)
20-23	Command code (23:20 = 0010)

Figure 5-3 Attenuator Command Format

SECTION 6

DIGITAL AUDIO INPUT INTERFACE

INTRODUCTION

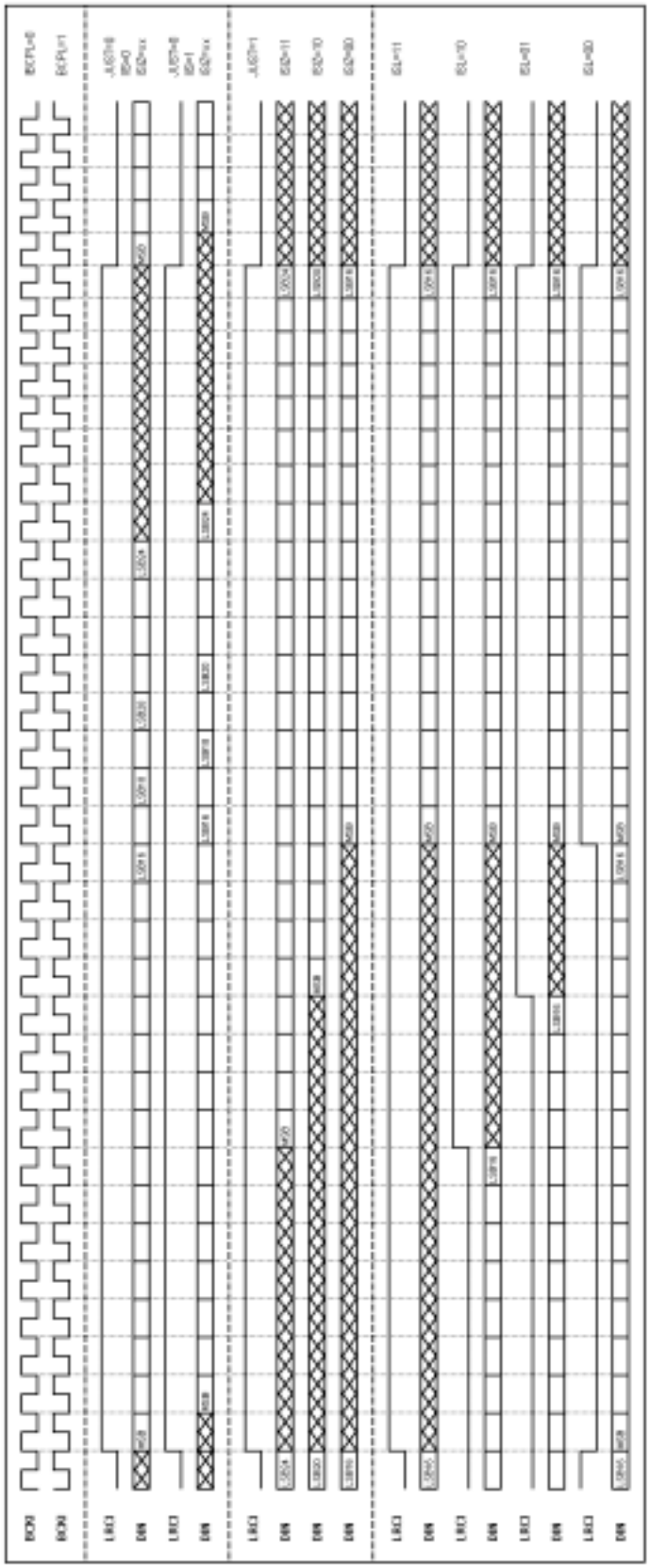
The PMD200 input interface supports a broad variety of data formats. Input data format is determined by eight signals: ISL1, ISL0, IFSPL, IBCPL, JUST, IIS, ISZ1, and ISZ0. Only IBCPL and JUST are exposed on pins in Hardware mode.

INPUT FORMAT CONFIGURATION

Table 6-1 Input Format Configuration Options

Signal	Description	Value	Result
IBCPL	Input Bit Clock Polarity	H	Input data latched on rising edge of bit clock
		L	Input data latched on falling edge of bit clock
JUST	Input Data Justification	H	Input data is right-justified, ISZ0/1 determine word length
		L	Input data is left justified, ISZ0/1 determine word length
IIS	IIS Format Support	H	Input data starts one bit clock after word clock edge
		L (default)	Input data starts/ends on word clock edge
		Note: IIS mode is not valid when JUST=H (right-justified)	
ISZ1,ISZ0	Input Word Size	L,L (default)	16-bit
		L,H	18-bit
		H,L	20-bit
		H,H	24-bit
		Note: 18-bit input word size is not valid in right-justified modes	
ISL1,ISL0	Input Slot Length	L,L	16 bit clocks
		L,H	20 bit clocks
		H,L	24 bit clocks
		H,H	32 bit clocks
		Note: Slot length must be greater than or equal to the input sample length	
IFSPL	Frame Sync Polarity	H	High-level input frame sync identifies the left channel
		L	Low-level input frame sync identifies the left channel

Figure 6-1 Digital Audio Input Data Formats



SECTION 7

OUTPUT INTERFACE

INTRODUCTION

The PMD200 output provides an extremely flexible interface to support a broad variety of digital-to-analog converters. The output format is determined by 11 signals: OSIZ0, OSIZ1, COB, WCPL, OBCPL, FSEL0, FSEL1, FSEL2, OVER0, OVER1, and OMUL. In hardware mode, only OSIZ0, OSIZ1, COB, and FSEL0 are exposed on pins. Default values are used for all other signals.

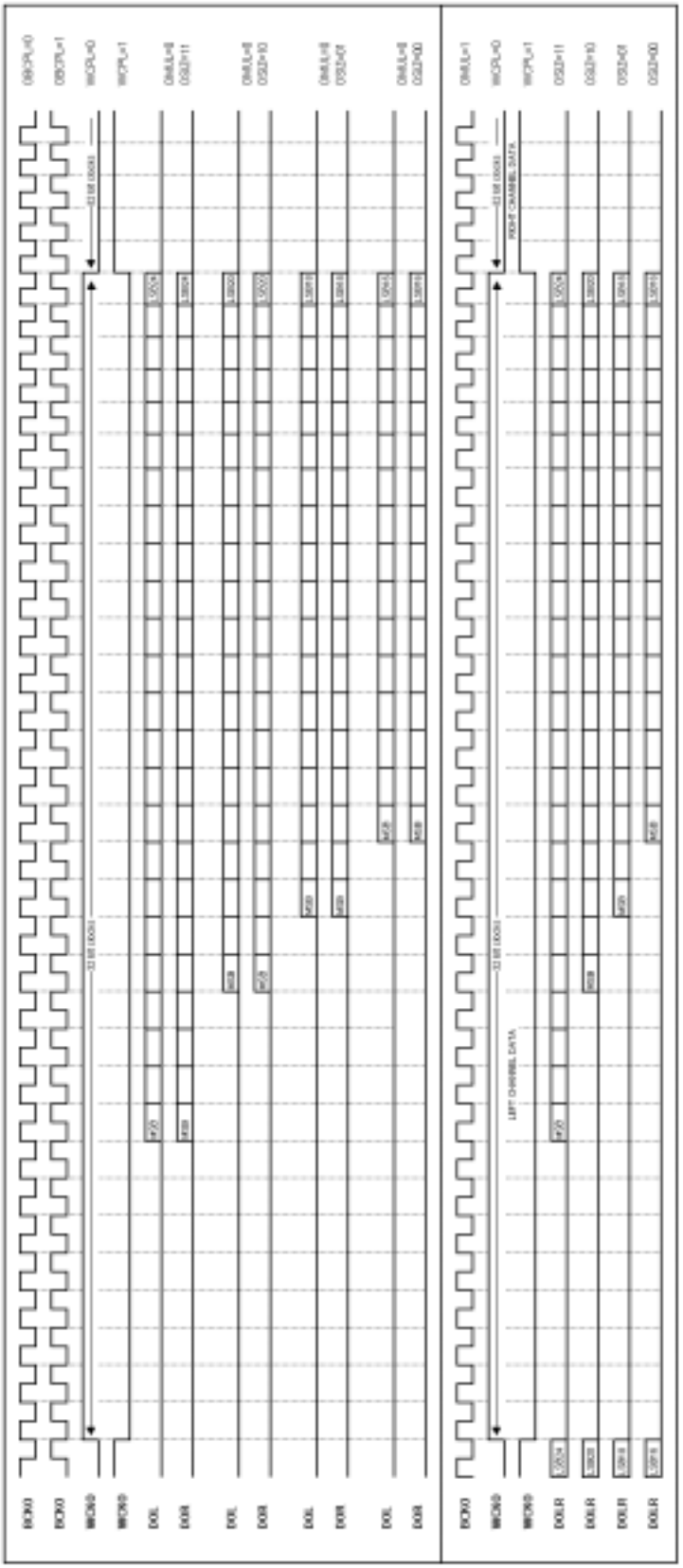
OUTPUT FORMAT CONFIGURATION

Table 7-1 Output Format Configuration Options

Signal	Description	Value	Result
COB	Complimentary Offset Binary	L	Output is in complimentary offset binary format
		H	Output is in 2's-compliment format
FSEL2,1,0	Sample Rate Select	L,L,L (default when FSEL0=L)	44,100 samples per second
		L,L,H (default when FSEL0=H)	48,000 samples per second
		L,H,L	88,200 samples per second
		L,H,H	96,000 samples per second
		H,L,L	176,400 samples per second
		H,L,H	192,000 samples per second
		H,H,x	Reserved
OVER1,0	Oversampling Rate	L,L	Reserved
		L,H	2 x FS
		H,L	4 x FS
		H,H (default)	8 x FS
		Note: 8xFS is not available for 88.2k or higher sample rates. 4xFS is not available for 176k or higher sample rates.	
OMUL	Output Multiplex	L (default)	Left output on DOL, right output on DOR
		H	Left and right outputs interleaved on DOL
OBCPL	Output Bit Clock Polarity	L (default)	Output data is valid on the rising edge of the bit clock
		H	Output data is valid on the falling edge of the bit clock

WCPL	Output Word Clock Polarity	L	Word clock transitions from high to low at the end of the output word. In multiplexed mode, low-level word clock identifies the left sample
		H	Word clock transitions from low to high at the end of the output word. In multiplexed mode, high-level word clock identifies the left sample
OSIZ1,0	Output Word Size	L,L	16-bit output samples.
		L,H	18-bit output samples.
		H,L	20-bit output samples.
		H,H	24-bit output samples

Figure 7-1 Digital Audio Output Formats



SECTION 8

DITHER

INTRODUCTION

Dither can be added to the output of the system. The dither mode is determined by three signals: DITH2, DITH1, and DITH0. Seven levels of high-frequency HDCD dither and one of TPDF dither are available. The levels are scaled to the output word size. In hardware mode, the DITH pin selects between Dither Mode 0 and Dither Mode 7.

Note: Dither is not generated for input sampling rates of 176kHz or above.

DITHER MODES

Table 8-1 Dither Options

Dither Level	DITH2	DITH1	DITH0	DITH (hardware mode only)
Mode 0	L	L	L	L
Mode 1	L	L	H	
Mode 2	L	H	L	
Mode 3	L	H	H	
Mode 4	H	L	L	
Mode 5	H	L	H	
Mode 6	H	H	L	
Mode 7 (TPDF)	H	H	H	H

SECTION 9

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for the package. The PMD200 is available in a 100-pin TQFP. Table 9-1 shows the pin/name assignments for the package.

TQFP Package Descirption

Top view of the 100-pin TQFP package is shown in Figure 9-1 with its pin-outs. The 100-pin TQFP package mechanical drawing is shown in Figure 9-2.

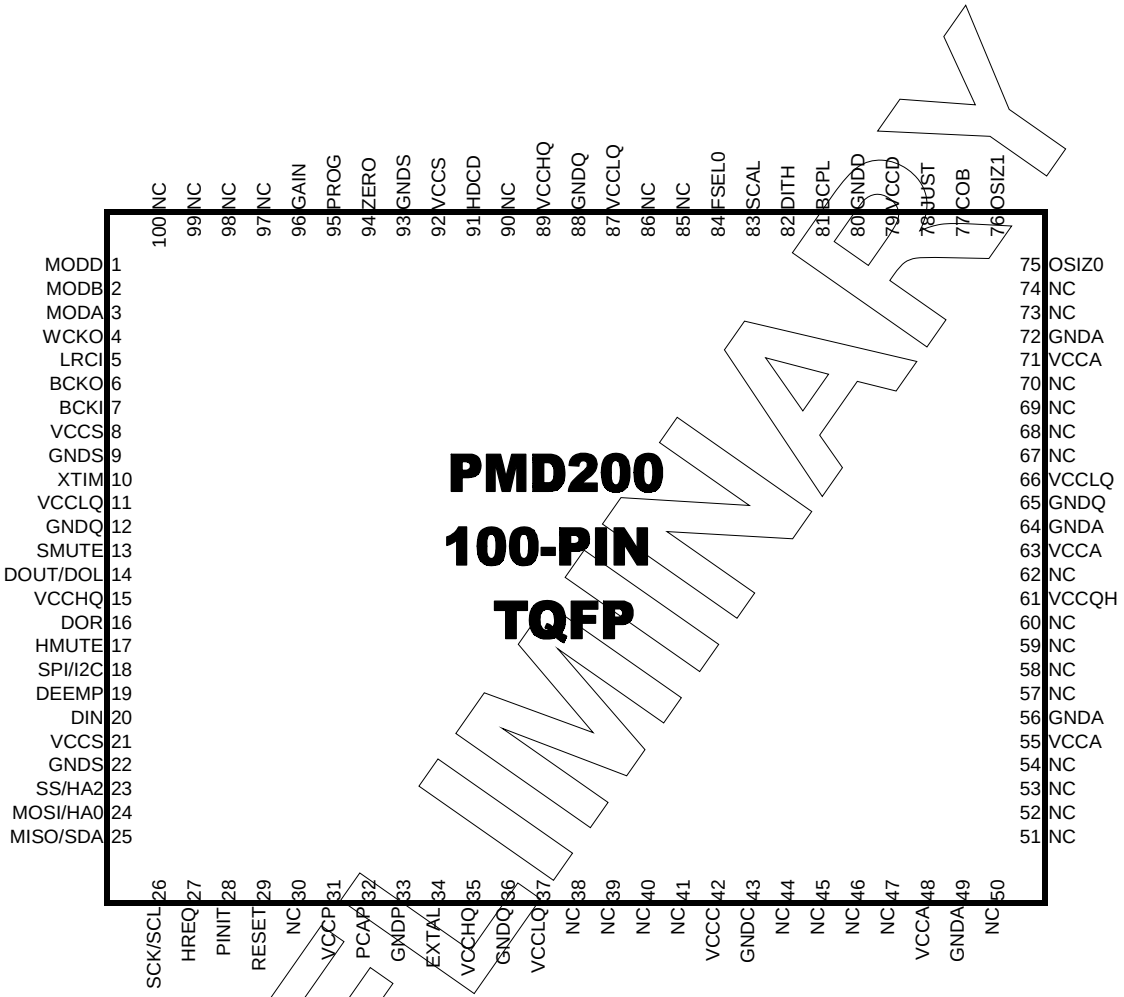


Figure 9-1 PMD200 100-Pin Thin Quad Flat Pack (TQFP), Top View

Table 9-1 Signals By Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	MODD	26	SCK/SCL	51	NC	76	OSIZ1
2	MODB	27	HREQ	52	NC	77	COB
3	MODA	28	PINIT	53	NC	78	JUST
4	WCKO	29	RESET	54	NC	79	VCCD
5	LRCI	30	NC	55	VCCA	80	GNDD
6	BCKO	31	VCCP	56	GNDA	81	BCPL
7	BCKI	32	PCAP	57	NC	82	DITH
8	VCCS	33	GNDP	58	NC	83	SCAL
9	GNDS	34	EXTAL	59	NC	84	FSEL0
10	XTIM	35	VCCHQ	60	NCNC	85	NC
11	VCCLQ	36	GNDQ	61	VCCHQ	86	NC
12	GNDQ	37	VCCLQ	62	NC	87	VCCLQ
13	SMUTE	38	NC	63	VCCA	88	GNDQ
14	DOUT/DOL	39	NC	64	GNDA	89	VCCHQ
15	VCCHQ	40	NC	65	GNDQ	90	NC
16	DOR	41	NC	66	VCCLQ	91	HDCD
17	HMUTE	42	VCCC	67	NC	92	VCCS
18	SPI/I2C	43	GNDC	68	NC	93	GNDS
19	DEEMP	44	NC	69	NC	94	ZERO
20	DIN	45	NC	70	NC	95	PROG
21	VCCS	46	NC	71	VCCA	96	GAIN
22	GNDS	47	NC	72	GNDA	97	NC
23	SS/HA2	48	VCCA	73	NC	98	NC
24	MOSI/HA0	49	GNDA	74	NC	99	NC
25	MISO/SDA	50	NC	75	OSIZ0	100	NC

Note: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MISO/SDA pin which is the Master In, Slave Out pin in SPI mode, but acts as the I2C data bus in I2C mode.

Table 9-2 Pin Number by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
BCKI	7	GNDS	93	NC	57	SCK/SCL	26
BCKO	6	HDCD	91	NC	58	SMUTE	13
BCPL	81	HMUTE	17	NC	59	SPI/I2C	18
COB	77	HREQ	27	NC	62	SS/HA2	23
DEEMP	19	JUST	78	NC	67	VCCA	48
DIN	20	LRCI	5	NC	68	VCCA	55
DITH	82	MISO/SDA	25	NC	69	VCCA	63
DOR	16	MODA	3	NC	70	VCCA	71
DOUT/DOL	14	MODB	2	NC	73	VCCC	42
EXTAL	34	MODD	1	NC	74	VCCD	79
FSEL0	84	MOSI/HA0	24	NC	85	VCCHQ	15
GAIN	96	NC	30	NC	86	VCCHQ	35
GNDA	49	NC	38	NC	90	VCCHQ	61
GNDA	56	NC	39	NC	97	VCCHQ	89
GNDA	64	NC	40	NC	98	VCCLQ	11
GNDA	72	NC	41	NC	99	VCCLQ	37
GNDC	43	NC	44	NC	100	VCCLQ	66
GNDD	80	NC	45	NC	60	VCCLQ	87
GNDP	33	NC	46	OSIZ0	75	VCCP	31
GNDQ	12	NC	47	OSIZ1	76	VCCS	8
GNDQ	36	NC	50	PCAP	32	VCCS	21
GNDQ	65	NC	51	PINIT	28	VCCS	92
GNDQ	88	NC	52	PROG	95	WCKO	4
GNDS	9	NC	53	RESET	29	XTIM	10
GNDS	22	NC	54	SCAL	83	ZERO	94

TQFP Package Mechanical Drawing

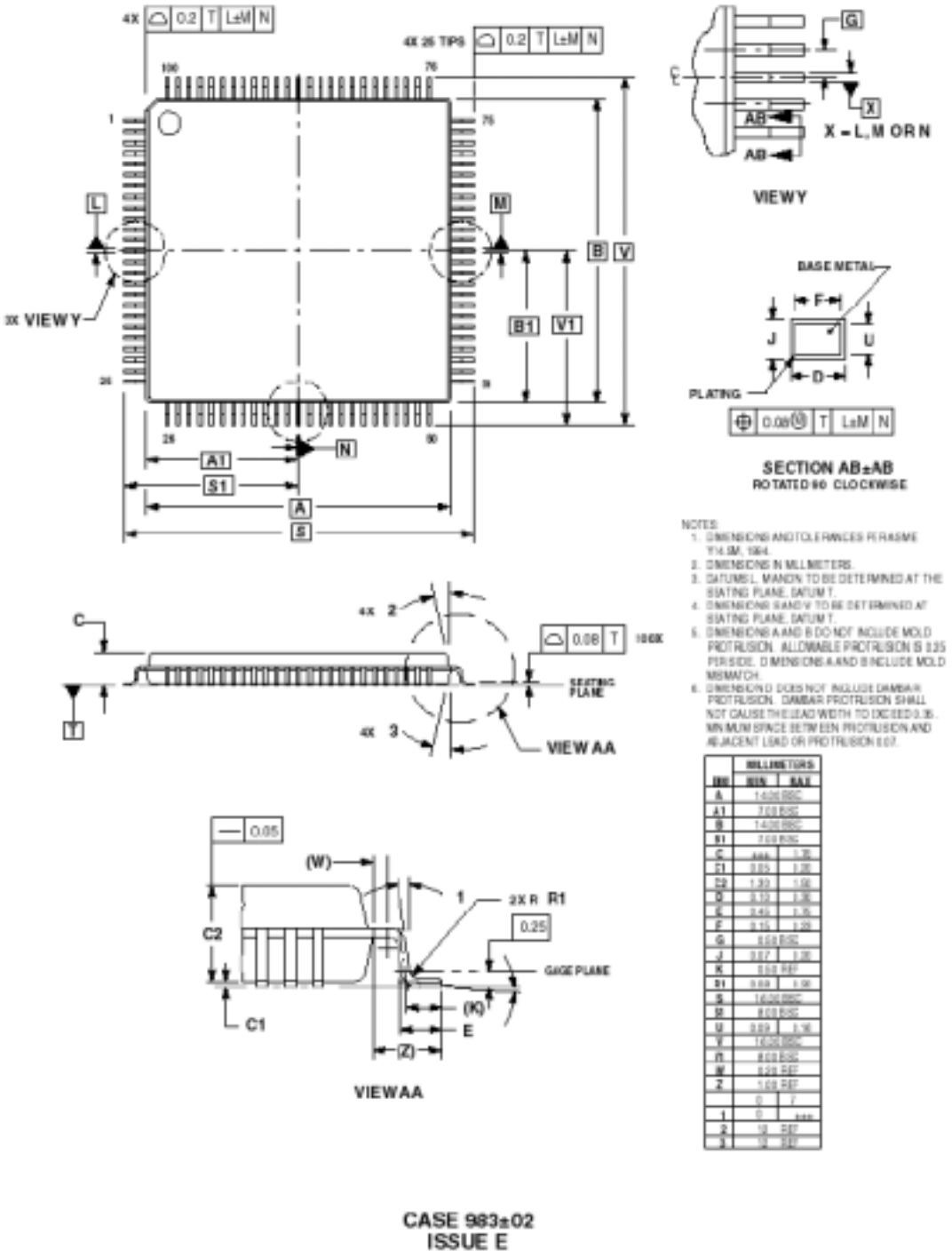


Figure 9-2 100-Pin TQFP Mechanical Drawing

ORDERING DRAWINGS

Complete mechanical information regarding the PMD200 (DSP56364) packaging is available by facsimile through Motorola's Mfax system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's personal identification number (PIN)
  Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.
- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

SECTION 10

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, TJ, in ^{o}C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where T_A = ambient temperature ^{o}C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ^{o}C/W
P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance, and a case-to-ambient thermal resistance.

$$RTJA = RTJC + RTCA$$

Where: $R_{\theta JA}$ = package junction-to-ambient thermal resistance ^{o}C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance ^{o}C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ^{o}C/W

RTJC is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, RTCA. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system-level thermal simulation tool.
The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.
A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J-T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for

determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J\text{-}T_T/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). He suggested value for a pull-up or pull-down resistor is 10kΩ.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 μF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple PMD200 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 5V-tolerant pins and the chip V_{CC} never exceeds 3.95V.

POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitacnces of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

Where C = node/pin capacitance
V = voltage swing
F = frequency of node/pin toggle

The maximum internal current (I_{CCI} max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions. For applications that require very low current consumption, do the following:

- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.

PLL PERFORMANCE ISSUES

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

INPUT (EXTAL) JITTER REQUIREMENTS

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

SECTION 11

ORDERING INFORMATION

Ordering information will be provided when it becomes available.

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