Si570 Clock Board V3.5 user guide

By Ian Jin Ver. 0.9b

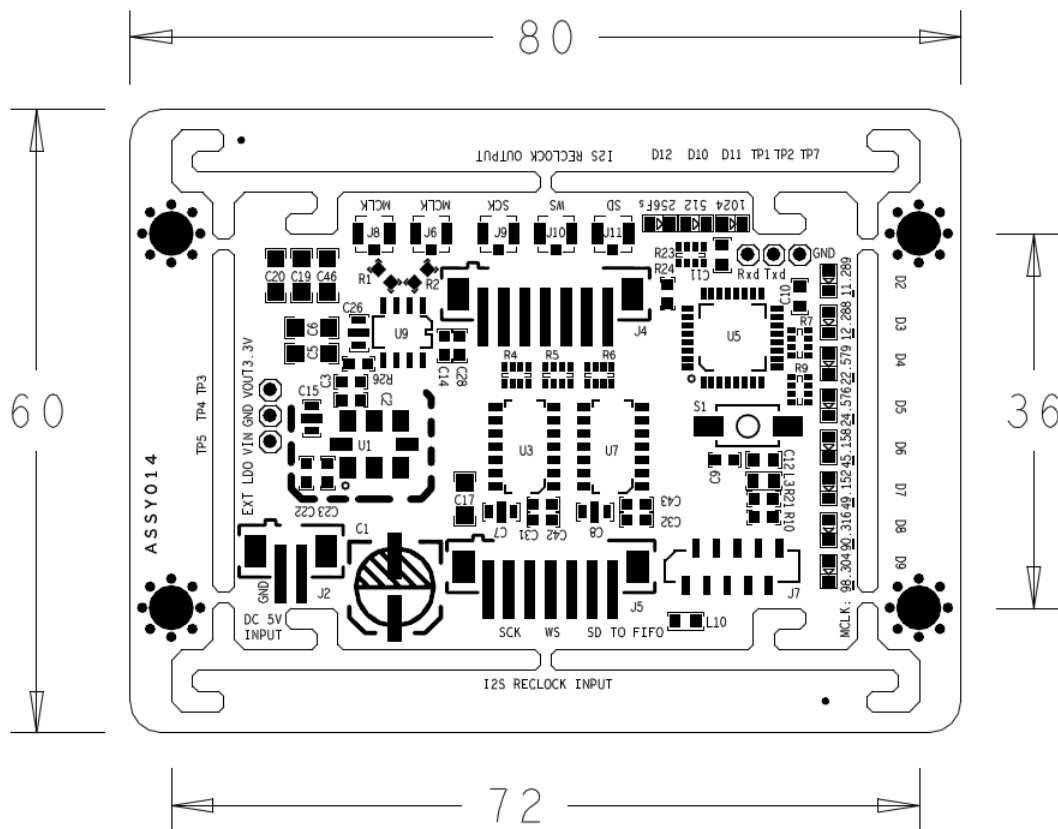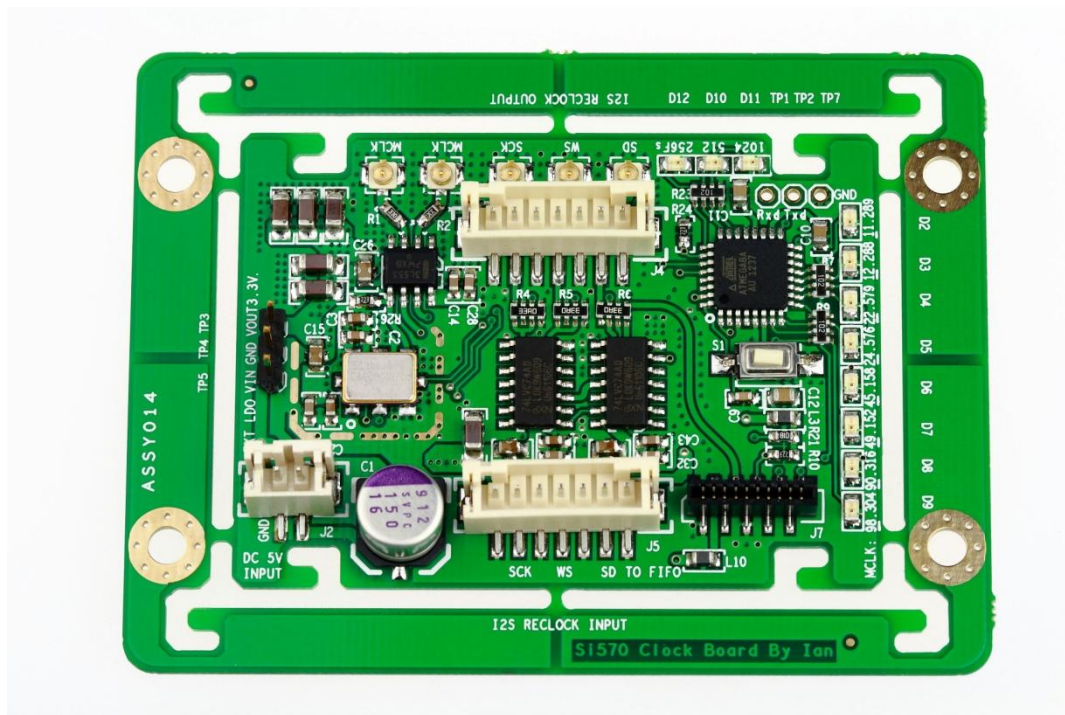## Features and specifications

1. MCLK frequencies: 11.2896MHz, 12.2880MHz, 22.5792MHz, 24.5760MHz, 45.1584MHz, 49.1520 MHz, 90.3168 MHz, 98.3040MHz(factory default)

2. MCLK xFs: 256*Fs, 512*Fs, 1024*Fs,2048*Fs

3. Supporting audio frequencies: 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz, 352.8KHz, 384KHz

4. MCLK output: Two source terminated 50ohm u.fl output ports and one un-terminated u.fl output, LVTTL level

5. Working mode: FIFO mode and standalone mode

6. Inverted MCLK: Enabled as default

7. External Controller: Support via USART

8. Automatic Fs switching function: Supported at FIFO mode, Frequency/xFs combination strategy is settable, external third party controller can take over as well

9. Dual mono DAC support: Native

10. I2S Re-clocking: Included

11. Power : DC input 4V-6V, 150mA, from FCC/FPC cable or external DC input

12. Phase noise* (dBc/Hz)

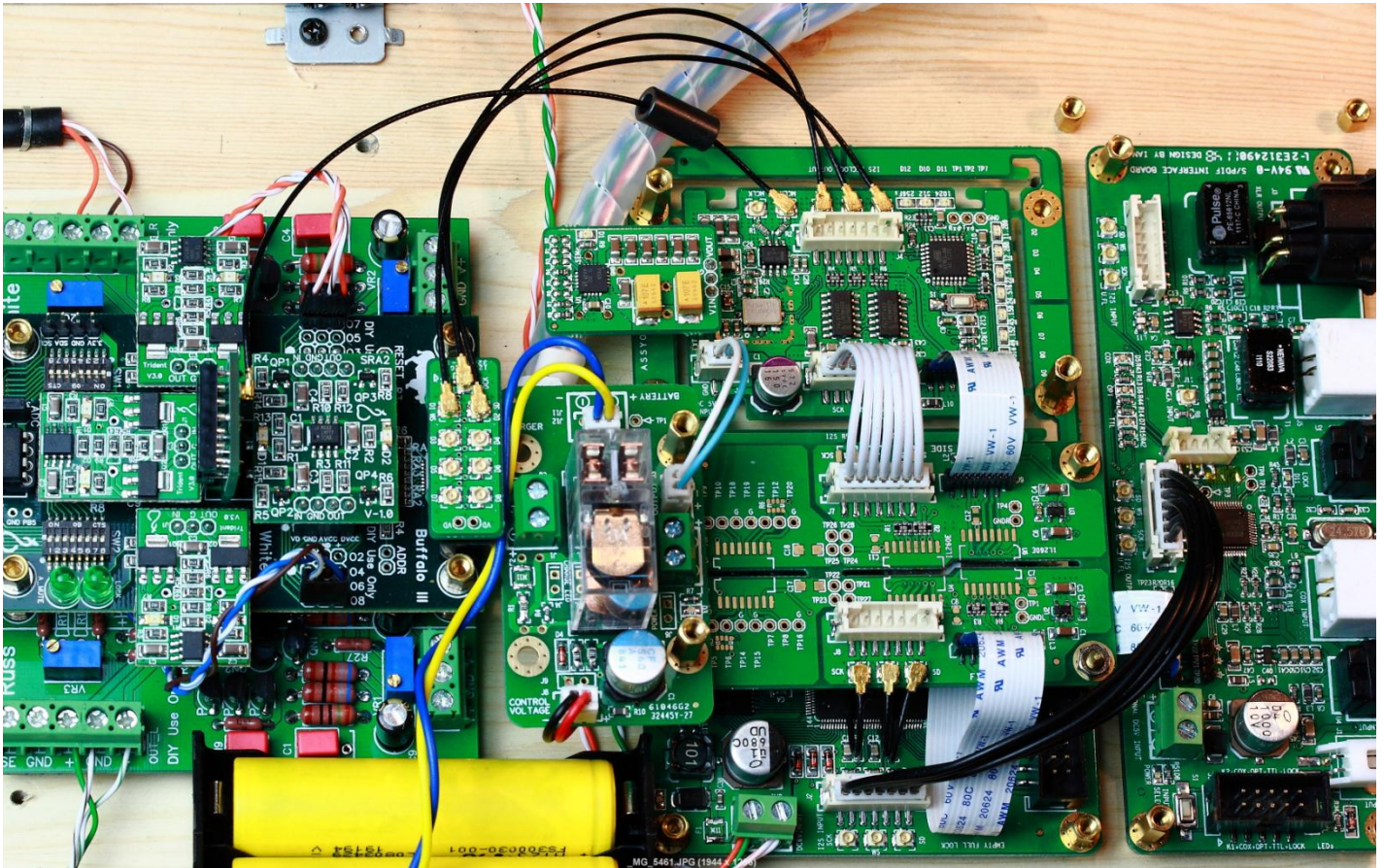|	
100Hz	-112
1KHz	-122
10KHz	-132
1MHz	-137
10MHz	-150

13. Period Jitter*:   2ps RMS, 14ps Peak-to-Peak

14. Frequency Stability*: ±50ppm
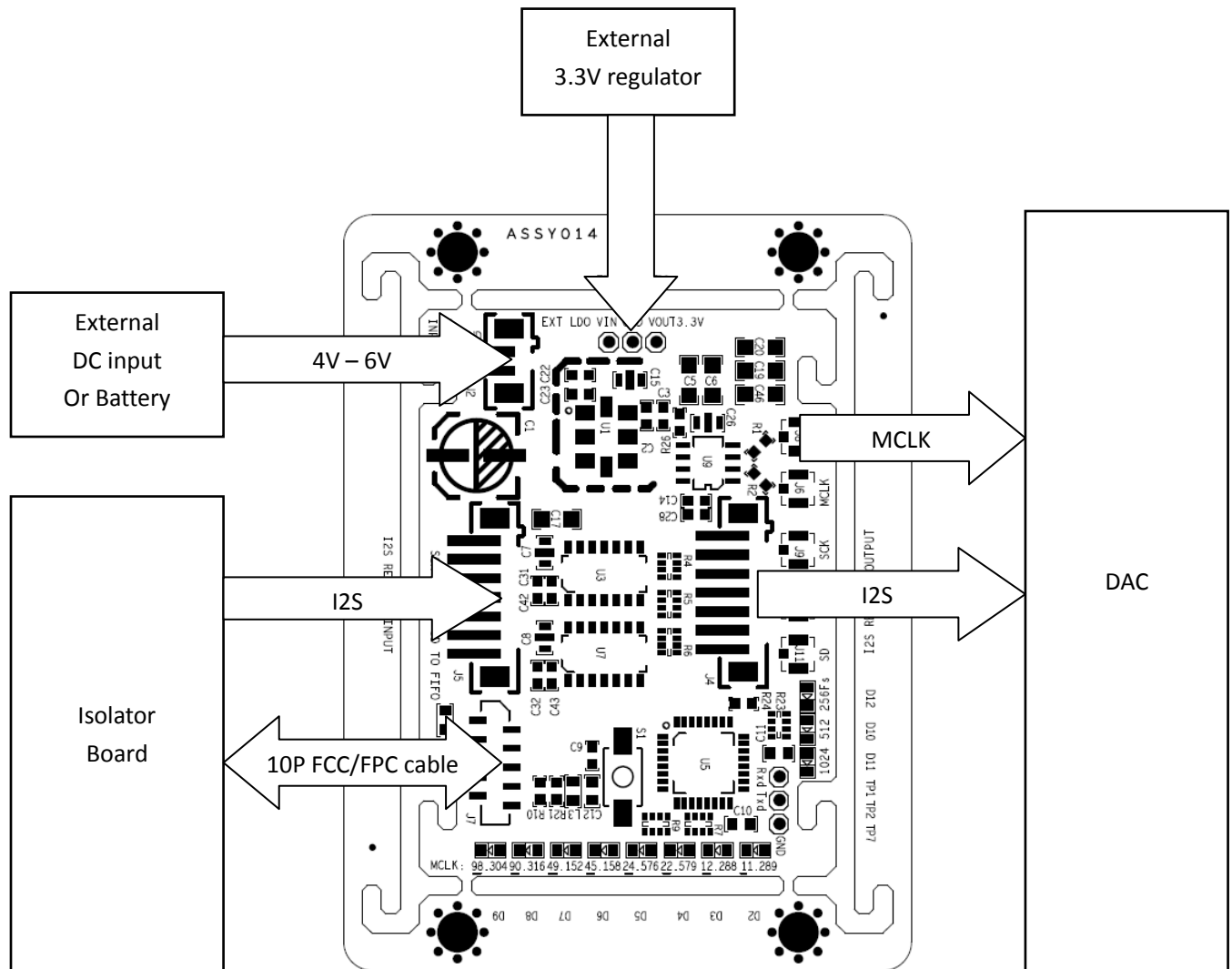
Note*: From Silicon Labs Si570 datasheet

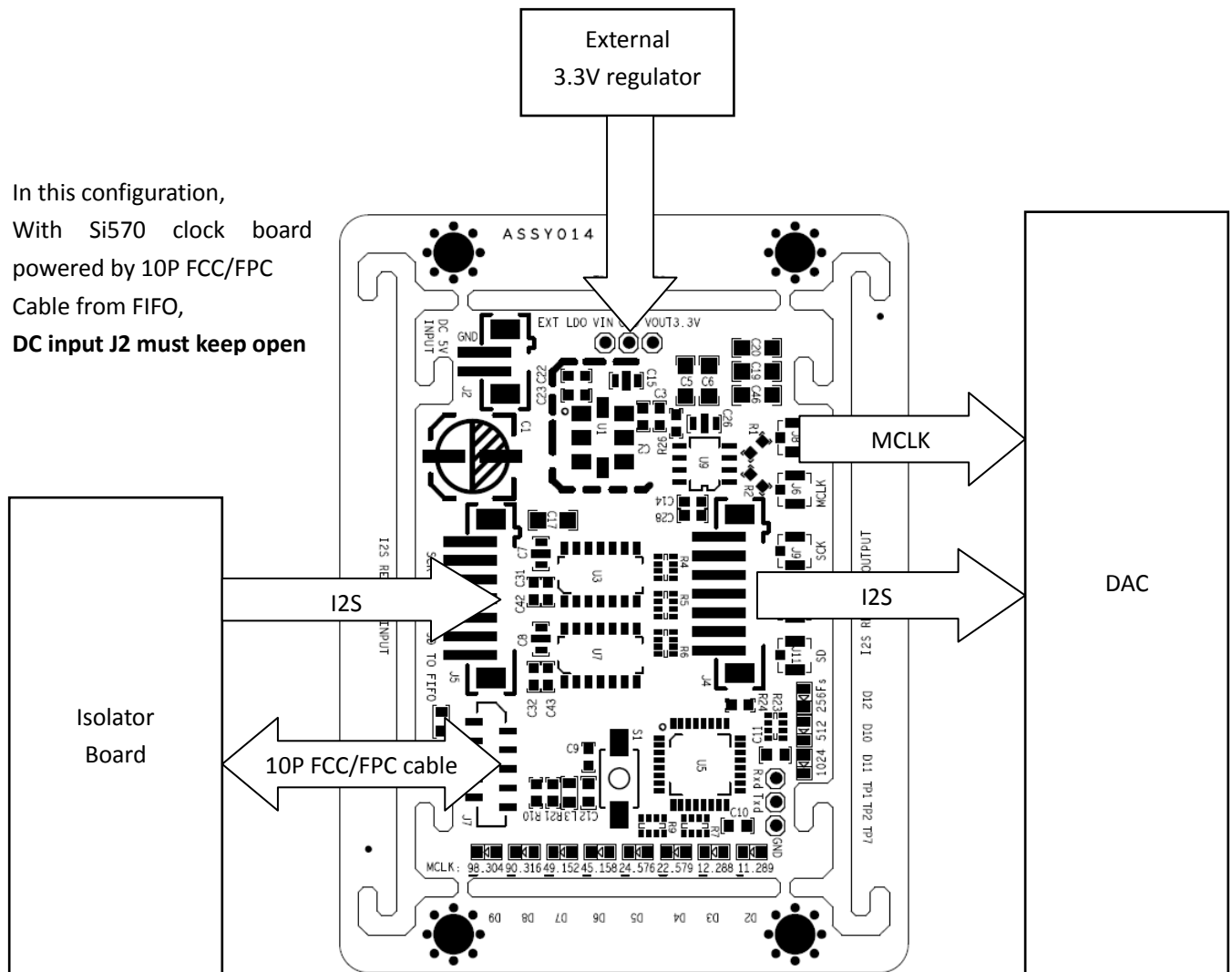## Layout and dimensions (in mm)

Typical system configuration

Integrating into system with FIFO and DAC via isolator (recommended)

Integrating into system with FIFO and DAC without isolator

External
3.3V regulator

In this configuration,
With Si570 clock board
powered by 10P FCC/FPC
Cable from FIFO,
DC input J2 must keep open

Isolator
Board

I2S

10P FCC/FPC cable

MCLK

I2S

DAC

Working at standalone mode

Si570 clock board can work at standalone mode as a universal digital audio clock generator without connecting to a FIFO. At this mode, frequencies could be set manually at any time by the on-board push button. The setting will be stored into onboard flash memory and will be recall automatically after each power up

Connectors and indicators

Connectors	Descriptions	Notes	Type	Comment
MCLK	Two MCLK outputs in 50ohm U.FL	Two of them Equivalent in function but from different driver. Use any of them for stereo DAC or both of them for dual mono DACs (Do not connect to S/PDIF board)	U.FL	A must for DACs in sync mode
J5	I2S input for re-clocking 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Connecting to I2S source on isolator board, FIFO board or other I2S devices according to the working mode	7P PH2.0mm	recommended
SCK,WS,SD	I2S re-clocking output in 50ohm U.FL	Connecting to I2S input of DAC Equivalent in function to J4 with better signal integrity, recommended	U.FL	recommended
J12,J13,J14	Optional I2S re-clocking output in 50ohm U.FL	Second group of I2S output for dual mono DACs Equivalent in function to above I2S output with individual source terminating resistors, U.FL sockets need to be assembled in if use	U.FL	optional
J2	DC input 1 – GND 2 – DC 4V – 6V	Need to connect to external DC power or battery if works together with an isolator board or at standalone mode. Must be kept un-connected if works with FIFO directly without a isolator board	2P PH2.0mm	Conditional
TP3,TP4,TP5	External 3.3V regulator TP5 – VIN TP4 – GND TP3 - VOUT	TPS7A4700 low noise LDO board is recommended See related section for details	SIP3 2.54mm	Must
J7	Control cable	Connect to isolator board or FIFO board if works with	10P FPC	A must except at standalone
S1	Setting button For manual frequency setting or frequency/xfs combination setting	See related section for details	Push button	

Connectors	Descriptions	Notes	Type	Comment
TP1,TP2,TP7	External controller TP1- Rxd TP2 – Txd TP7 – GND	USART port for optional external controller See related section for details	SIP3 2.54mm	Optional
J1	Optional MCLK	Optional un-terminated MCLK output U.FL socket need to be assembled in case of use. Cable has to be very short or be terminated at device end	U.FL	No recommended
J15, J16, J17	Optional I2S input for re-clocking In U.FL 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Alternative option to J5, equivalent in function U.FL sockets need to be assembled in case of use	U.FL	Optional
J4	Optional I2S re-clocking output 2 – SCK 4 – WS 6 – SD 1,3,5,7 – GND	Alternative option to I2S output in U.FL, equivalent in function, Use above I2S output in U.FL if it is possible	7P PH2.0mm	Optional Use I2S output in U.FL if it is possible
D6 – D9	MCLK indicators	Indicating current MCLK frequency 11.2896MHz, 12.2880MHz, 22.5792MHz, 24.5760MHz, 45.1584MHz, 49.1520 MHz, 90.3168 MHz, 98.3040MHz	8 LED	
D10 – D12	xFs indicators	Indicating current xFs 256*Fs, 512*Fs, 1024*Fs, 2048*Fs (All on)	3 LED	

*Note: I2S signal names are based on the I2S standard. Other names might be linked as below:

BCK = SCK, LRCK = WS, DATA= SD

External regulator solutions

3.3V external regulator has to be connected into TP3, TP4, TP5. High quality low noise external power supply could be employed to boost the Si570 performance. This external regulator will significantly change the sound quality of Si570 clock board. Carefully selection on this regulator is required according to personal preference.
Some of the possible regulator solutions are:

1, TPS7A4700 low noise LDO board (recommended)
This LDO board is confirmed to be one of the best LDO boards so far to power the Si570 clock board. You can plug it into the 3P SIP socket, but it would be better soldering directly to the pins once you decided to stick with it. TPS7A4700 regulator board could be placed both in vertical and in horizontal position to the clock board.

Please note, the six output capacitors on right side of the TPS7A4700 regulator board affect the sound style of the Si570 clock board significantly. Changes and improvements will be made if replace them with different kind of MLCC.

2, Third party 3PIN regulator boards
Many candidates are available. But have to make sure the output current is enough to power Si570 clock board which is rated at 150mA.

3, Shunt regulators
Any 3.3V Shunt regulator can work for the Si570 clock board. But the high frequency performance has to be confirmed suitable powering oscillators.

4, Direct 3.4V LiFePO4 battery cell
To achieve this configuration, we have to
(1), Running Si570 clock board with an isolator board or in standalone mode
(2), Short TP5(VIN) and TP3(VOUT) pins by a jumper
(3), Connect to a 3.4V LiFePO4 battery cell via battery management board from DC input connector J2.
If running with an isolator board, half of the isolator board will be powered by the same 3.4V battery automatically from 10P FFC/FPC cable on J7. Usually we don't need remove or bypass the LDO on isolator board because most of LDOs is tested still be capable enough to power the half isolator with 3.4V input (the output will be a bit lower than 3.3V).

5, Standard TO220-3 3.3V 3 terminal regular IC
Pin to pin compatible stand LDO IC, such as 78M33, is working. But not recommended for real operating because of the poor output noise performance.

Please note, a good linear regulator for an audio amplifier may no longer be good for an oscillator. To power a XO, we need a regulator not only has perfect low noise performance but also can keep that good performance for high frequency RF/VCO applications.

DC Power of Si570 Clock Board

There are two ways powering the Si570 clock board: Power from FIFO by 10P FFC/FPC cable via J7, or power from external power supply via DC input J2. They are suitable for different situations:

1, Work with FIFO via an isolator board (recommended)
This the best way running the clock board to ensure lowest EMI noise by cutting the ground loop. In this case, you have to power the Si570 clock board from external power supply by DC input J2. Very well filtered and regulated DC power supply is required. Battery based DC power solutions are recommended to achieve super low noise performance. Please note, in this case, half of the isolator board will be powered from a same DC power.

2, Work with FIFO without an isolator board
In this case, Si570 clock board is powered automatically from the 10P FFC/FPC cable by FIFO. You have to leave the DC input connector J2 unconnected, otherwise the two DC powers will be short together, except you remove L10 on the Si570 clock board, which is not recommended.

3, Running Si570 clock board as a standalone audio clock generator without connecting to a FIFO
In this case, you have to power the Si570 clock board from external power supply by DC input J2, as same as the first case.

Manually Setting frequencies

When work as a universal digital audio clock generator, frequencies could be set manually at any time by the push button. The setting will be stored into onboard flash memory and will be recall automatically after each power up.

To set a desired output frequency, we need

1, Keep press and hold the on board push button S1 for more than two seconds.

2, The frequency LED indicators will start flashing and then scanning.

3, Release button S1 at the moment when the LED of desired frequency is lighting

4, That LED will flash for a while and then becomes solid light which indicates new frequency is set with success.

Automatic Fs switching function and frequency/xFs combination group

When work together with a FIFO, frequencies and xFs will be switched automatically according to the input I2S Fs and the preset frequency and xFs combination group.   Four pre-set combination groups are:

//Group1:   Si570 frequency and *Fs combination for low MCLK range
{F112896, 256*FS},   44.1 KHz
{F122880, 256*FS},   48 KHz
{F225792, 256*FS},   88.2 KHz
{F245760, 256*FS},   96 KHz
{F451584, 256*FS},   176.4KHz
{F491520, 256*FS},   192 KHz
{F903168, 256*FS},   352.8KHz
{F983040, 256*FS}   384 KHz

// Group2:   Si570 frequency and *Fs combination for low mid MCLK range
{F225792, 512*FS},   44.1 KHz
{F245760, 512*FS},   48 KHz
{F225792, 256*FS},   88.2 KHz
{F245760, 256*FS},   96 KHz
{F451584, 256*FS},   176.4KHz
{F491520, 256*FS},   192 KHz
{F903168, 256*FS},   352.8KHz
{F983040, 256*FS}   384 KHz

// Group3:   Si570 frequency and *Fs combination for middle MCLK range
{F451584, 1024*FS},   44.1 KHz
{F491520, 1024*FS},   48 KHz
{F451584, 512*FS },   88.2 KHz
{F491520, 512*FS },   96 KHz
{F451584, 256*FS },   176.4KHz
{F491520, 256*FS },   192 KHz
{F903168, 256*FS },   352.8KHz
{F983040, 256*FS }   384 KHz

// Group4:   Si570 frequency and *Fs combination for high MCLK (**factory default**)
{F903168, 2048*FS},   44.1 KHz
{F983040, 2048*FS},   48 KHz
{F903168, 1024*FS},   88.2 KHz
{F983040, 1024*FS},   96 KHz
{F903168, 512*FS },   176.4KHz
{F983040, 512*FS },   192 KHz
{F903168, 256*FS },   352.8KHz
{F983040, 256*FS }   384 KHz

Group4 is highly recommended for ESS DACs .

The default combination groups could be programmed by the on-board push button and will be saved into on-board flash memory.

To program the group1 as the default combination: manually set frequency to 12.2880MHz or 11.2896MHz;

To program the group2 as the default combination: manually set frequency to 24.5760MHz or 22.5792MHz;

To program the group3 as the default combination: manually set frequency to 49.1520MHz or 45.1584MHz;

To program the group4 as the default combination: manually set frequency to 98.3040MHz or 90.3168MHz;

Inverted MCLK function

Inverted MCLK function is enabled as factory default. This feature was designed to optimize the noise performance at synchronous mode according to ESS DAC application note. With this function, the raising edge of the MCLK will be half period prior to the changing on I2S signals. Positive result shows based on the real listening testing. This feature may also be good for other DACs.

To disable this function in case of doing research or for other applications, you have to

1, Remove U2

2, Short R28 with a 0 ohm 0603 jumper.

External controller and communication protocol (optional for high level user)

Si570 driver opens status display and part of frequency control to third party external controller from a UART now. The USART is reserved on board as TP1,TP2 and TP7. USART isolator is recommended if running with a external controller.

Here is the communication protocol:

//Si570 multi-frequency clock board serial communication protocol V1.0 2012-11-03 by Ian
//USART 9600,n,8,1

//events sent from si570 driver
//Format: 0xAA,EVENT,DATA,0x55
//EVENTS:
#define GETNEWFS   0xC1   //FIFO detected a new Fs which need a new MCLK frequency
#define SETFRQ   0xC2   //new Si570 frequency is set
#define SETXFS   0xC3   //new xfs is set
#define WRONGINPUTCMD   0xC4   //wrong input commend or no input command
#define WRONGINPUTFRQ   0xC5   //input frequency is overange
#define INVALIDINPUTFRQ   0xC6   //input frequency is invalid for current Fs

//Command response from external controller
//Format: 0xA5,CMD,DATA,0x5A
//0xC8 command has to be sent within 100ms after getting event 0xC1,
//otherwise Si570 driver will determine the setting frequency and xfs according to the preset without stop the music
//CMD:
#define TOINPUTFRQ   0xC8   //set frequency for the new detected Fs by external controller

//sample frequency data of event 0xC1,
//#define FS22   0
//#define FS24   1
//#define FS44   2
//#define FS48   3
//#define FS88   4

```
//#define FS96        5
//#define FS174       6
//#define FS192       7
//#define FS352       8
//#define FS384       9

//xfs data for event 0xC3
//#define XFS256      0
//#define XFS512      1
//#define XFS1024     2
//#define XFS2048     3

//frequency data for event 0xC2 and command 0xC8
//#define F112896     0
//#define F122880     1
//#define F225792     2
//#define F245760     3
//#define F451584     4
//#define F491520     5
//#define F903168     6
//#define F983040     7
```

Driving dual mono DAC

Si570 clock board was designed natively supporting DACs in dual mono configuration.

To run DAC in dual mono mode, I'm highly recommended using u.fl coaxial cables with same length for both of the block to guarantee signals arrive at same moment (every 1 inch 50ohm coaxial cable will cause roughly 120ps!).   In this case, U.FL sockets for the second group of I2S output have to be mounted on footprints of J12,J13 and J14 at bottom side of PCB.

Application notes

1. Si570 clock board is optimized for digital audio application which requires high frequency MCLK up to 98.3040MHz, as well as the multi-frequency output capability. The Si570 clock board may not be your best choice if you just want to stick with low frequency MCLK, for example, 22.5792MHz, 24.5760MHz.

2. Si570 clock board is working at double speed mode natively. I don't suggest feeding the MCLK from it into DIT section of the S/PDIF board to set up a S/PDIF FIFO (DIR no any problem). If you really want, you have to feed the MCLK from FIFO board to S/PDIF board rather than from Si570 clock board.

3. Si570 is a XO based programmable oscillator with high Q crystal inside the metal case. Normally, it needs a couple of hours to burn in before really going stable if being used it for the first time. A couple of minutes warm up time are also required at each power up time.

4. Power supply affects the sound quality and style significantly to this Si570 clock board. Selecting and turning the power supply with careful is very important to achieve best performance according to personal preference. Please see the related tips for details.

5. Si570 Clock Board was preset at 98.3040MHz and combination group 4 as factory default. You can connect it right away to an ESS DAC at both SYNC/ASYNC modes and both stereo and dual mono configuration. However, to drive other DACs, you have to set the MCLK frequency and the xFs combination group manually according to the DAC specification before first time running to avoid any possible problem.

6. Different MCLK/Xfs combination group may sound difference even playing a same I2S track.

Tips of further improvements

1. Power supply decides the sound quality of this Si570 clock board. Choosing a good external regulator is very important to achieve better performance.

2. Output capacitors on TPS7A4700 LDO board, affect the sound quality significantly. The output capacitors assembled on the finished TPS7A4700 LDO board are 10uF 25V X7R MLCC. They sound with great details, quiet background and beautiful high range. But I came across other kind of 10uF 16V X7R MLCC which has wonderful middle range. If it is possible, try different output capacitors to meet best personal preference.

3. DC input is also very important. Ultra low noise DC power is preferred. Battery based DC power with passive management board is recommended to get good result simply.

4. Try good optional output capacitors at bottom side of PCB: C4, C16, C40, C41, C44. Footprint: 1206. Available for MLCC or A size TANT capacitors. C36, C39 available for E size TANT capacitor or bigger package MLCC. X7R or high grade is required if going with MLCC. Have to make sure the external LDO is working with bigger capacitive load.

5. Try optional input capacitors at bottom side of PCB: C38. Footprint E size. Available for TANT or suitable size MLCC.

6. If you want, you can replace the flip-flops with 74G74 to give a try. The 74G74 comes with 0.2ns less Tpd than the one from NXP. Based on my testing result, both of them have very good re-clocking performance. ESS DAC locks perfectly for both of them at lowest bandwidth without any problem. I didn't notice any difference on sound quality in between. Maybe you can. However, if you want going with dual mono DAC configuration, please make sure 74G74 has enough driving current to keep the good raising/falling time and logic level.

7. Optional shield case over Si570 chip is expected to be positive to block EMI noise.

8. Rubber suspensions are also recommended to reduce mechanical vibration which will cause piezoelectric effect on both crystal and MCLL.

Period jitter measurement result of Si570 Clock Board in time domain

1. Jitter measurement result

    Period jitter (RMS): 3.85 ps
    Period jitter peak-to-peak: $\pm$12ps
    Jitter distribution: Gaussian
    Frequency: 98.3097MHz

2. Testing condition

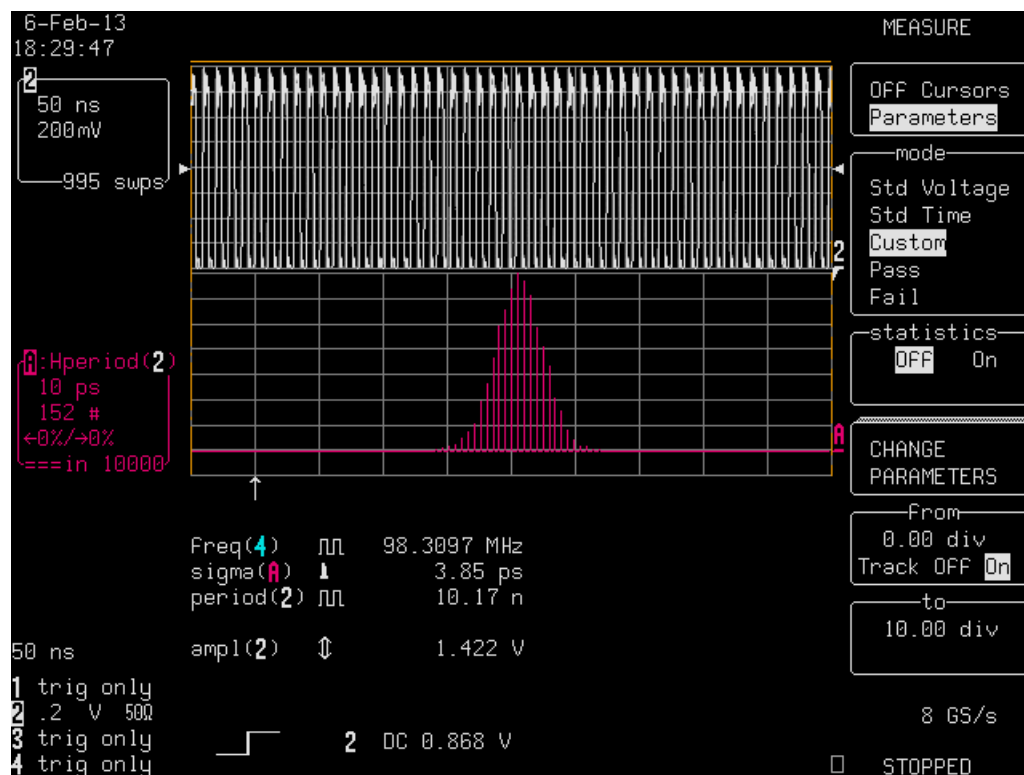   Testing equipment: LeCroy LC584AXL with JTA package

    Jitter measurement noise floor of: 2 ps

    Number of Samples: N=10,000 cycle

    Sampling: 8 GS/s

3. Some notes

    This testing result is just for reference. Different Si570 chip may come with slightly different jitter performance. Measuring clock period jitter in time domain is the easiest way to evaluate a clock, but may not be the best solution. The best way to analyze jitter of a clock is measuring the phase noise in frequency domain by a signal source analyzer. Phase noise plot can tell more details by spectrum.