



时钟设置
 1.当28脚CKSEL=L时,PLL方式,无需外接晶体
 2.当CKSEL=H时,XTI方式

设置SCKO
 13,14脚

设置输出格式(输出格式为I2S、左校验、右校验等.)
 25,26脚

16 bit MSB first, Right justified (支持的数字位数: DF1706、SM5813、和已加转换模块为DF1700的DF1704、SM5847)
 18/24 bit格式 (支持使用IIS格式的数字位数: TDAI307、SAA7226、NOS/ITDAI54)

24 bit MSB first, Left justified (典型支持的数字位数为 PMD109, 晶片的PMD109 或者 使用IC14 则晶片与IC13 脚对应)

24 bit MSB first, Right justified (支持SM5842、DF1704、DF1706、SM5847、PCM179X系列、AD195X系列、CS4398系列等等)

OUTPUT IN CLOCK FROM DATA SOURCE	CKPOL	DATA POL
24 bit MSB first, Right justified	0	0
16 bit MSB first, Right justified	0	0
18 bit MSB first, Right justified	0	0
24 bit MSB first, Left justified	0	1
24 bit MSB first, Right justified	1	0
24 bit MSB first, Right justified	1	1

OUTPUT SERIAL AUDIO DATA OUTPUT FORMAT	DATA POL	CKPOL
16 bit MSB first, Right justified	0	0
18 bit MSB first, Right justified	0	0
24 bit MSB first, Right justified	0	0
24 bit MSB first, Left justified	0	1
24 bit MSB first, Right justified	1	0
24 bit MSB first, Right justified	1	1

File	Number	Revision
A1		
File	11-Jan-2011	Sheet of
File	15-AMP-COMP-PCB-10b	Drawn by: